# A 5 GHz 7.2 dB NF low power direct conversion receiver front-end with balun LNA*

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**Abstract:** A 5GHz low power direct conversion receiver radio frequency front-end with balun LNA is presented. A hybrid common gate and common source structure balun LNA is adopted, and the capacitive cross-coupling technique is used to reduce the noise contribution of the common source transistor. To obtain low $1/f$ noise and high linearity, a current mode passive mixer is preferred and realized. A current mode switching scheme can switch between high and low gain modes, and meanwhile it can not only perform good linearity but save power consumption at low gain mode. The front-end chip is manufactured on a 0.13-$\mu$m CMOS process and occupies an active chip area of 1.2 mm$^2$. It achieves 35 dB conversion gain across 4.9–5.1 GHz, a noise figure of 7.2 dB and an IIP3 of –16.8 dBm, while consuming 28.4 mA from a 1.2 V power supply at high gain mode. Its conversion gain is 13 dB with an IIP3 of 5.2 dBm and consumes 21.5 mA at low gain mode.

**Key words:** 5GHz; balun LNA; capacitive cross-coupling; current mode passive mixer; current mode switching
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## 1. Introduction

With the proliferation of wireless local area networks (WLANs) operating in mobile devices such as cellular phones and tablet PCs, the WLAN solution demands low cost, low power consumption and high performance implementation[1, 2]. As one of the WLAN protocols, IEEE 802.11a standard operates in the 5 GHz band, which provides a total signal bandwidth of 300 MHz and its data rate can reach to 54 Mb/s. As to IEEE 802.11n standard, it works at 2.4 GHz and 5 GHz bands using multi-in multi-out (MIMO) technique, which can improve the data rate up to 600 Mb/s. As a result, a high performance transceiver working at 5 GHz deserves great attention. Since the receiver radio frequency (RF) front-end plays an important part in the transceiver system, this paper focuses on the study and design of a 5 GHz direct conversion receiver RF front-end. Several performance aspects such as gain, noise, linearity and power consumption are discussed.

## 2. Front-end architecture

The block diagram of the receiver RF front-end is as shown in Fig. 1. Direct conversion architecture is chosen due to its high level of integration and the simplicity of the baseband circuitry[3]. The RF front-end consists of two major blocks: balun low noise amplifier (LNA) and current mode passive mixer.

In the receiver RF front-end, single-ended input LNA is preferred to save I/O pins because antennas and RF filters usually produce single ended signals. However, differential signaling in the receiver chain is preferred in order to reject power and substrate noise and to reduce second-order distortion. To satisfy both requirements above and save the off-chip balun which has typically 0.5–1 dB insertion loss, the balun LNA is selected in this design.

Regarding the mixer, current mode passive mixer is used. Firstly, it has good $1/f$ noise performance because there is no DC current flowing through the switching devices[4, 5]. Secondly, operating the passive mixer in the current mode with low load impedance improves its linearity since it eliminates the distortion caused by a large voltage swing at the mixer input compared with the voltage mode active or passive mixers[5, 6]. In addition, the transimpedance amplifier used in the passive mixer can not only change the current into voltage but also serve as a first-order active filter.

According to the system simulation, the RF front-end should meet the specification requirements shown in Table 1.

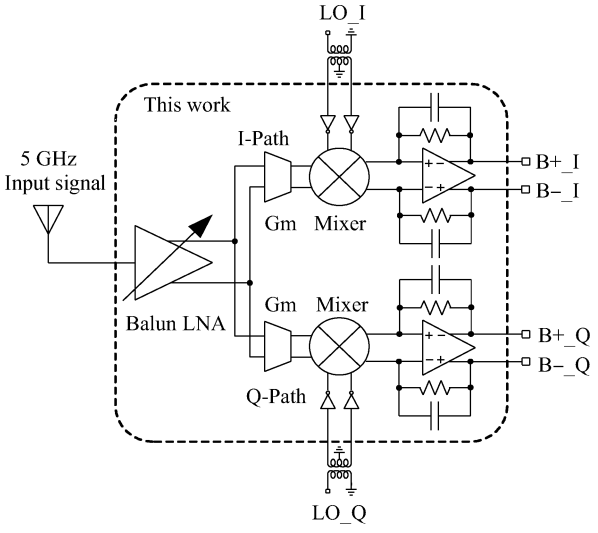


Fig. 1. Block diagram of the receiver RF front-end.

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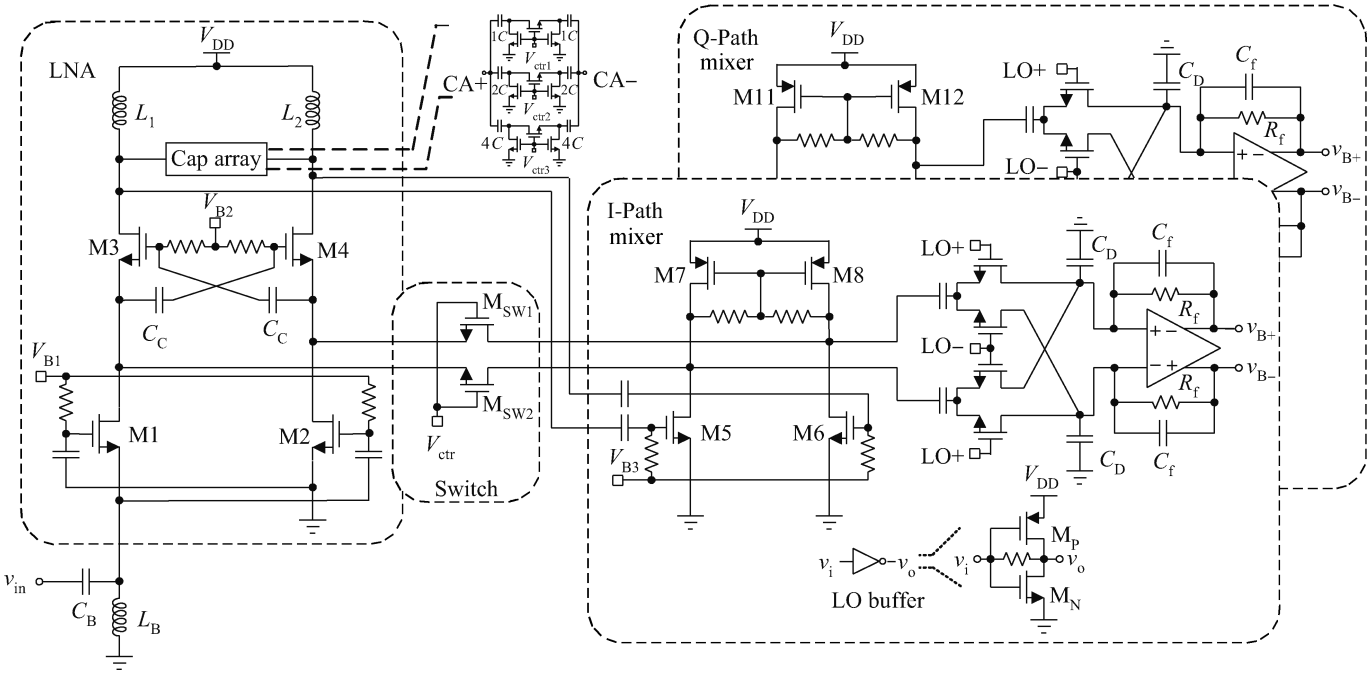


Fig. 2. Schematic of receiver RF front-end.

Table 1. Specification of the RF front-end.

| $S_{11}$ (dB) | Gain (dB) | NF (dB) | $IIP_3$ (dBm) | $P_{1dB}$ @ Low gain (dBm) | Power (mW) |
|---|---|---|---|---|---|
| $< -10$ | 35 | $< 9$ | $> -20$ | $> -24$ | $< 40$ |

## 3. Front-end design

Figure 2 shows the RF front-end circuit of the receiver. In this section, analysis and design of the balun LNA and current mode passive mixer are demonstrated in detail. The gain control scheme is specially highlighted.

### 3.1. Balun LNA

The balun LNA has been demonstrated successfully by using the common-gate common-source (CG–CS) amplifier topology recently, which exhibits not only single to differential conversion but also noise cancellation[7]. Due to its easy input matching property across large bandwidth, this type of balun LNA shown in Fig. 3 is usually applied to the broadband system. However, to reduce the off-chip balun and eliminate its insertion loss affection, the balun LNA with inductive load is preferred in this design. To simplify the analysis, resistive load is substituted with the inductive load.

The input impedance of the balun LNA is $1/g_{m1}$. If $R_s = 1/g_{m1} = 50\ \Omega$, the input matching can be achieved across a broad band. From simple derivation the voltage gain can be written as $A_V = g_{m1}R_{L1} + g_{m2}R_{L2}$. The output noise power of the circuit can be calculated and divided by the noise contribution of the signal source, which leads to the noise figure

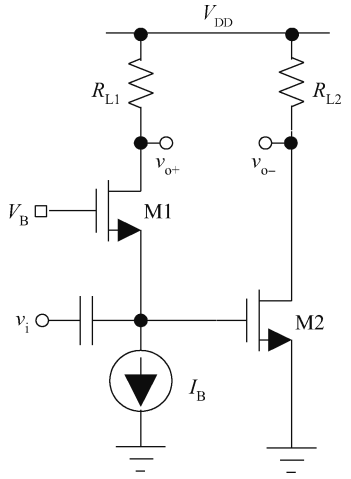


Fig. 3. Schematic of CG-CS balun LNA.

$$\begin{aligned} \mathrm{NF} = 1 &+ \frac{\gamma g_{m1}(R_{L1} - R_S g_{m2} R_{L2})^2}{R_S A_V^2} \\ &+ \frac{\gamma g_{m2} R_{L2}^2 (1 + g_{m1} R_S)^2}{R_S A_V^2} \\ &+ \frac{(R_{L1} + R_{L2})(1 + g_{m1} R_S)^2}{R_S A_V^2}. \end{aligned} \tag{1}$$

The noise current of M1 is common mode signal to the output; therefore it can be eliminated when the gains of CG and CS amplifier are the same. This conclusion can be validated from Eq. (1). Assuming that $\gamma = 1$, $1/g_{m1} = 1/g_{m2} = R_s = 50\ \Omega$, $R_{L1} = R_{L2} = 250\ \Omega$, then the voltage gain is 20 dB and noise figure is 3.8 dB which is a poor noise performance. To decrease the noise figure, Reference [7] increases the CS input transconductance $g_{m2}$ and decreases its load resistance $R_{L2}$

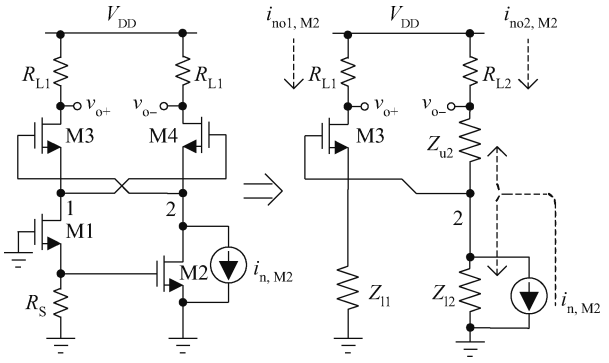


Fig. 4. Equivalent circuit for M2 noise analysis of balun LNA.

while keeping a balanced output. By designing $g_{m2} = 4g_{m1}$, NF can be reduced to 3 dB at the 5 GHz band with power consumption of 14 mW.

In this design, we adopt the capacitive cross-coupling technique to reduce the M2 channel noise current without increasing power consumption as shown in Fig. 2[6]. The coupling results in a negative feed-forward path to improve NF performance of the balun LNA.

The output noise due to M2 is analyzed by the equivalent circuit, as illustrated in Fig. 4. Transistor M1, M2 and M4 are each replaced by an effective impedance and cross-coupling capacitor $C_C$ is ignored as $C_C \gg C_{gs3,4}$. The output noise current $i_{no2,M2}$ is determined by current division principle at node 2 using the impedance ratio, while $i_{no1,M2}$ is generated through M3 acting as a CS amplifier with degenerative resistor $Z_{l1}$. Therefore, the two output noise current can be expressed respectively as

$$i_{no2,M2} = \frac{Z_{l2}}{Z_{u2} + Z_{l2}} i_{n,M2}, \tag{2}$$

$$i_{no1,M2} = -\frac{g_{m3}}{1 + g_{m3}Z_{l1}}(Z_{u2}||Z_{l2})i_{n,M2}$$

$$\approx -\frac{Z_{u2}Z_{l2}}{Z_{l1}(Z_{l2} + Z_{u2})} i_{n,M2}. \tag{3}$$

The final output noise current generated from M2 channel noise current is the difference between $i_{no1,M2}$ and $i_{no2,M2}$ as

$$i_{no,M2} = i_{no1,M2} - i_{no2,M2} = -\frac{1 + \dfrac{Z_{u2}}{Z_{l1}}}{1 + \dfrac{Z_{u2}}{Z_{l2}}} i_{n,M2}. \tag{4}$$

Like the algebraic derivations in Ref. [6], $Z_{u2} \approx Z_{l2}$ and $Z_{l1} \approx 4Z_{l2}$ can be obtained. Then we can get that $i_{no,M2} = -0.625 i_{n,M2}$ and the noise contribution of the M2 reduces to 39% of the balun LNA without using capacitive cross-coupling technique. Simulation result directly shows that noise contribution of M2 is reduced from 52% to 33%.

A 3-bit capacitor array is inserted at the output terminal of the balun LNA to adjust the output resonance frequency to the targeted 5 GHz. The proposed balun LNA's noise figure is 0.6 dB better than the conventional one and it performs a noise figure of 3.3 dB, a voltage gain of 28.4 dB and –0.5 dBm IIP3 while dissipating 5.6 mA from a 1.2 V supply.

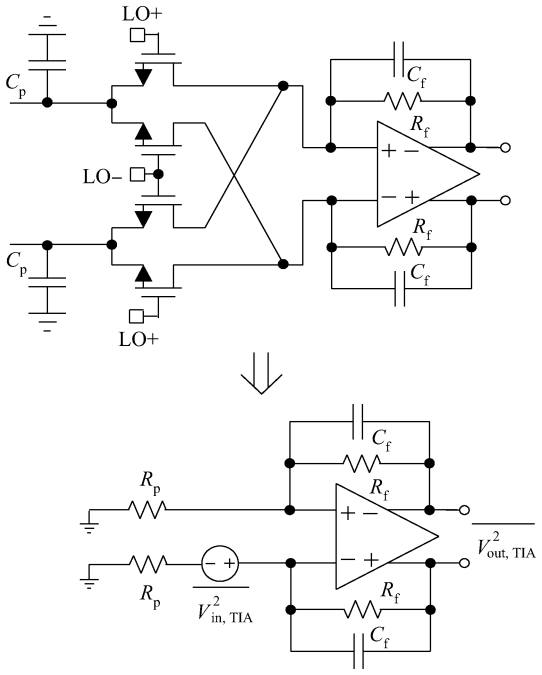


Fig. 5. Equivalent switch capacitor network for noise calculation.

### 3.2. Passive mixer

The double balanced topology mixer is widely used because it minimizes the LO feedthrough and rejects the noise from LO circuitry[8]. Especially for direct conversion receiver, less self-mixing is achieved using double balanced structure. As discussed in Section 2, the current mode passive mixer has good $1/f$ noise and linearity performance. It is composed of a transconductance stage, a switching quad and a transimpedance amplifier (TIA) with a feedback resistor and capacitor, as shown in Fig. 2. Next conversion gain, noise and linearity performance of the current mode passive mixer are analyzed.

#### 3.2.1. Conversion gain

The conversion gain of the passive mixer with ideal square wave switching can be expressed as[8]

$$\mathrm{CG} = \frac{v_{B+} - v_{B-}}{v_{in}} = \frac{2}{\pi} g_m R_f, \tag{5}$$

where $g_m$ is the transconductance of M5 and M6, and $R_f$ is the feedback resistance of the TIA. In practice, the actual gain will be smaller due to the parasitic capacitances at the source terminal of the switches and at the transconductance stage that shunt part of the RF signal to ground. Therefore, special care should be taken for the sizing and layout of the switch and transconductance stage transistors so that they do not add too much parasitic capacitances.

#### 3.2.2. Noise

$1/f$ noise is a critical problem in direct conversion receiver design and current mode passive mixer has much lower $1/f$ noise because there is no DC current flowing through the switching quad. In fact, the main $1/f$ noise source of the current mode passive mixer is the TIA. In addition, the TIA will

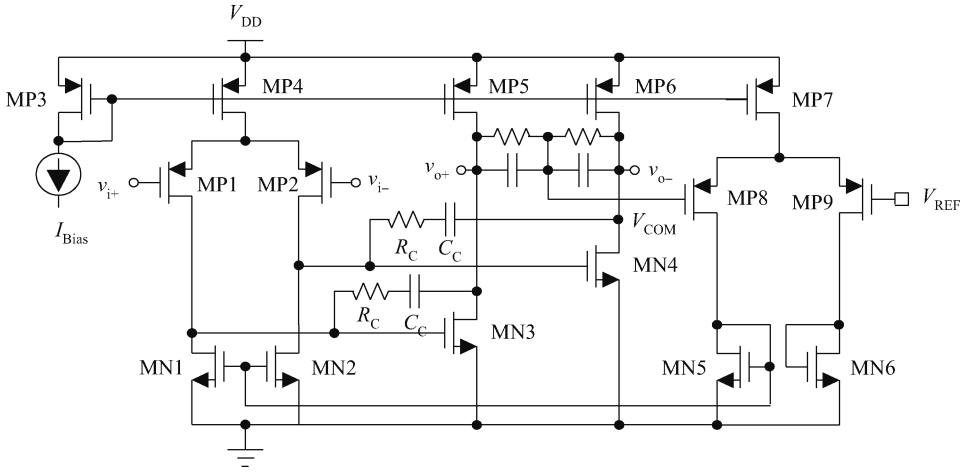


Fig. 6. Schematic of the TIA used in passive mixer.

degrade thermal noise performance of the receiver. As shown in Fig. 5, there is an equivalent resistor $R_p$ across the two virtual ground nodes, produced by the switching of all the parasitic capacitors $C_p$ at the mixer input. Like classical switch capacitor circuits, the equivalent resistance is expressed as[5]

$$R_p = \frac{1}{2f_{LO}C_p}. \tag{6}$$

If the TIA's equivalent input noise is $\overline{v_{in,TIA}^2}$, then the total output noise from the TIA can be given by

$$\overline{v_{out,TIA}^2} = \left(1 + \frac{2R_f}{R_p}\right)^2 \overline{v_{in,TIA}^2} = (1 + 4f_{LO}C_pR_f)^2\overline{v_{in,TIA}^2}, \tag{7}$$

where $R_f$ is the feedback resistor, $f_{LO}$ is the LO frequency. From Eq. (7) we can see that $C_p$ plays an important role in minimizing the output noise of the TIA. As a result, careful sizing the switching devices and layout are indispensible to minimize the parasitic capacitance $C_p$.

Three noise sources of passive mixer are: the input transistors of the transconductance stage, feedback resistor $R_f$ and the TIA. To have a clear understanding of the noise contribution from these three parts, the equivalent input noise of the mixer is derived as

$$\begin{aligned}\overline{v_{in,mixer}^2} &= \frac{\overline{v_{out,g_m}^2} + \overline{v_{out,R_f}^2} + \overline{v_{out,TIA}^2}}{CG^2} \\ &= \frac{8kT\gamma g_m R_f^2 + 8kTR_f + (1 + 4f_{LO}C_pR_f)^2\overline{v_{in,TIA}^2}}{\left(\frac{2}{\pi}g_mR_f\right)^2} \\ &= \frac{2kT\gamma g_m + 2kT\frac{1}{R_f} + \left[\frac{1}{2R_f} + 2f_{LO}C_p\right]^2\overline{v_{in,TIA}^2}}{\left(\frac{g_m}{\pi}\right)^2}.\end{aligned} \tag{8}$$

Equation (8) clearly shows that increasing $g_m$ and $R_f$ can improve the noise figure of the mixer. However, this should compromise the linearity performance, which is analyzed below. In addition, the TIA noise performance is also critical. Next, the TIA design considerations are presented.

The TIA is a two-stage operational amplifier, as shown in Fig. 6. Its bandwidth must be large enough to maintain the virtual ground effective across the whole channel band. The unit gain bandwidth of this TIA is 384 MHz with 60° phase margin. RC feedback is applied to produce a 20 MHz pole frequency. To reduce the $1/f$ noise of the TIA, large input PMOS transistors (900/0.8 $\mu$m) biased in weak reversion are used. The equivalent input referred white noise of the TIA is $\frac{2nV}{\sqrt{Hz}}$ with a current consumption of 5.5 mA.

The LO signals are AC coupled to the mixers, which allows for the optimization of the switching quad DC bias for noise and linearity. According to the relative value of the gate voltage $V_g$ to the source voltage $V_s$ of the switches, different working modes can be defined. If $V_g < V_s + V_{th}$, the mixer works at OFF-overlap; if $V_g > V_s + V_{th}$, the mixer works at ON-overlap. Overlap refers to a window in time and around the LO zero crossing where two transistors with a common output terminal are at the same state[9].

During the ON-overlap period, there will be more output noise generated by the TIA due to the on-resistance of the switches[10]. However, operating the mixer with too much OFF-overlap is also not acceptable because the LO signal cannot fully turn on the switches and the gain decreases. In addition, white noise would also rise correspondingly[9]. As a result, gate voltage of the switches is set to 1.1 V to make the mixer work in a little OFF-overlap state.

### 3.2.3. Linearity

As the TIA creates the virtual ground across the whole channel band, current mode passive mixer has small voltage swing across the switches, which leads to a significantly good linearity. To achieve high linearity, the switch size should be large enough to have a low on-resistance. Furthermore, large switch transistors can improve their matching, which lead to high IIP2. However, a large device would introduce more parasitic capacitance, which leads to a large TIA noise contribution according to Eq. (8). There is therefore a tradeoff between linearity and noise. A 50/0.13 $\mu$m RF transistor size is numerically optimized to obtain both good noise and linearity performances.

To achieve high linearity the mixer should have a low load

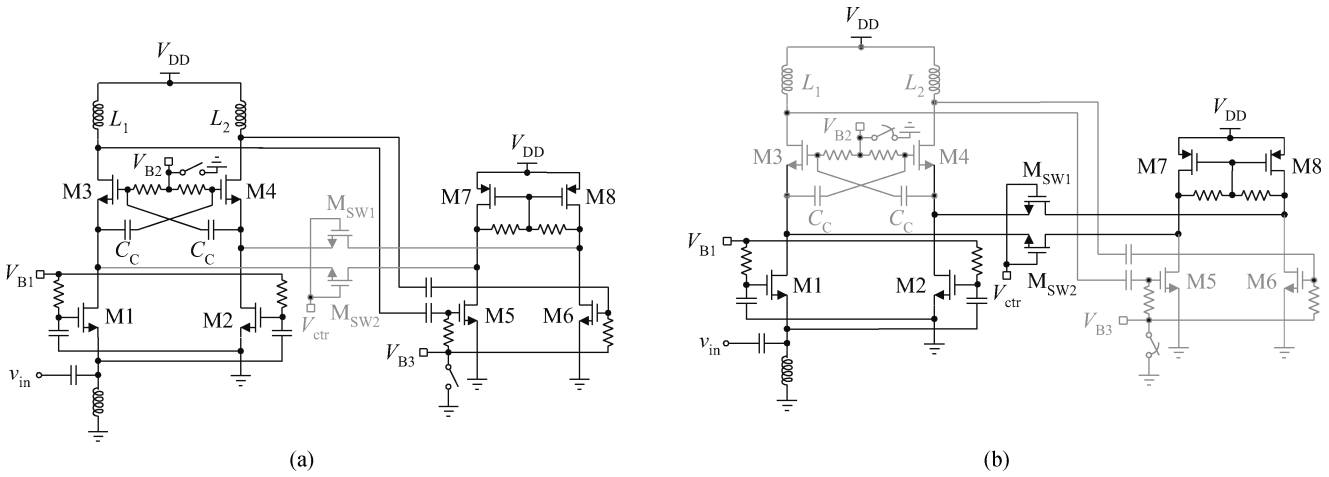


Fig. 7. Gain control configuration. (a) High gain mode. (b) Low gain mode.

resistance, which reduces the voltage swing at the source and drain of the switching quad. However, the conversion gain is proportional to the load resistance. As a result, a compromise between linearity and gain should be made when designing the load resistance. In this design, it is set to 1 kΩ as a tradeoff.

Furthermore, a 3 pF capacitor is inserted between the drain node of the switch and ground to filter out the high frequency interferential signal. The IF signal experiences a first-order low-pass filtering, which can attenuate the blocking signals. This lowers the linearity requirements on the receiver analog baseband. A self-biased LO buffer is used, as shown in Fig. 2, which can maintain a 50% duty cycle and improve the LO edge transition.

### 3.3. Gain control scheme

To improve the dynamic range of the receiver, the RF front-end should provide different gain modes to meet the requirements of high and low level signals. This design provides high and low gain modes. A current mode switching scheme is adopted to achieve the low gain mode with excellent linearity[6].

High gain mode and low gain mode configurations are demonstrated respectively in Fig. 7 as a pair of switch transistors is inserted between LNA output and mixer input terminal. When the switch transistors are turned off as in Fig. 7(a), the front-end performs as a cascaded two-stage amplifier, giving a transconductance of $g_{m1}R_o g_{m5}$ where $R_o$ is the equivalent output resistance of the balun LNA. When the switch transistors are turned on as in Fig. 7(b), then the transistors M3–M6 are all off. Therefore, the front-end is configured as one single-stage cascode amplifier, providing a transconductance of $g_{m1}$. As a result, the gain step of $g_{m5}R_o$ is achieved. In this design 20 dB gain attenuation is obtained.

This current mode switching scheme helps achieve high linearity by avoiding inter-stage intermodulation since the two cascaded amplifiers are reduced to a single-stage amplifier at low gain mode. As the switch transistor has low on-resistance, the signal current flowing through the switch transistor generates small voltage swing, which leads to negligible linearity degradation. A more attractive advantage is that it can save power consumption when working at low gain mode and measurement result also shows that 8.3 mW can be saved.

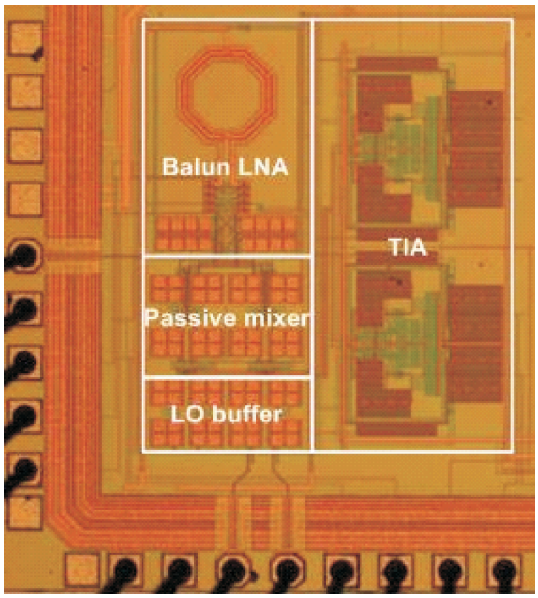


Fig. 8. Die photograph of the RF front-end.

## 4. Experimental results

The receiver RF front-end chip was implemented on a 0.13-$\mu$m CMOS process and occupies an active chip area of 1.2 mm$^2$. The photograph of the die is shown in Fig. 8. It was tested on a FR4 printed circuit board. Special care has been taken to design the PCB because of the high frequency signal. The whole I/Q circuits including the LO buffer consume 28.4 mA from a 1.2 V supply at high gain mode, while dissipating 21.5 mA at low gain mode.

Figure 9 shows the $S_{11}$ characteristic at different gain modes; for the two modes of operation $S_{11}$ is better than –10 dB from 4.8 to 5.2 GHz. Sweeping the LO frequency across 4.9–5.1 GHz, the conversion gain is 35 dB at high gain mode and 13 dB at low gain mode. It is almost flat over 200 MHz band shown in Fig. 9.

Figure 10 shows the simulated and measured double side

Table 2. Performance summary and comparison.

| Parameter | This work | | JSSC 09[4] | JSSC 07[2] | JSSC 05[1] | Spec. |
|---|---|---|---|---|---|---|
| | High gain | Low gain | High gain | High gain | High gain | |
| Frequency (GHz) | 5 | 5 | 5 | 5 | 5 | 5 |
| Balun LNA | Yes | Yes | Yes | NO | NO | — |
| Conversion gain (dB) | 35 | 13 | 68* | 14–94.5* | 70* | 35 |
| DSB noise figure (dB) | 7.2 | 20 | 6.5 | 8 | 6.5 | 9 |
| In-band IIP3 (dBm) | –16.8 | 5.2 | –16 | –14.2 | –25 | -20 |
| $P_{1dB}$ (dBm) | –26 | –6 | ? | –20*** | ? | –24*** |
| $S_{11}$ (dB) | $< -10$ | $< -10$ | –13 | $< -10$ | $< -10$ | $< -10$ |
| Supply (V) | 1.2 | 1.2 | 1.1 | 1 | 1.8 | 1.2 |
| Power (mW) | 34.1 | 25.8 | 89.1–115.5** | 32.3 | 252** | $< 40$ |
| Technology | 0.13-$\mu$m CMOS | 0.13-$\mu$m CMOS | 45 nm CMOS | 0.18-$\mu$m CMOS | 0.18-$\mu$m CMOS | — |

*Receiver. ** Receiver & LO. ***Low gain mode.

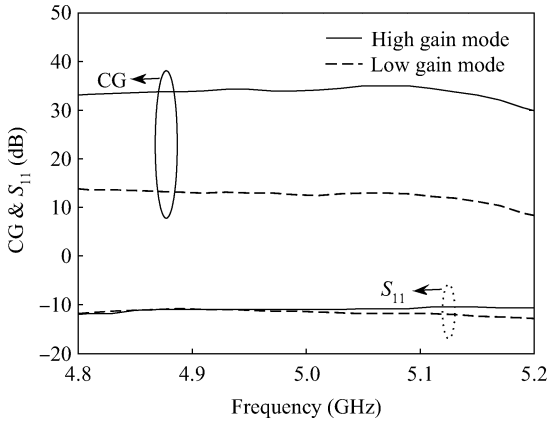


Fig. 9. Measured conversion gain and $S_{11}$ at different gain modes.

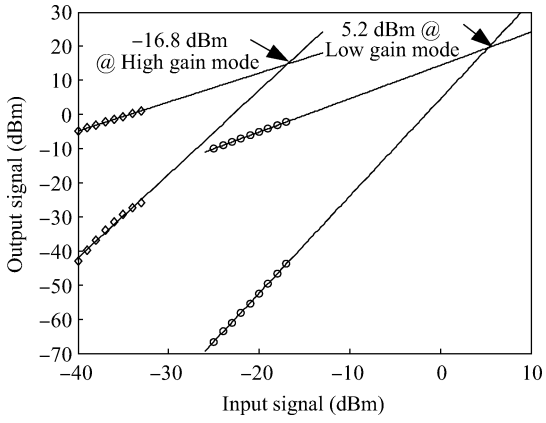


Fig. 11. Measured IIP3 at different gain modes.

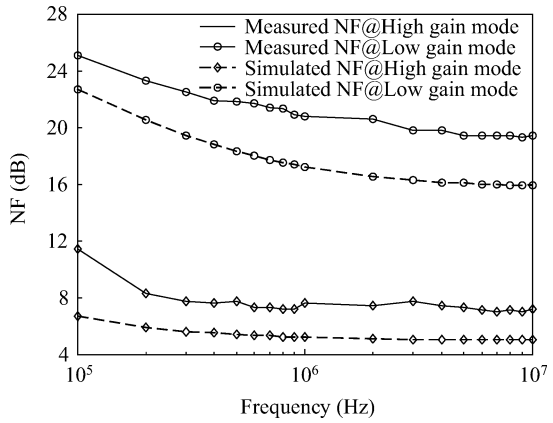


Fig. 10. Measured versus simulated noise figure.

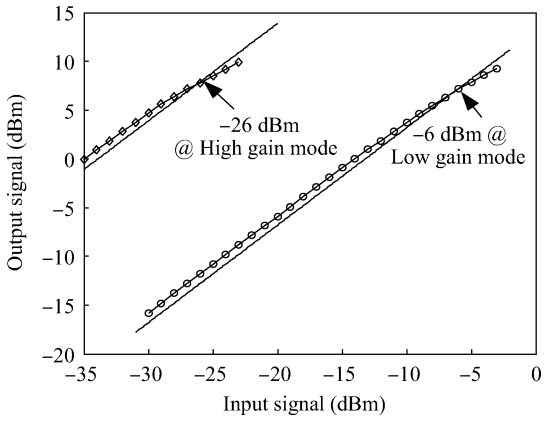


Fig. 12. Measured $P_{1dB}$ at different gain modes.

band (DSB) noise figure versus output frequency at high and low gain modes measured by the Agilent E4440a spectrum analyzer. The NFs are 7.2 dB and 20 dB, respectively, in the center of the band and $1/f$ noise corner is below 200 kHz. At high gain mode, the measured NF worsens around 2 dB because of the gain dropping as compared with the simulation.

The third-order intercept point is measured with a two-tone test at 5.058 GHz and 5.060 GHz. At high and low gain modes, IIP3 achieve –16.8 dBm and 5.2 dBm respectively as shown in Fig. 11. This validates that good linearity can be obtained using the current mode switching scheme to get the low gain. Figure 12 shows the measured 1 dB compression point ($P_{1dB}$) at high and low gain mode. They are –26 dBm and –6 dBm respectively. From the comparison below, we can see that –6 dBm $P_{1dB}$ at low gain mode is rather a good result.

Table 2 shows the performance summary of this work. The achieved results meet the specification requirement very well and noise and linearity performance are especially superior to the specification. In addition, compared with recent reported works, the presented RF front-end also obtains a moder-

ate noise performance. As to linearity performance, it is better than Ref. [1] and comparable to Ref. [4] at high gain mode; at low gain mode it exhibits excellent performance because of the current mode switching scheme. The power consumption is relatively low especially working at low gain mode.

In summary, the result demonstrates the effectiveness of the presented front-end architecture and design methodology. This structure can be applied to the broad band receiver which conforms to the same design method.

## 5. Conclusion

This paper presents a low power direct conversion receiver RF front-end working at 4.9–5.1 GHz. This front-end consists of balun LNA and current mode passive mixer. The presented balun LNA, which uses capacitive cross-coupling technique, has a better noise performance than the conventional one without increasing the power consumption. Sizing and biasing optimization methods were presented to design the current mode passive mixer. In addition, low gain mode can save 8.3 mW power consumption by using current mode switching scheme. The front-end chip is fabricated on a 0.13-$\mu$m CMOS process and achieves a 35 dB conversion gain, a noise figure of 7.2 dB, $1/f$ noise corner of below 200 kHz, an in-band IIP3 of –16.8 dBm, while consuming 28.4 mA from a 1.2 V power supply at high gain mode.

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