A 140 mV 0.8 μA CMOS voltage reference based on sub-threshold MOSFETs*

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Abstract: A CMOS voltage reference circuit based on sub-threshold MOSFETs is proposed, which utilizes a temperature-dependent threshold voltage, a peaking current mirror and sub-threshold technology. The reference has been fabricated in an SMIC 0.13 μm CMOS process with only MOS transistors and resistors. The experimental results show a reference voltage variation of 2 mV for a supply voltage ranging from 0.5 to 1.2 V and 0.8 mV for temperatures from −20 to 120 ℃. The proposed circuit generates a reference voltage of 140 mV and consumes a supply current of 0.8 μA at room temperature. The occupied area is only 0.019 mm^2.

Key words: sub-threshold; peaking current mirror; low voltage; low power
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1. Introduction

Low voltage and low power are essential goals for circuits and systems deployed in a pervasive electronics scenario, where a battery can maintain a long lifetime. The voltage reference is a critical block in analog and mix-signal circuits such as voltage regulators and analog/digital converters. Some of the key requirements for an ideal voltage reference are as follows: (1) output voltage is temperature-independent; (2) output voltage is supply-independent; (3) operation over a wide range of supply voltage; (4) output voltage can be easily scaled[1]; and (5) capable of low-voltage low-power operation. The most common references satisfying some of these key parameters are current-mode[2, 3] and voltage-mode[4] bandgap references, which are obtained through exploiting the characteristics of bipolar junction transistors (BJTs). Unfortunately, the major disadvantages of bandgap references are their power dissipation and minimum supply voltage. While in many low-voltage low-power CMOS reference circuits[5−7], bad temperature coefficients (TCs) or line regulation (LNRs) are reported because of: (1) the drawbacks of the first-order temperature compensation; and (2) the limited number of devices cascaded from the supply voltage to the ground.

In this paper, we describe a new and simple topology that provides a low-power and low-voltage CMOS voltage reference with good line regulation and temperature stability. A sub-threshold operation technique is used to lower the power consumption of the circuit. Line regulation of the voltage reference has been improved greatly because of the negative feedback loops existing in the proposed circuit. The curvature-corrected component of the circuit utilizes cascade-connected NMOS transistors, which operate in the sub-threshold region at high temperature. Therefore, a lower temperature drift of output voltage is achieved. The novel reference was implemented in 0.13 μm CMOS technology and verified by experimental results. More details of the proposed voltage reference circuit are discussed in the following sections.

2. Proposed circuit

In low-voltage low-power CMOS voltage reference design, MOS transistors are biased in the weak inversion region to replace the BJTs in circuits. Similar to the temperature dependence of emitter–base voltage in BJT, the gate-source voltage of an MOSFET represents the simplest implementation in CMOS technology of a conversely proportional to absolute temperature (CTAT) voltage. Considering the sub-threshold operation of a p-MOSFET with a PTAT drain current, the temperature dependence of the gate–source voltage of the n-MOSFET can be expressed as[6, 9]

$$V_{\mathrm{GS6}}(T) = A_0 + A_1 T + A_2 T \ln T, \tag{1}$$

where the constants A_0, A_1 and A_2 are dependent on the process technology. As can be seen from Eq. (1), the first term A_0 is a constant, the second one is a linear term and the last term models the nonlinearity of the temperature-dependent factor of gate–source voltage. Normally, first-order compensation involves the cancellation of the second T term while high-order temperature compensation covers the cancellation of the logarithmic T term. In our proposed circuit, the cascade sub-threshold MOSFET can achieve the function of high-order temperature compensation.

The proposed reference circuit is shown in Fig. 1. It is composed of four main sub-circuits. The first part is the peaking current mirror circuit, which is made up of transistors M4–M6 and resistor R_1. The second part is the negative feedback loop consisting of transistors M1–M3, M7 and resistors R_2–R_3. The third part is the curvature-compensated sub-circuit, which is composed of MTC1 and MTC2. The fourth part is the start-up circuit. The elements M4, M5 and R_1 constitute the peaking current source, which is a PTAT component. M3 and M6 are biased as current mirrors by the voltage drop across R_2 plus R_3, the voltage V_{GS3} and V_{GS6} is therefore a CTAT component. M8 mirrors the PTAT current generated in the peaking current source and injects it into the downside resistors R_4 and R_3.

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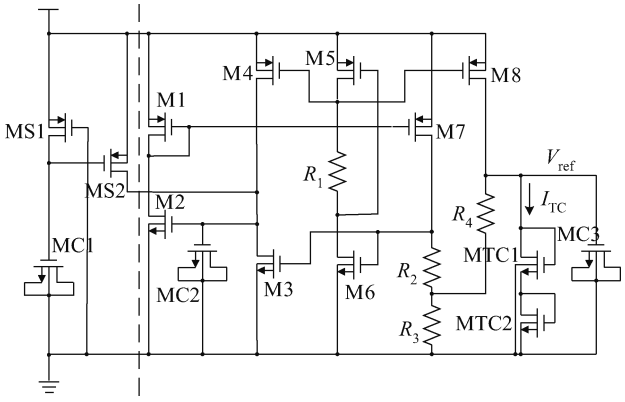

Fig. 1. Proposed CMOS voltage reference with a start-up circuit.

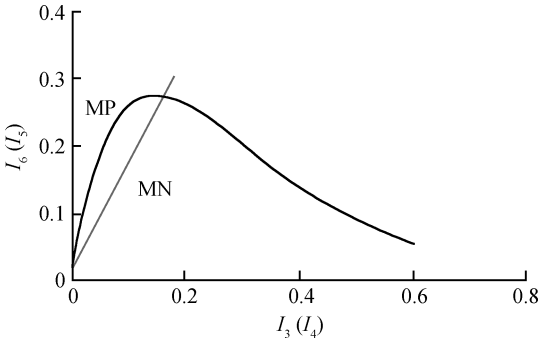

Fig. 2. Current relationship of M3–M6.

Elaborating the ratios of resistors and transistors we obtain the voltage V_{ref} as the sum of a PTAT component and a V_{GS}-based component. Design considerations of the circuit are illustrated in following section.

3. Design consideration

3.1. CTAT source

The CTAT source is composed of M1–M3, M7 and resistors R_2–R_3, M3 is biased in sub-threshold region. It generates a supply-independent voltage V_{GS3}. The circuit operates as following: M1 and M7 form current mirrors, and their drain current are according to the ratio between them. M3, M2, M1 and M7 form a negative feedback path, and this forces current through R_2 and R_3 to be constant, namely supply-independent. For example, if the current of R_2 and R_3 increase because of supply voltage variation, the negative feedback opposes this change to keep the current constant, V_{GS3} is thus supply-independent. The voltage across R_3 is

$$V_{R3}(T) = V_{GS3}(T)\frac{R_3}{R_3 + R_2}. \tag{2}$$

The transistor MC2 as a MOS capacitor C_C compensates the negative feedback loop. MC2 imposes a dominant pole at the gate of M2. It also sets the gain-bandwidth product of the feedback loop, which results in

$$w_{GBW} = \frac{g_{m3}g_{m4}(R_3 + R_4)}{C_C}\frac{(W/L)_7}{(W/L)_1}. \tag{3}$$

Obviously, a higher gain of the feedback loop means a more accurate CTAT current, but a bigger occupation area of the compensation capacitor as well. Consequently, proper values of the gain and capacitor must be set in order to maintain ω_{GBW} well below the value of the other poles which exist in the circuit.

3.2. PTAT source

For a PMOS transistor operating in a sub-threshold region, its drain current is given by[7]

$$I_D = I_S\frac{W}{L}\exp\frac{V_{SG} - |V_{thp}|}{nV_T}\left[1 - \exp\left(-\frac{V_{SD}}{V_T}\right)\right], \tag{4}$$

where V_T is the thermal voltage, n is the sub-threshold slope parameter, V_{thp} is the threshold voltage, and I_S is proportional to the square of thermal voltage V_T and the carrier electrical mobility μ. Assuming that the channel length is long enough and $V_{SD} > 4V_T$, $V_{thp4} = V_{thp5}$, we can extract the expression of the relation between two currents of M4 and M5:

$$I_{D4} = I_{D5}\frac{(W/L)_4}{(W/L)_5}\exp\frac{V_{SG4} - V_{SG5}}{nV_T}. \tag{5}$$

For M4 and M5 operating in a sub-threshold region, the voltage difference between their source-gate is a PTAT voltage, which results in:

$$\Delta V_{SG} = V_{SG5} - V_{SG4} = I_{D5}R_1. \tag{6}$$

Substituting Eq. (6) into Eq. (5), we get

$$I_{D4} = I_{D5}\frac{(W/L)_4}{(W/L)_5}\exp\left(\frac{-I_{D5}R_1}{nV_T}\right). \tag{7}$$

The peaking current mirror circuit is designed such that I_{D4} is at its peaking value. It can be achieved by zeroing the derivative of I_{D4} with respect to I_{D5} using Eq. (7), yielding the design condition to maintain the current peaking[10], it yields

$$I_{D5}R_1 = nV_T. \tag{8}$$

Therefore, we obtain the PTAT current

$$I_{D5} = nV_T/R_1. \tag{9}$$

If the condition is satisfied, then the drain currents of M4 and M5, via Eq. (7), are related by

$$I_{D4} = I_{D5}\frac{(W/L)_4}{(W/L)_5}e^{-1}. \tag{10}$$

By setting the values of R_1 and the aspect ratios of M3–M6, we obtain the needed operation of the peaking current mirror circuit. For example, if we set $R_1 = 200$ kΩ, $(W/L)_5/(W/L)_4 = 1/e$, then adjusting the ratio of M4 and M5 will make I_{D4} and I_{D5} change. The drain current relationship between M3–M6 is illustrated in Fig. 2.

Normally, in order to improve the power supply rejection ratio (PSRR) of the PTAT source, we set the working point greater than peaking point, so that the upper MOS peaking current mirror (M4, M5) and the lower linear current mirror (M3, M6) form a negative current feedback loop, together with other

components they can form a negative feedback loop to maintain stability and improve the PSRR performance of the circuit. From the small signal model of the proposed circuit, we can get that

$$\frac{\partial V_{\rm ref}}{\partial V_{\rm in}} = \frac{R_3+R_4}{g_{\rm m3}(R_3+R_2)} \times \left\{ \frac{1}{r_{\rm o4}} + \frac{g_{\rm m4}(1-g_{\rm m5}R_1)[r_{\rm o8}-(R_3+R_2)g_{\rm m6}r_{\rm o6}]}{(R_3+R_2)g_{\rm m6}r_{\rm o6}g_{\rm m8}r_{\rm o8}} - \left(\frac{1}{r_{\rm o3}}+\frac{1}{r_{\rm o4}}\right)\frac{g_{\rm m8}}{g_{\rm m7}}\left[\frac{2}{g_{\rm m8}r_{\rm o8}} - \frac{2}{(R_3+R_2)g_{\rm m6}r_{\rm o6}r_{\rm o8}} - \frac{R_3+R_2}{r_{\rm o8}} - \frac{1}{g_{\rm m1}r_{\rm o2}}\right]\right\}. \tag{11}$$

If we adopt the right value of the correlative parameters in Eq. (11), we can get the high PSRR of the proposed circuit.

3.3. Curvature compensation

From above discussion, we obtain the PTAT and CTAT sources. The output stage, which consists of M8 and R_4, completes temperature compensation. M8 mirrors the PTAT current generated in the PTAT source, which results in

$$I_{\rm D8} = I_{\rm D4}\frac{(W/L)_8}{(W/L)_4} = \frac{nV_{\rm T}}{R_1}\frac{(W/L)_8}{(W/L)_4}e^{-1}. \tag{12}$$

Therefore, the output voltage can be expressed as

$$V_{\rm ref} = V_{\rm GS6}\frac{R_3}{R_2+R_3} + (R_3+R_4)I_{\rm D8} = V_{\rm GS6}\frac{R_3}{R_2+R_3} + nV_{\rm T}\frac{R_3+R_4}{R_1}\frac{(W/L)_8}{(W/L)_4}e^{-1}. \tag{13}$$

Substituting Eq. (1) into Eq. (13), and then the new equation with respect to temperature to get the following equation:

$$\frac{\partial V_{\rm ref}}{\partial T} = \frac{R_3}{R_2+R_3}\frac{\partial V_{\rm GS6}}{\partial T} + n\frac{R_2+R_3}{R_1}\frac{(W/L)_8}{(W/L)_4}e^{-1}\frac{\partial V_{\rm T}}{\partial T} = \frac{R_3}{R_2+R_3}(A_1+A_2+A_2\ln T) + \frac{nk}{q}\frac{R_3+R_4}{R_1}\frac{(W/L)_8}{(W/L)_4}e^{-1}, \tag{14}$$

where k is the Boltzmann constant, q is the charge of the electron. From Eq. (14), by setting the right values of the resistance and aspect ratio, we can get the zero temperature coefficient of the reference output value at various temperatures. However, this method only compensates the first-order temperature, while the logarithmic T term cannot compensate by this simple method. Therefore, we introduce cascade sub-threshold MOS transistors, as shown in the Fig. 1. MTC1 and MTC2 compose the cascade MOS transistors, which operate in the sub-threshold region.When the temperature rises, the threshold voltage will be reduced. Then the current drained by the cascade MOS transistors are proportional to the absolute temperature because of the threshold voltages of the MOS transistors. In fact, the quantity of the current by the MTC1 and MTC2 is so small that it can be ignored at lower temperatures[9]. Thus, when we add these cascade MOS transistors into the circuit, the PTAT current will rise slowly as the temperature increases, as shown in Fig. 3. Therefore it will generate the function of high-order temperature coefficient (TC) compensation. Figure 4 shows the contrast of the reference voltage $V_{\rm ref}$ without/with $I_{\rm TC}$ compensation.

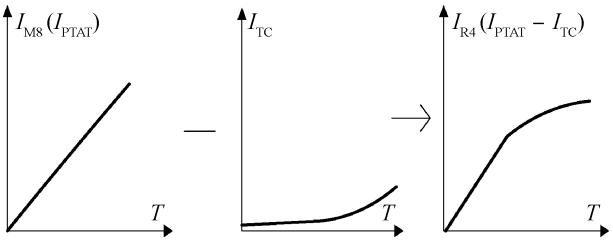

Fig. 3. The affection of $I_{\rm TC}$ to the $I_{\rm PTAT}$.

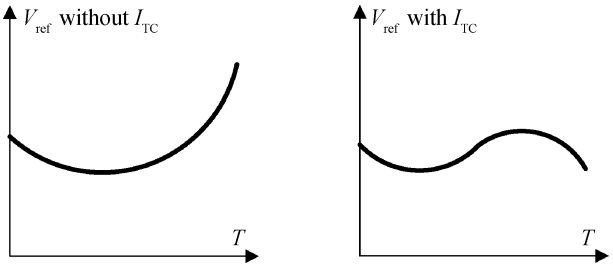

Fig. 4. Contrast of reference voltage $V_{\rm ref}$ without/with $I_{\rm TC}$ compensation.

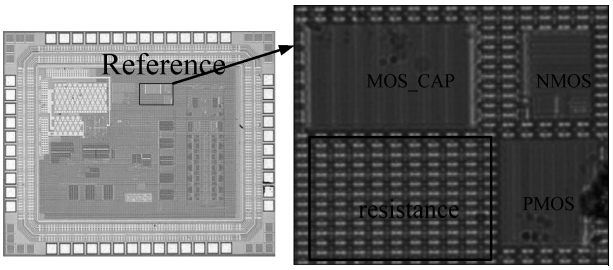

Fig. 5. Micrograph of the chip contains the proposed circuit.

4. Experimental results

The proposed circuit shown in Fig. 1 has been designed and implemented in a CMOS SMIC 0.13 μm process and the main process parameters are $V_{\rm THN} = 310$ mV and $V_{\rm THP} = -279$ mV. The circuit is designed to provide a lower voltage for low voltage application.

Table 1 summarizes the parameters of the components in the proposed circuit. Figure 5 shows the micrograph of the chip containing the proposed circuit. The area of the proposed circuit is only 0.019 mm^2. Figure 6 shows the reference voltage as a function of supply voltage from 0 to 1.2 V. The voltage reference circuit starts to work when the supply voltage reaches almost 0.5 V. An almost constant reference voltage

Table 1. Resistance values and transistor dimensions in the proposed circuit.

Component	Parameter	Component	Parameter
M1	$W = 4\ \mu$m, $L = 10\ \mu$m	MC1	$W = 10\ \mu$m, $L = 10\ \mu$m
M2	$W = 2\ \mu$m, $L = 10\ \mu$m	MC2	$W = 100\ \mu$m, $L = 10\ \mu$m
M3	$W = 60\ \mu$m, $L = 4\ \mu$m	MC3	$W = 250\ \mu$m, $L = 10\ \mu$m
M4	$W = 100\ \mu$m, $L = 4\ \mu$m	MS1	$W = 0.5\ \mu$m, $L = 10\ \mu$m
M5	$W = 50\ \mu$m, $L = 4\ \mu$m	MS2	$W = 4\ \mu$m, $L = 2\ \mu$m
M6	$W = 100\ \mu$m, $L = 4\ \mu$m	R_1	197 kΩ
M7	$W = 4\ \mu$m, $L = 10\ \mu$m	R_2	616 kΩ
M8	$W = 185\ \mu$m, $L = 4\ \mu$m	R_3	246 kΩ
MTC1, MTC2	$W = 10\ \mu$m, $L = 1.2\ \mu$m	R_4	246 kΩ

Table 2. Resistance values and transistor dimensions in the proposed circuit.

Reference	This work	Ref. [6]	Ref. [10]	Ref. [12]	Ref. [13]
Process	0.13 μm CMOS	0.35 μm CMOS	0.6 μm CMOS	0.35 μm CMOS	0.18 μm CMOS
Temperature range (℃)	−20 to 120	0–70	0–100	−20 to 80	−23 to 77
Min. supply voltage (V)	0.5	1.4	1.4	0.95	1
Reference voltage (mV)	140	579	309	741	29
Max. supply current (μA)	0.8	2.3	9.7	N/A	1.48
Temperature coefficient (ppm/℃)	40.8	62	36.9	39.3	72.6
Line regulation (mV/V)	2.8	3.9	0.25	25	0.0204
Chip area (mm^2)	0.019	0.126	0.055	N/A	N/A

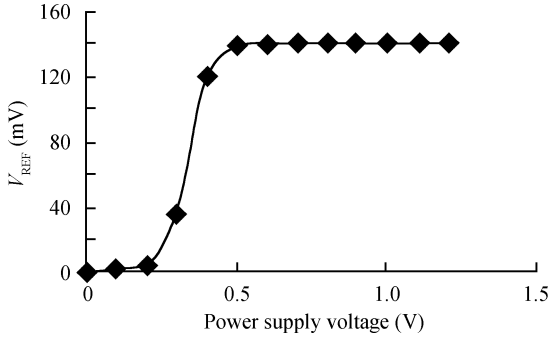

Fig. 6. Measured reference voltage as a function of the power supply voltage.

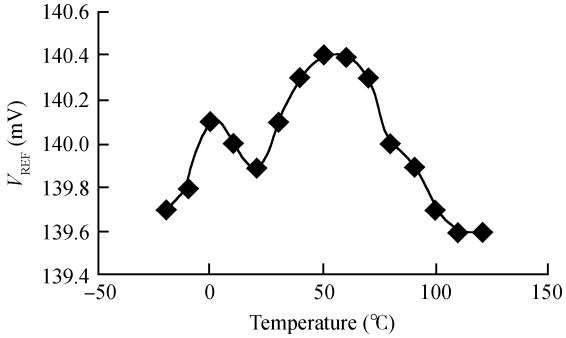

Fig. 7. Measured reference voltage as a function of the temperature.

can be obtained when the supply voltage is more than 0.5 V; the variation of reference voltage is about 2 mV at room temperature. Figure 7 shows the reference voltage as a function of temperature from −20 to 120 ℃, the variation of reference voltage is about 0.8 mV. The temperature coefficient of the output voltage is about 40.8 ppm/℃. Table 2 summarizes and compares the experimental results of the proposed circuit with other published voltage reference circuits using sub-threshold MOSFETs. From the results, we can know that the proposed circuit has the smallest output reference voltage, supply current and chip area. Moreover, the other results, such as temperature coefficient and line regulation, are also comparable with published voltage reference circuits.

5. Conclusion

A CMOS voltage reference circuit based on sub-threshold MOSFETs has been described in this paper. Unlike conventional voltage reference designs, the proposed circuit has no BJT, only MOSFETs and resistors. The peaking current mirror circuit and cascade sub-threshold MOS transistors are used in the proposed circuit to achieve good performance. The test chip has been fabricated using a standard 0.13 μm CMOS process and experimental results are presented for theoretical analysis. The results show that the proposed voltage reference has a low supply current 0.8 μA, low supply voltage 0.5 V, small chip area 0.019 mm^2 and low-temperature coefficient 40.8 ppm/℃. Therefore it is well suited for on-chip reference generation in both analog and digital systems.

References

[1] Sanborn K, Ma D, Ivanov V. A sub-1-V low-noise bandgap voltage reference. IEEE J Solid-State Circuits, 2007, 42(11): 2466

[2] Shiga B H, Umezawa H, Miyaba A, et al. A CMOS bandgap reference circuit with sub-1-V operation. IEEE J Solid-State Circuits, 1999, 34(5): 670

[3] Malcovati P, Maloberti F, Fiocchi C, et al. Curvature-compensated BiCMOS bandgap with 1-V supply voltage. IEEE

J Solid-State Circuits, 2001, 36(7): 1076
[4] Leung K N, Mok P K T, Leung C Y. A 2-V 23-μA 5.3-ppm/℃ curvature-compensated CMOS bandgap voltage reference. IEEE J Solid-State Circuits, 2003, 38(3): 561
[5] Giustolisi G, Palumbo G, Criscione M, et al. A low-voltage low-power voltage reference based on subthreshold MOSFETs. IEEE J Solid-State Circuits, 2003, 38(1): 151
[6] Cheng M H, Wu Z W. Low-power low-voltage reference using peaking current mirror circuit. Electron Lett, 2005, 41(10): 572
[7] De Carvalho Ferreira L H, Pimenta T C, Moreno R L. An ultra low-voltage ultra low-power CMOS threshold voltage reference. IEICE Trans Electron, 2007, E90-C(10): 2044
[8] Li Y J, Xia X J, Guan J W. A simple subthreshold CMOS voltage reference with curvature compensation. PrimeAsia IEEE Microelectronics & Electronics, 2009: 364
[9] Huang H Y, Wang R J, Hsu S C. Piecewise linear curvature-compensated CMOS bandgap reference. IEEE 15th ICECS, 2008: 308
[10] Leung K N, Mok P K T. A CMOS voltage reference based on weighted ΔV_{GS} for CMOS low-dropout linear regulators. IEEE J Solid-State Circuits, 2003, 38(1): 146
[11] Kerns D V. Optimization of the peaking current source. IEEE J Solid-State Circuits, 1986, 21(4): 587
[12] Ferreira L H C, Pimenta T C, Moren R L. A CMOS threshold voltage reference source for very-low-voltage applications. Microelectron J, 2008, 39(12): 1867
[13] Shu J, Min C. A low supply-dependence fully-MOSFET voltage reference for low-voltage and low-power. APCCAS, 2008: 662