

A low reference spur quadrature phase-locked loop for UWB systems*

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Abstract: This paper presents a low phase noise and low reference spur quadrature phase-locked loop (QPLL) circuit that is implemented as a part of a frequency synthesizer for China UWB standard systems. A glitch-suppressed charge pump (CP) is employed for reference spur reduction. By forcing the phase frequency detector and CP to operate in a linear region of its transfer function, the linearity of the QPLL is further improved. With the proposed series-quadrature voltage-controlled oscillator, the phase accuracy of the QPLL is guaranteed. The circuit is fabricated in the TSMC 0.13 μm CMOS process and operated at 1.2-V supply voltage. The QPLL measures a phase noise of -95 dBc/Hz at 100-kHz offset and a reference spur of -71 dBc. The fully-integrated QPLL dissipates a current of 13 mA.

Key words: QPLL; charge pump; UWB; glitch; S-QVCO

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1. Introduction

The OFDM UWB system is attractive due to its high data-rate transmission in short-range wireless communication. The frequency band from 6.2 to 9.4 GHz is available for China UWB standard applications, and is divided into 12 sub-bands. Figure 1 shows the block diagram of the proposed China UWB standard synthesizer. It consists of divide-by-2 stages, single-sideband (SSB) mixers and multiplexers. The use of an SSB mixer enables the QPLL to generate quadrature 8.448 GHz and quadrature intermediate frequency.

The UWB system does not require a QPLL with narrow channel spacing. Therefore, the QPLL is implemented using a CP-based integer- N architecture as shown in Fig. 1. The QPLL consists of a PFD, a CP, a loop filter (LF), frequency dividers and a QVCO. However, spurs are always generated by timing or voltage level mismatch between UP and DN current pulses from the CP. Timing mismatch can be reduced by using some clock buffers. Current-level mismatch is categorized into two types: static and dynamic mismatch. Static offsets can be avoided by using a cascade topology^[1,2] to reduce the current mismatch by increasing its output resistance. In many cases, the static sources of spur generation, which are predictable and invariant in time, can be easily suppressed. But dynamic spur sources, such as glitches on the loop filter, are time-varying and difficult to fully suppress. The glitch of the CP leads to high reference spurs. Furthermore, dithering of the CP output current will induce variation of the QPLL loop bandwidth. Such a large variation may bring the QPLL from a stable to an unstable region.

In order to reduce dynamic offsets, a novel CP circuit with a glitch-suppression technique is employed. In this way, a glitch-free CP with perfect current matching characteristic is

achieved. Aiming for China UWB standard transceivers, a low phase noise and low reference spur QPLL with this CP is implemented.

2. Architecture and design considerations

In the proposed QPLL clock generator, phase noise, reference spurs and phase accuracy are the main concerns. Proper selection of the LF bandwidth is critical for minimum jitter generation and transfer. The loop bandwidth must be set high enough to suppress close-in QVCO phase noise and low enough to reject unwanted jitter in the reference clock source. A narrowband integer- N QPLL is employed because low phase noise at an offset above a few hundred kHz and low reference spur are desirable. The overall integrated phase noise (IPN) from 0 Hz up to infinity is defined by the UWB proposal and it can be approximately calculated by

$$\begin{aligned} \text{IPN} &= \frac{360}{2\pi} \\ &\times \sqrt{2 \int_0^{f_c} 10^{k/10} df + 2 \int_{f_c}^{\infty} 10^{k/10} \times 10^{-20 \lg(f/f_c)/10} df} \\ &= \frac{180}{\pi} 10^{k/20} \sqrt{2f_c}, \end{aligned} \quad (1)$$

where f_c is the loop bandwidth (Hz) and k is the in-band phase noise density (dBc/Hz). To achieve integrated phase noise below -35° , in-band phase noise should be lower than -85.07 dBc/Hz for a loop bandwidth of 600 kHz, since the reference clock frequency is 48 MHz. According to the above analysis, the loop bandwidth is set to 600 kHz, which is smaller than

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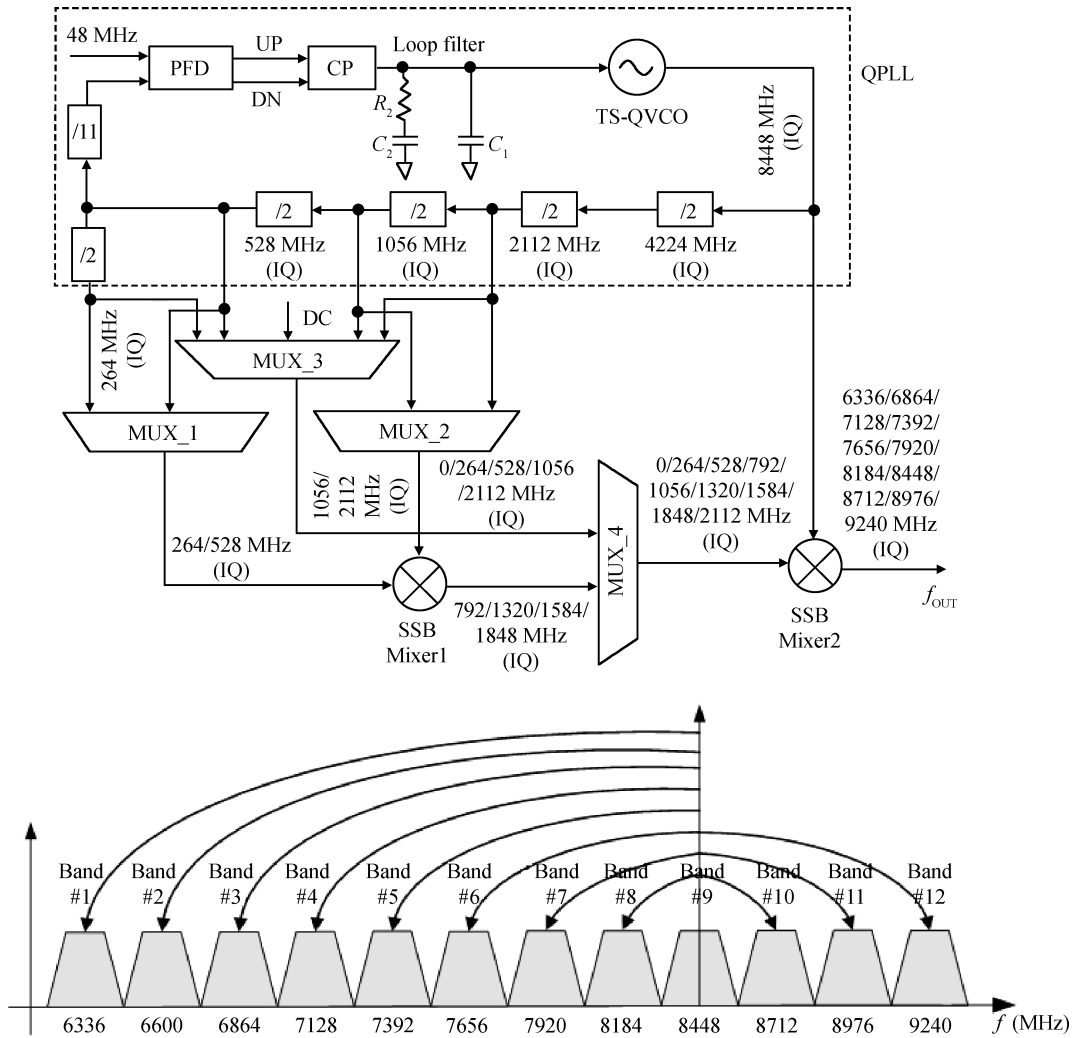


Fig. 1. Block diagram of the proposed UWB frequency synthesizer.

one-tenth of the reference frequency to guarantee loop stability and optimize the overall IPN. The phase margin is set to 62° for fast settling.

In addition to the loop noise, when the current mismatch exists in the CP, phase offset occurs at the output of the QPLL. The amount of the phase offset is expressed by

$$\Phi_e = 2\pi \frac{\Delta t_{on}}{T_{ref}} \frac{\Delta_i}{I_{CP}}, \quad (2)$$

where Φ_e , Δt_{on} , T_{ref} , I_{CP} , Δ_i are the phase offset, the turn-on time of the PFD, the reference clock period, the charge pump current and the current mismatch of the charge pump, respectively^[2]. The amount of the reference spur in the third order QPLL is given by

$$P_r = 20 \lg \frac{\sqrt{2}(I_{CP}R/2\pi)\Phi_e K_{VCO}}{2f_{ref}} - 20 \lg \frac{f_{ref}}{f_{pl}}, \quad (3)$$

where R is the resistor value in the loop filter, K_{VCO} is the VCO gain, f_{ref} is the reference frequency of the PFD, and f_{pl} is the frequency of the pole in the loop filter. Therefore, to reduce reference spurs, the turn-on time of the PFD should be minimized. The matching of current sources in the CP is critical to minimize spurious tones resulting from the ripple on the

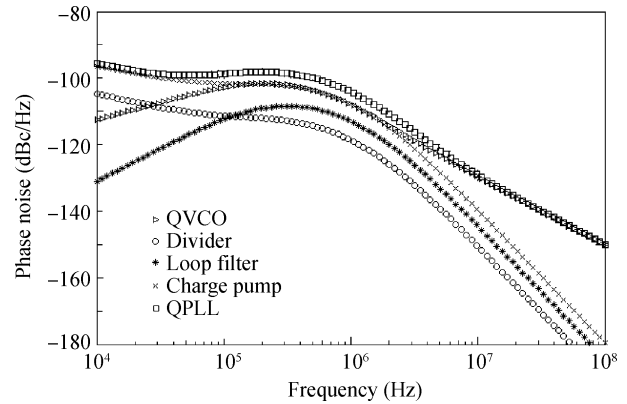


Fig. 2. Simulated phase noise of the QPLL.

QVCO control line. In addition, the gain of the QVCO has to be minimized. The minimum value is required to cover the process variation. The determined value is 120 MHz/V. Finally, the loop noise is simulated as shown in Fig. 2.

Since the final output phase accuracy of the SSB mixer largely depends on the phase accuracy of the input signals, a top-series QVCO is adopted to minimize the phase mismatch

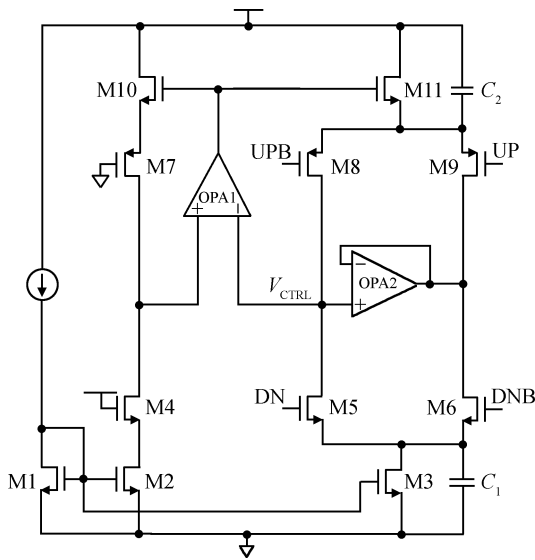


Fig. 3. Schematic of the conventional CP.

of the LO signal. The detailed circuit designs will be described in the following section.

3. Building blocks

3.1. Charge pump

A high performance CP is a key block in the QPLL design. The output current of the CP determines the output voltage of the LF, which tunes the QVCO to produce the desired LO signal. Any mismatch between the charging and discharging current induces steady-state and dynamic offset. Not only does steady-state offset cause the output reference spur to deteriorate, but dynamic mismatch, i.e. glitch, in the output current increases the level of reference spurs in the QPLL. This section first focuses on the suppression of dynamic offset. Steady-state offset will be discussed later.

For an ideal CP, when a square-wave UP/DN signal is applied, the output current should be a square waveform without any glitches. However, in the actual implementation of a CP, the output current pulse has glitches which are produced via two mechanisms. The first type of glitch is caused by the speed limitation of the common source node of the differential pairs. For example, during the switching period, there is a voltage difference due to parasitic capacitance at the common source node. The voltage difference leads to a current glitch for the transistor being turned on. The same phenomenon occurs at the UP switch. The second type of glitch is generated by charging or discharging the gate-to-drain capacitance of the output transistors, which directly injects current into the output node. The magnitude of the second glitch can be larger than the output current when the input signal is switching extremely fast. In a conventional CP, two large capacitors C_1 and C_2 are always employed on common source nodes. The capacitors C_1 and C_2 can reduce the speed that common source nodes are changed by the current sources as shown in Fig. 3. However, these extra capacitors have to be large enough to achieve this purpose. A large chip area is consumed. Moreover, these large capacitors can only reject the first type of glitch.

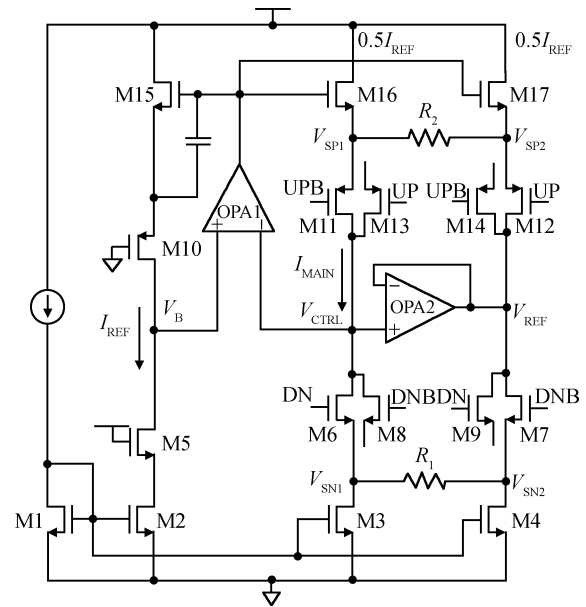


Fig. 4. Schematic of the proposed CP.

To overcome this problem, a glitch-suppressed CP is employed as shown in Fig. 4. Considering the DN current path first, the proposed CP splits the DN current source into two identical ones having half of the original current. The current paths are connected with resistors R_1 . The differential switching pair, M6 and M7, produces the differential-mode voltage outputs of V_{SN1} and V_{SN2} across the resistor. The two outputs have the same pulse shapes as those of DN and DNB, respectively. When M6 is on, V_{SN1} is driven up to $V_{OUT} - V_{DS,M6}$ and V_{SN2} is dropped by $0.5I_{CP}R$ to be $V_{OUT} - V_{DS,M6} - 0.5I_{REF}R$. On the other hand, when M7 is on, V'_{SN2} is driven up to $V_{REF} - V_{DS,M7}$ and V'_{SN1} is lowered to $V_{REF} - V_{DS,M7} - 0.5I_{REF}R$. Therefore, the amplitude of the injected pulse waveform ΔV_{SN1} is given by

$$\begin{aligned} \Delta V_{SN1} &= V_{SN1} - V'_{SN1} \\ &= V_{OUT} - V_{REF} + V_{DS,M7} - V_{DS,M6} + 0.5I_{REF}R. \end{aligned} \tag{4}$$

If V_{OUT} and V_{REF} have negligible offset and $V_{DS,M6}$ and $V_{DS,M7}$ are well matched, the amplitude simply becomes $0.5I_{REF}R$. Therefore, when M6 is turned on, the rising pulse ΔV_{SN1} produced by the voltage difference can block the dynamic voltage drop induced by the DNB current source. In this way, the first type of glitch is eliminated.

The source terminals of M8–M9 and M13–M14 are floating to avoid extra dc current. The size of the transistors M8–M9 and M13–M14 is equal to the size of the transistors M6–M7 and M11–M12. When all eight transistors stay in the saturation region, they have exactly the same gate-to-drain overlap capacitance. Thus, the glitches on the discharging current induced by the switching of DN and DNB cancel each other. The same thing happens for the glitches generated on the charging current provided by PMOS devices. Therefore, the second type of glitch is suppressed. Figure 5 shows the simulation result of the CP output without (grey dashed line) and with (black solid line) glitch-suppression techniques. With the proposed

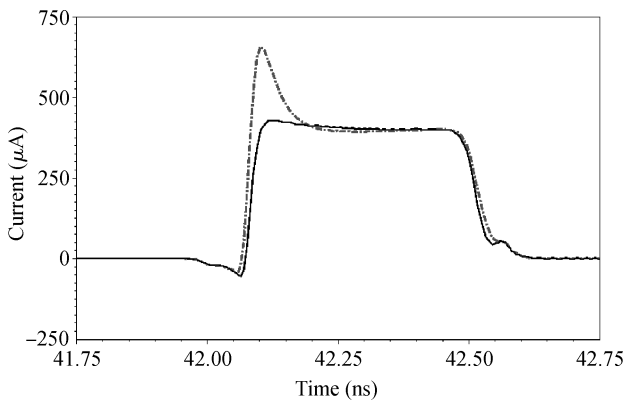


Fig. 5. Comparison of current pulse.

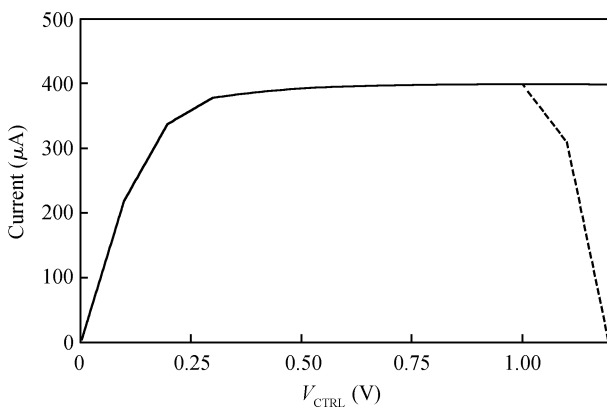


Fig. 6. Simulated output current of the proposed CP.

technique, the glitches are effectively suppressed at the output current.

As for steady-state offset, the proposed CP uses an error amplifier to improve the current matching characteristic. The proposed CP uses the feedback function of the error amplifier, OPA2, to hold the voltages of V_{CTRL} and V_{REF} . As a result, the source nodes of the switching transistors will have the same voltage before and after switching. The charge sharing between them is reduced. The voltage V_B will change with V_{CTRL} by inserting a high-gain error amplifier OPA1. The amplifier forces the charging current to closely follow the discharging current. Meanwhile, the current I_{MAIN} is the same as half of the current I_{REF} . A metal-insulator-metal (MIM) capacitor is added to compensate for the feedback loop. Since the working range of the common-mode inputs have to cover from V_{DD} to V_{SS} for the two amplifiers, two rail-to-rail-input operational amplifiers are implemented. In addition, the OPA2 provides a rail-to-rail output swing. The proposed CP improves the matching characteristics by enhancing the current matching and lessening the charge sharing with two amplifiers.

Figure 6 shows the DC simulation result of the proposed CP. The CP shows the current matching characteristic to be less than 1% of the sourcing/sinking current difference. A perfect current matching characteristic is observed over the CP output voltage range of 0.0–1.0 V.

3.2. PFD

The dead zone of the conventional PFD is avoided by inserting extra delay at the Reset path. Therefore, the maximum operating frequency of the PFD is limited. To overcome this problem, the proposed PFD uses its outputs (UPB/DNB), instead of its inputs, to trigger the reset signal. Figure 7 shows the schematic of the proposed PFD. If the rising edge of REF leads that of the DIV, then UP goes logic high. UP remains high until the rising edge of DIV raises DN to high level. As UPB and DNB go logic low, RST goes to logic high and resets the PFD into the initial state. The PFD is set by the rising edge of the higher-frequency REF waveform and is not cleared until the advent of the lower-frequency DIV. Thus, the sequential order of triggering of UP/DN and Reset removes the dead zone from the PFD.

To circumvent the charge-sharing phenomena caused by the redistribution of parasitic charges, an improved D-flip-flop (DFF) circuit is used^[3]. The gate voltages of the PMOS transistors are interchanged in the same rail of each latch. By turning off \overline{D} first before q switches from high to low, the proposed PFD does not suffer from charge sharing. The PFD is immune to dead-zone and charge-sharing effects and possesses improved frequency/phase sensitivities. To drive the switching transistors of the charge pump, inverting and non-inverting buffers are placed between the charge pump and the PFD. Input inverters are used to convert the input signal into a steep square waveform.

In addition, the reset signal may lead to an uncertain state of the DFF at the instant when the circuit powers on. The uncertainty makes the initial values of UP, DN indistinct. Since the output signals of the PFD are also the input signals of the CP, the uncertain state may result in abnormal operation of the CP, which influences the locking time of the PLL. To eliminate this problem, two small size PMOS transistors are added to work as level recovery circuits to avoid the uncertain state of the PFD.

3.3. Linearity enhancement technique for PFD/CP

In the design of QPLL, the nonlinearity of the QPLL is mainly caused by the PFD/CP non-linear transfer function^[4]. In PFD/CP circuits, non-linearity is mainly attributed to the gain variation near the zero phase error region. Biasing the output of the CP at non-zero phase offset can avoid the dead zone nonlinearity. With sufficient phase offset, the operation region can be shifted to the desired linear part of the transfer curve as shown in Fig. 8. QPLL with phase offset can significantly reduce the nonlinearity and the phase noise contribution of the PFD/CP. However, there is a trade-off between the nonlinearity and noise contribution from the CP. The phase offset should be set high enough to avoid the dead zone. When the phase offset is large, the noise contribution due to CP's on-time increases. Thus, the optimization of phase offset and phase noise has been achieved for this QPLL. In this design, a NMOS transistor biased at a DC voltage is added at the output of the CP to move the PFD/CP operation to a linear region.

3.4. QVCO

The single-sideband (SSB) mixer necessitates the use of

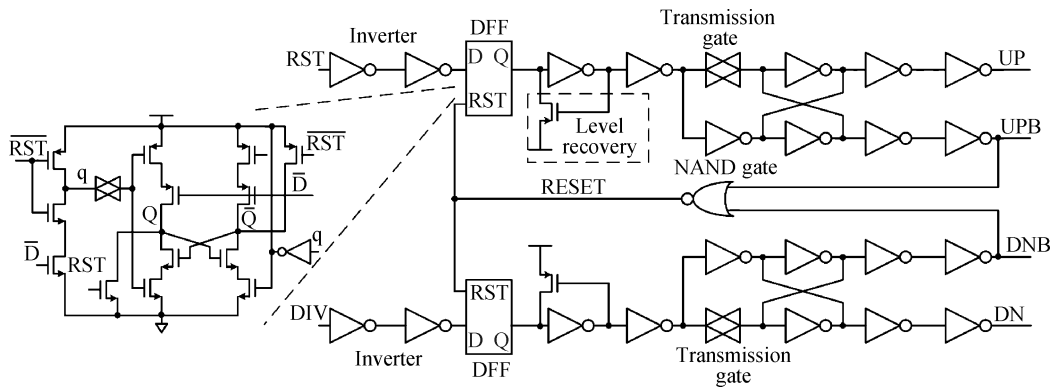
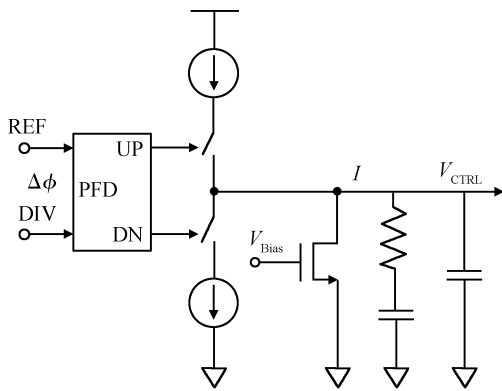
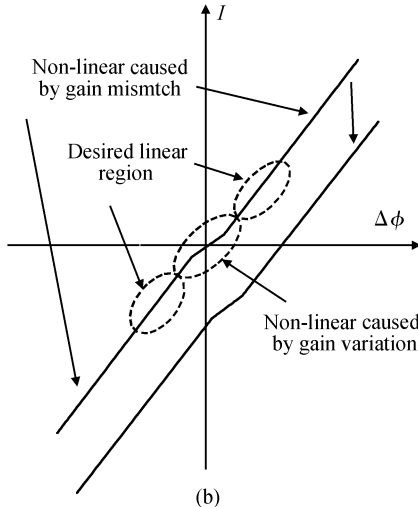


Fig. 7. Schematic of the proposed PFD.



(a)



(b)

Fig. 8. (a) PFD/CP linearized by adding an offset current at CP output. (b) Shift of the PFD/CP transfer curve.

a QVCO. The final output phase accuracy of the SSB mixer largely depends on the phase accuracy of the input signals. Meanwhile, the phase noise of the QVCO heavily influences the overall phase noise of the QPLL and synthesizer, especially the out-of-band phase noise. However, quadrature coupling transistors in parallel-QVCO (P-QVCO) make a large contribution to the phase noise. The cascode structure greatly reduces the noise from the cascode device. Thus, better phase noise performance can be achieved by series connection be-

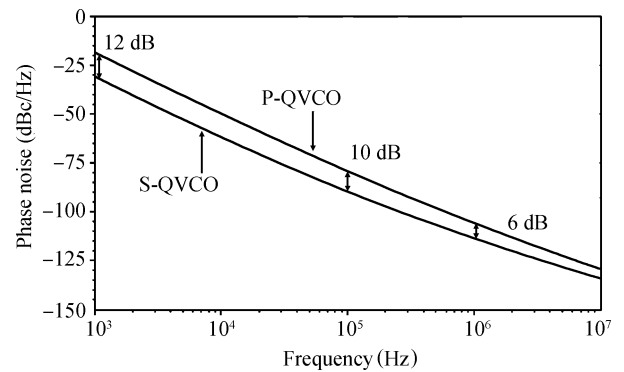


Fig. 9. Phase noise comparison.

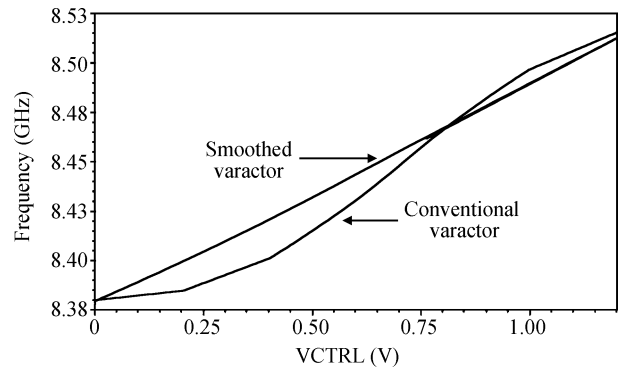


Fig. 10. Tuning curves of conventional and smoothed varactors.

tween coupling and switching transistors as shown in Fig. 9. The two QVCOs present almost the same phase error. However, the phase error of the S-QVCO depends on the amount of mismatch between ideally identical components. Therefore, the S-QVCO is more suitable for our design.

In addition, a linearization technique is used to lower the effective KVCO while maintaining the same tuning range^[5]. Nearly the whole supply voltage range is exploited as shown in Fig. 10. Varactors biased at different voltages connect with MIM capacitors in series as DC blockers. The DC bias voltages are generated by a resistor ladder. As shown in Fig. 11, the resonators are each made of a differential inductor, an array of 5-bit binary weighted switched capacitors and thick oxide MOS varactors. A $K_{VCO} = 120 \text{ MHz/V}$ is adopted to achieve

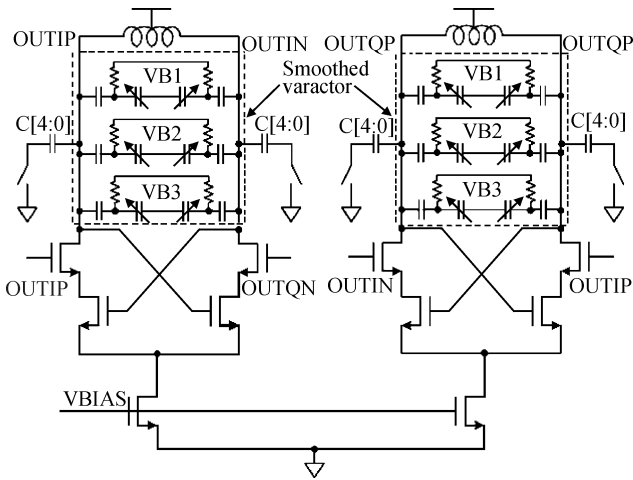


Fig. 11. Schematic of a top-series QVCO with smoothed varactors.

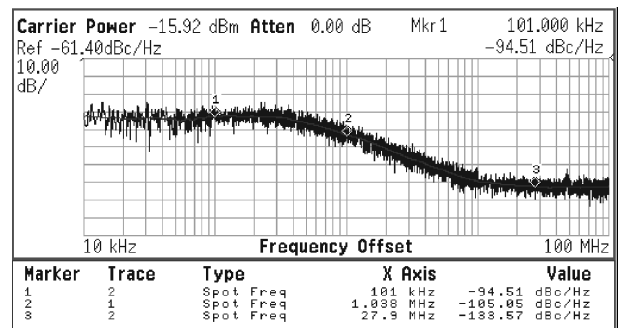


Fig. 13. Measured PLL phase noise and integrated phase noise.

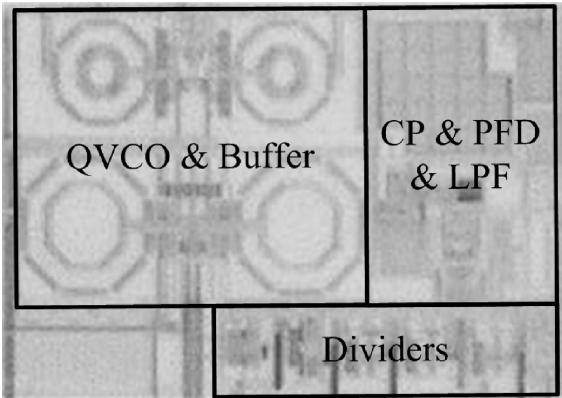
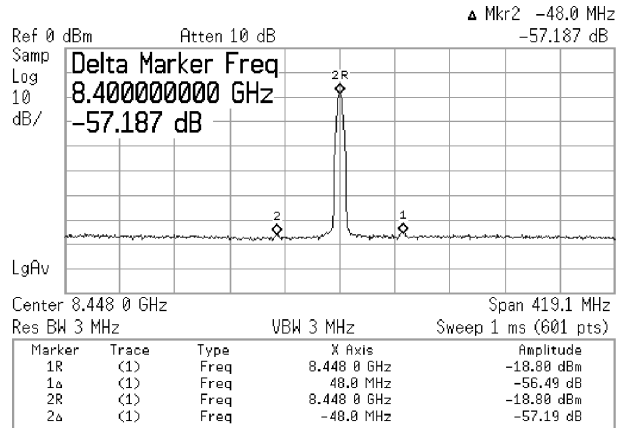
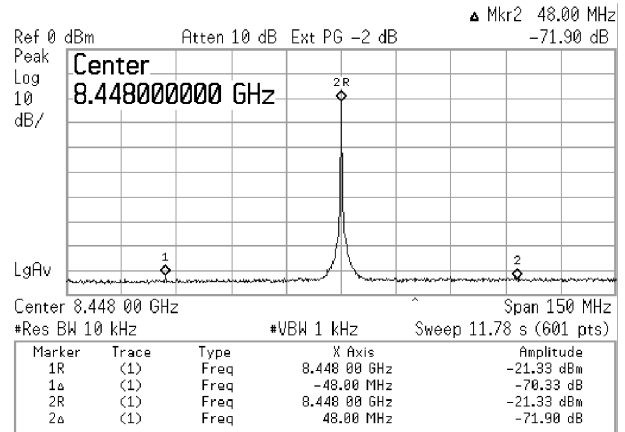


Fig. 12. Chip photograph.



(a)



(b)

Fig. 14. Comparison of the measured QPLL reference spurs (a) without and (a) with the glitch-suppression technique.

lower AM-FM noise conversion.

4. Experimental results

The QPLL is designed and fabricated using the TSMC 0.13- μm 1P8M CMOS process. A photograph of the chip is shown in Fig. 12. The circuit occupies an active area of $0.9 \times 1.3 \text{ mm}^2$, and draws a static current of 13 mA from a 1.2-V supply voltage.

The measured tuning range of the S-QVCO is from 7.6 to 9.5 GHz. With an external reference of 48 MHz, the synthesizer is locked at 8448 MHz with a phase noise of -94.5 dBc/Hz at 100 kHz offset and -105 dBc/Hz at 1 MHz offset as shown in Fig. 13. The measured integrated phase noise from 10 kHz to 50 MHz is 1.93° .

To verify the effect of the glitch-suppression technique, two QPLLs have been fabricated with different CPs. Figure 14(a) shows the reference spurs without glitch-suppression, while the reference spur level is -71 dBc seen from the QPLL with glitch-suppression. The glitch-suppression technique further suppresses the reference spurs by 15 dB. Table 1 presents the performance summary of the proposed QPLL and a comparison with previously published PLLs.

5. Conclusions

A fully integrated 0.13 μm CMOS QPLL with a glitch-rejected CP is presented. The CP not only exhibits perfect current matching characteristics, but also suppresses the current glitch effectively. Moreover, a high-speed PFD and linearity enhancement technique are employed to remove the dead zone and improve the linearity of the QPLL. To guarantee the phase accuracy, a series-QVCO and QIFDs are used. The 8448 MHz QPLL achieves a phase noise of -95 dBc/Hz at 100-kHz frequency offset and measures a reference spur of -71 dBc . The

Table 1. Performance summary and comparison.

Parameter	Ref. [8]	Ref. [9]	Ref. [10]	This work
Process (μm)	0.18 CMOS	0.18 CMOS	0.13 CMOS	0.13 CMOS
Supply voltage (V)	1.8	1.8	1	1.2
Frequency (GHz)	4.8	9.953	2	8.448
Reference frequency (MHz)	1	2488	62.5	48
Phase noise (dBc/Hz) @ 1 MHz	-104	-107	-99.27	-105
Reference spur (dB)	-55	N/A	N/A	-71
Area (mm^2)	0.9	0.71	0.40	1.17
Power consumption (mA)	10	81	12	13

whole PLL circuit (without test buffer) only consumes a current of 13 mA for a 1.2-V supply voltage with active area of $0.9 \times 1.3 \text{ mm}^2$.

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