In situ nanoscale refinement by highly controllable etching of the (111) silicon crystal plane and its influence on the enhanced electrical property of a silicon nanowire*

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Abstract: Nanoscale refinement on a (100) oriented silicon-on-insulator (SOI) wafer was introduced by using tetra-methyl-ammonium hydroxide (TMAH, 25 wt%) anisotropic silicon etchant, with temperature kept at 50 ℃ to achieve precise etching of the (111) crystal plane. Specifically for a silicon nanowire (SiNW) with oxide sidewall protection, the *in situ* TMAH process enabled effective size reduction in both lateral (2.3 nm/min) and vertical (1.7 nm/min) dimensions. A sub-50 nm SiNW with a length of microns with uniform triangular cross-section was achieved accordingly, yielding enhanced field effect transistor (FET) characteristics in comparison with its 100 nm-wide pre-refining counterpart, which demonstrated the feasibility of this highly controllable refinement process. Detailed examination revealed that the high surface quality of the (111) plane, as well as the bulk depletion property should be the causes of this electrical enhancement, which implies the great potential of the as-made cost-effective SiNW FET device in many fields.

Key words: TMAH etching; nanofabrication; silicon nanowire; field effect transistor
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1. Introduction

Anisotropic etching, which typically exhibits great disparities in etch rate for different single crystal planes, e.g. the (100) and (111) planes in the case of silicon, has been widely used in the field of micro-electro-mechanical systems (MEMS) for decades because of its convenience, high efficiency and cost-effectiveness. A variety of important structures, such as cantilever, micro-beam and microfluidic channels, can be realized with appropriate process flow by using anisotropic etching. Moreover, with specific design, it also plays a role in the advent of nanotechnology, especially in the definition of nanostructures[1, 2].

Multiple silicon etchants, including KOH and EPW, have been developed to achieve reliable anisotropic etching[3]. Improvements, however, are required to solve problems such as metallic ion pollution and toxicity during manipulation. TMAH, on the other hand, is non-toxic, and convenient to handle under different conditions. In addition, it yields great CMOS compatibility and material selectivity without altering the anisotropic feature. In-depth research has been conducted on the etching behavior of TMAH[4–6]. Generally, a higher temperature was used (70–90 ℃) to get fast silicon etching and undercutting for the purpose of cavity formation and structure release. However, the precise controllability of the TMAH etch rate, which was usually the key factor in nanofabrication, was only reliable under lower temperatures (down to 50 ℃).

In our previous work[7], a novel and cost-effective fabrication method that employed TMAH etching was developed to define a silicon nanowire with a width around 100 nm. Herein, based on investigation of TMAH undercutting of thin silicon film, an efficient *in situ* nanoscale refinement was introduced, which enabled effective reduction of the original SiNW's width down to 40 nm. Enhanced FET characteristics, attributed to crystal surface quality and bulk depletion, were also extracted, which implied the great potential of refined SiNW devices.

2. Experiments and fabrication

TMAH undercutting has been used to refine SiNW with trapezoid cross-section in the lateral direction[8], with the risk that the wire could be terminated when the two undercut (111) crystal planes met at the center (as noted in Fig. 1(a)). In fact, as long as the process stability of TMAH etching was guaranteed,

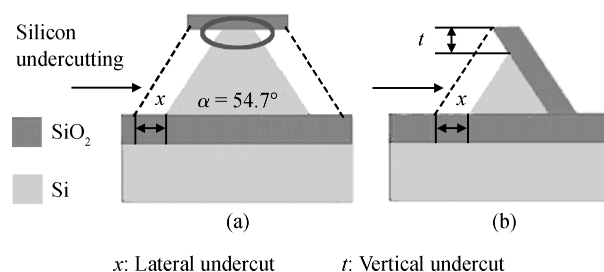

Fig. 1. Undercutting-based nanowire refinements. (a) One-dimensional silicon refinement. (b) Two-dimensional silicon refinement.

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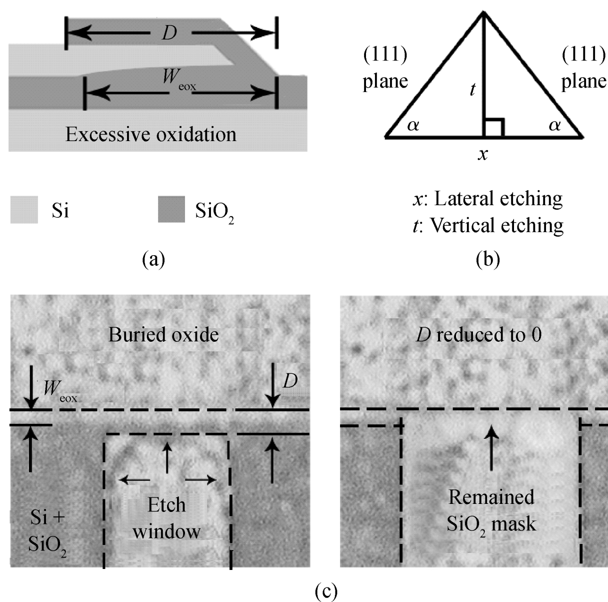

Fig. 2. Thin film TMAH undercutting. (a) Etching structure with excessive oxidation. (b) Geometric relationship between etching lengths in different directions. (c) High-resolution microscope snapshots.

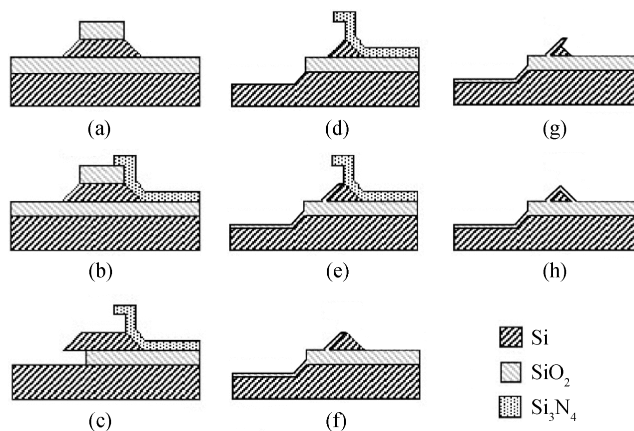

Fig. 3. *In situ* nanowire refinement applied in the fabrication process of a SiNW.

the *in situ* refinement was more efficient when we used silicon thin film with transient thickness, which enabled effective size reduction in both lateral and vertical directions. Combined with sidewall protection, the process would be even safer, avoiding the unintentional failure of SiNWs (Fig. 1(b)).

2.1. Thin film TMAH undercutting

Experiments were carried out first to characterize the etching behavior of TMAH (25 wt%, 50 ℃) for a transient thin film with a thickness of nanometers. The test samples were fabricated by oxidation of the structure layer on a SOI wafer and opening the etching window as described in Appendix A. Owing to oxygen diffusion through the buried oxide, there is an "excessive oxidation region" near the edge of the pattern (Fig. 2(a)), which formed the transient thin film, which was also observed with a microscope (with a range of w_{eox} = 500 nm in Fig. 2(c)). The distance D from the etching interface to the pattern edge was recorded using a HIROX KH-7700 high-resolution microscope workstation as illustrated in Fig. 2(c). The etch length over a specific period of time for the (111) plane can then be derived by timing the average lateral etching length by a coefficient of sin $\alpha = 54.7°$ is the characteristic angle between the (100) and (111) crystal planes (Fig. 2(b)).

2.2. *In situ* nanowire refinement

Based on our previously developed process[7], the *in situ* TMAH nanoscale refinement of a SiNW with triangular cross-section was validated. After defining the SiNW with width about 100 nm (Fig. 3(d)), a thin film oxidation (20 nm) was adopted to provide silicon dioxide sidewall protection during the subsequent TMAH refining (Fig. 3(f)). The process was efficient because it reduced the size in both lateral and vertical directions.

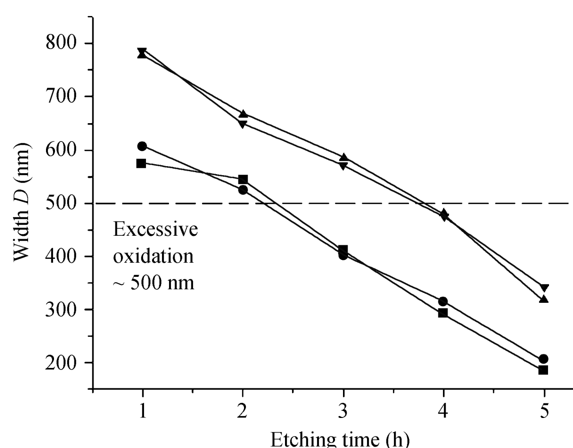

Fig. 4. TMAH undercutting for a silicon thin film with transient thickness; an almost constant-rate etching was observed for four test samples with different initial D.

After the metallization, the FET transfer characteristics of the as-made SiNW device were extracted using a Cascade probe station with an HP 4156 module, with varying gate and source–drain voltages, to evaluate the gate control capability. For simplicity, the silicon substrate was used as the back gate, with I/V measurements implemented though the SiNW, and finally comparison was made between the refined SiNW and its 100 nm pre-refining counterpart (Fig. 3(d)).

3. Results and discussion

3.1. Thin film TMAH undercutting

For undercutting characterization of the single-crystal silicon layer in nanometers, as described in Section 2.1, the TMAH solution exhibited some unique features. Etching data of four test samples with different initial D are listed in Fig. 4, and an almost constant-rate (140 nm/h or 2.3 nm/min) undercutting was observed. Taking the transient thickness of silicon near the edge of the patterns owing to excessive oxidation into account, the undercutting rate was almost independent of the layer thickness, which meant that factors generally decelerating the etching, such as diffusion-induced limitation[9] and the

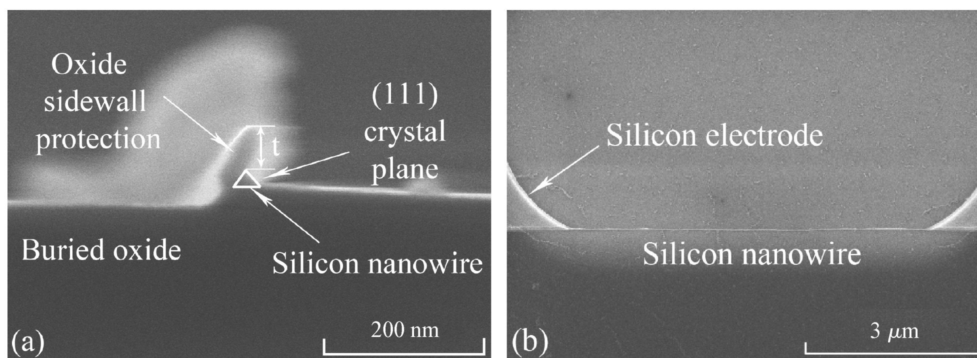

Fig. 5. SEM aspects of *in situ* nanowire refinement. (a) Cross-section geometry, with the SiNW outlined for illustration. (b) SiNW with length in microns.

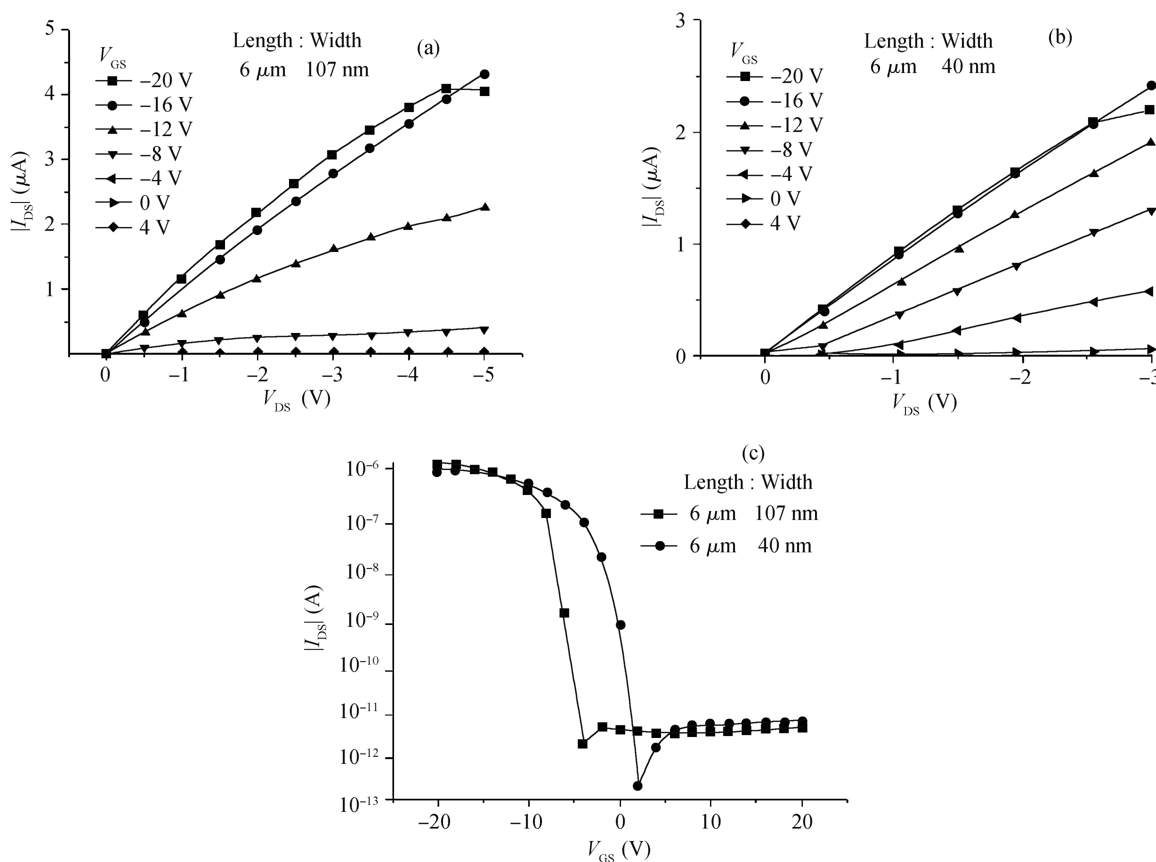

Fig. 6. FET characteristics of an *in situ* refined SiNW and its pre-refining counterpart. (a) Pre-refining SiNW with width of 107 nm. (b) *In situ* refined SiNW with width of 40 nm. (c) Transfer curves with $V_{DS} = -1$ V.

electric double layer (EDL) effect[7], did not dominate in the silicon undercutting. In fact, the ultra-slow etching for (111) silicon crystal plane was 'screening' the influence of etchant concentration fluctuations; in other words, the front-end etchant consumption is always determined by the etch-rate of the (111) plane, which is constant throughout the silicon layer with transient thickness.

3.2. *In situ* nanowire refinement

For structures with oxide sidewall protection, controllable etching of the (111) plane was also observed (Fig. 5(a)). The vertical etch rate was determined by SEM measurement as 1.7 nm/min. Compared to the lateral etch rate (2.3 nm/min), a concise relationship of $\sqrt{2}$ had been achieved. We note that it is exactly the geometric relationship in Fig. 2(b) that further demonstrated the viability of sidewall protection by a thermally grown oxide, and similar etching behavior of the (111) crystal plane as the TMAH undercutting procedure. This sidewall protection process could be applied to refine the nanostructure effectively, as long as the controllability was guaranteed by lower temperature TMAH etching.

Using this *in situ* refinement process, a sub-50 nm nanowire with a length of several microns was successfully realized (Fig. 5(b)). The width of the nanowire could be reduced to 40 nm, attaining the resolution of much more expensive pro-

cesses such as E-beam lithography[11]. With respect to other popular top-down SiNW fabrication methods, self-limiting oxidation for instance[12], the remaining (111) crystal plane in our solution would yield higher efficiency in specific applications such as surface monolayer modification for bio-chemical detection[8].

The FET characteristic for a single silicon nanowire (6 μm long and 40 nm wide) was extracted for comparison with its pre-refining counterpart (6 μm long and 107 nm wide). As illustrated in Figs. 6(a) and 6(b), typical gate modulation of p-type devices in accumulation mode was observed. The current level of the refined SiNW in "on" status proved to be comparable to that reported in Refs. [11, 12], with even smaller cross-section area because of its triangular character, which demonstrated the high quality of our SiNWs. With the same length, an "on" current ratio proportional to the cross-section area according to the Ohm Principle, which is $(107/40)^2 = 7.16$ in this case, was expected. However, the ratio proved to be only 1.24 (when $V_{GS} = -20$ V and $V_{DS} = -1$ V). We attributed the current enhancement of the thinner nanowire device to the thermally grown sidewall process (Fig. 3(e)) and the *in situ* TMAH refinement (Fig. 3(f)). The oxidation effectively reduced the defects on the (111) crystal plane, and TMAH etching removed the lattice damage due to the great Si–Si_3N_4 interfacial stress, which both contributed to alleviate the carrier scattering and trapping that drastically confined the "on" current in such a minute structure.

The transfer curves, on the other hand, are shown in Fig. 6(c). The on/off ratios are both about 10^5–10^6, which indicated bulk depletion with forward bias, as expected by using width estimation of the planar depletion layer (Appendix B). Accordingly the thinner device was believed to have the advantage of reaching the bulk depletion more quickly with its smaller dimension. A difference was also noticed when investigating the threshold voltage (V_{th}). In the case of the pre-refining device (107 nm), a negative shift (about -4 V) of threshold voltage from 0 V implied some defect-induced carrier trapping with light channel doping (5×10^{15} cm^{-3}), while for a refined 40 nm nanowire device the threshold voltage was located near 0 V as a result of surface quality improvement, which has been discussed for "on" current enhancement, and further confirmed the advantage of such an *in situ* nanoscale refinement base on highly controllable etching of the (111) silicon crystal plane. We note that low-voltage operation is preferred for nanowire applications, such as electronic devices and hand-held sensors.

4. Conclusion

In this paper, the undercutting behavior of TMAH anisotropic silicon etchant was studied at relatively lower temperature (50 ℃) for a (100) oriented silicon-on-insulator layer having a thickness of nanometers. An almost thickness-independent etch rate was observed owing to the ultra-stable etching of the (111) silicon crystal plane. Combined with oxide sidewall protection, reliable and effective *in situ* nanoscale refinement, which enabled size reduction in both the lateral and vertical directions, was realized to reduce the width of the as-made silicon nanowire to 40 nm. Electronic characterization for such nanowire FET devices exhibited enhanced performance in comparison with their pre-refining counterparts (107 nm). The sidewall oxidation and TMAH undercutting helped to remove surface defects and lattice damage generated by previous processes. Also, the smaller dimension facilitated the bulk depletion procedure which improved the gate control capability. The high current level, as well as the lower operation voltage, implied the great potential of this highly controllable and cost-effective SiNW device in many fields.

Appendix A

First, a 100 nm oxide layer was thermally grown upon the 200-nm-thick (100) oriented top silicon layer on a p-type (1–10 Ω·cm) silicon-on-insulator (SOI) wafer. Patterns with ⟨110⟩ aligned square windows were sequentially transferred by optical lithography and buffered HF etching to expose part of the underlying silicon surface. Using TMAH anisotropic etchant (25 wt%), the boundary of the top silicon layer was automatically aligned in the ⟨110⟩ direction, and a very smooth (111) plane could be formed. Then the SiO_2 mask was totally removed, followed by another oxidation to reduce the silicon layer thickness below 100 nm. Etch windows were sequentially opened nearly 1 μm away from the original silicon boundary as shown in Fig. 2(a). The wafer was finally split to test samples for later TMAH etching. The temperature of the TMAH etchant was kept at 50 ℃, and test chips were rinsed with deionized water (DIW) every 60 min for data sampling.

Appendix B

The maximum width of the depletion layer in a gate–insulator–semiconductor device is determined by[10]

$$x_{\mathrm{dmax}} = \left[\frac{4\varepsilon_{\mathrm{r}}\varepsilon_0 k_{\mathrm{B}} T \ln(N_{\mathrm{A}}/n_{\mathrm{i}})}{q^2 N_{\mathrm{A}}}\right]^{1/2},$$

where ε_{r} is the relative dielectric constant, ε_0 is the vacuum permittivity, k_{B} is the Boltzmann constant, and T is the temperature. As for carrier parameters, q represents the carrier charge, N_{A} is the dopant concentration and n_{i} is the intrinsic carrier concentration. Using $\varepsilon_{\mathrm{r}} = 11.9$, $\varepsilon_0 = 8.85418781762 \times 10^{-12}$ F/m, $q = 1.60217733 \times 10^{-19}$ C, $k_{\mathrm{B}} = 1.380658 \times 10^{-23}$ J/K, $T = 293$ K, $n_{\mathrm{i}} = 1.45 \times 10^{10}$ cm^{-3}, and $N_{\mathrm{A}} = 5 \times 10^{15}$ cm^{-3} of the nanowire structure, the depletion region width can be calculated as $x_{\mathrm{dmax}} = 411.6$ nm.

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