Continuous time sigma delta ADC design and non-idealities analysis*

Yuan Jun(袁俊)[1,†], Zhang Zhaofeng(张钊锋)[3], Wu Jun(吴俊)[3], Wang Chao(王超)[3], Chen Zhenhai(陈珍海)[1], Qian Wenrong(钱文荣)[2], and Yang Yintang(杨银堂)[1]

[1]School of Microelectronics, Xidian University, Xi'an 710071, China
[2]Marvell Technology Group, Ltd., Shanghai 201203, China
[3]Shanghai Advanced Research Institute, Chinese Academy of Sciences,201203,China

Abstract: A wide bandwidth continuous time sigma delta ADC is implemented in 130 nm CMOS. A detailed non-idealities analysis (excess loop delay, clock jitter, finite gain and GBW, comparator offset and DAC mismatch) is performed developed in Matlab/Simulink. This design is targeted for wide bandwidth applications such as video or wireless base-stations. A third-order continuous time sigma delta modulator comprises a third-order RC operational-amplifier-based loop filter and 3-bit internal quantizer operated at 512 MHz clock frequency. The sigma delta ADC achieves 60 dB SNR and 59.3 dB SNDR over a 16-MHz signal band at an OSR of 16. The power consumption of the CT sigma delta modulator is 22 mW from the 1.2-V supply.

Key words: ADC; continuous time; sigma delta ADC; low power design; sigma delta modulation
DOI: 10.1088/1674-4926/32/12/125007 **EEACC:** 2570

1. Introduction

Today, discrete high-speed, high-resolution analog-to-digital conversion (ADC) ICs are based on pipeline conversion technology. These Nyquist-rate ADCs are the core building blocks of analog receiver front ends. However, the oversampling of ADC has traded digital signal processing complexity for relaxed requirements on the analog components compared to Nyquist-rate ADC[1]. Recently, the popularity of continuous-time (CT) ADC has been growing for application-specific ICs[2−4]. Moreover, CT implementation of ADC extends the input frequency range from a few 100 kHz up to a few 10 MHz and has proven to be very power efficient[5−7].

Compared with pipeline and discrete-time (DT) sigma delta converters, CT converters have advantages of a lower power consumption and inherent anti-aliasing filtering, hence extending battery life and reducing system complexity, which are especially important for portable wireless devices. Moreover, the absence of stringent settling requirements enables CT converters to digitize signals up to several hundred MHz, which is still not possible for their DT counterparts. However, they are more sensitive to clock jitter and feedback loop delay than DT sigma delta modulators, and they suffer from a large loop coefficient uncertainty due to the process variations of resistors and capacitors.

This paper describes the design and system considerations of the CT modulator. The circuit design and results of CT sigma delta ADC are presented.

2. System design and non-idealities analysis

2.1. CT sigma delta modulator architecture

The target specification for the CT sigma delta ADC described in this paper is defined to be 12 bits with a low voltage, low power, wide-bandwidth design.

At a system level, the resolution achieved by a sigma delta modulator is a function of the oversampling ratio (OSR), noise-shaping order and quantizer resolution[8]. In the present design, an OSR = 16 is imposed as a compromise between a technologically feasible clock frequency and the robustness requirement for a signal bandwidth of 16 MHz. To suppress quantization noise sufficiently for 12-bit performance, multibit quantization and at least a third-order noise-transfer function (NTF) are essential (Fig. 1).

The proposed continuous-time modulator architecture is shown in Fig. 1. The modulator comprises a 3-bit internal quantizer, operating at 512 MHz with an oversampling ratio of 16, and a third-order single-loop filter. In order to save power and maintain a good anti-alias filter characteristic, a combination of feedforward and feedback stabilized loop filters are implemented[8,9].

2.2. Excess loop delay

In real circuits, excess loop delay (ELD) is non-zero due to the finite speed of transistors. The ELD is usually introduced by the quantizer, DAC, DEM and loop filter. In DT modulators, ELD is negligible, but in CT modulators the ELD is very important.

A common solution to the excess loop delay while using an NRZ DAC pulse is to introduce an explicit full clock delay in the feedback path to absorb the varying quantizer delay as well as the other possible delays caused by the logic circuits. However, due to this full clock delay, the impulse response of the CT loop at the sampling instant T_s is zero. To compensate this response sample, an extra feedback branch is added directly to the quantizer input to make the total impulse response

* Project supported by the National Science and Technology Major Projects, China (No. 2010ZX03006-003-02).
† Corresponding author. Email: jyuan_sea@hotmail.com
Received 31 May 2011, revised manuscript received 3 August 2011
© 2011 Chinese Institute of Electronics

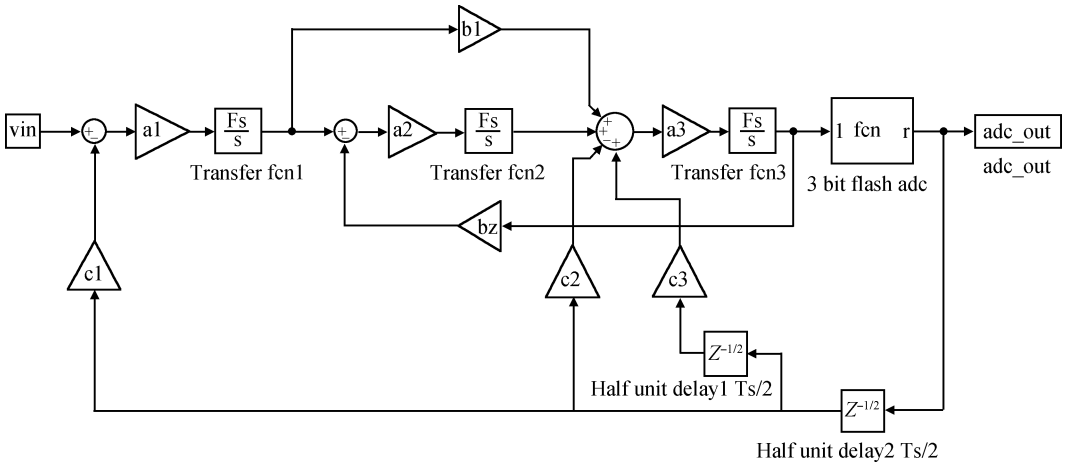

Fig. 1. Continuous time sigma delta modulator architecture.

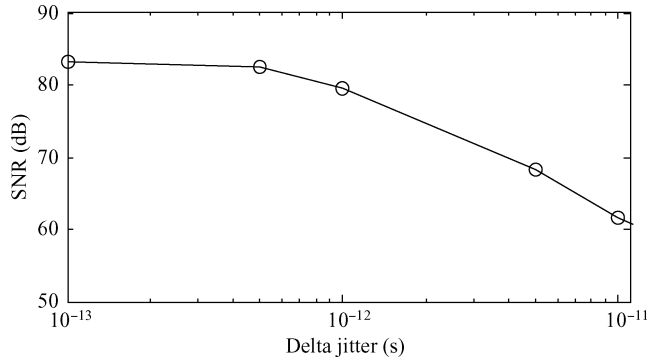

Fig. 2. Influence of clock jitter.

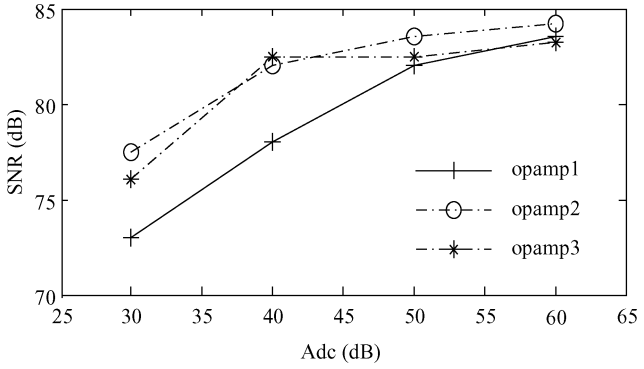

Fig. 3. SNR versus Adc.

equivalent to the DT target[10].

In this design, the quantizer and feedback DAC are clocked with opposite phase of the clock to avoid asynchronous feedback (caused by excess loop delay), hence improving the SNR. The delay of 1/2 clock may cause a stability issue. This is because the delay has altered the NTF. However, if this 1/2 clock delay has been accounted for in the loop filter design (or NTF design), stability can be maintained.

2.3. Clock jitter

In CTSD ADC, both the quantizer and the feedback DAC are clocked. The sampling error due to clock jitter at the quantizer is shaped by the same order of modulator so that it adds little noise to the modulator output. However, clock jitter in the feedback DAC generates noise that is not shaped and affects the modulator performance significantly. Assuming the clock jitter is in the front of white noise with a Gaussian distribution, its standard deviation is $\sigma_{\Delta t\_\mathrm{CT}}$. The in-band jitter error is reduced by a factor of the OSR over the total jitter error above, so we can calculate the signal-to-jitter noise ratio as:

$$\mathrm{SNR}_{\mathrm{jitter\_CT}} = \frac{P_{\mathrm{s}}}{P_{\mathrm{jitter}}} = \frac{\mathrm{OSR}\cdot A^2}{2\sigma_{\Delta y}^2 \dfrac{\sigma_{\Delta t\_\mathrm{CT}}^2}{T_{\mathrm{s}}^2}}, \tag{1}$$

where OSR is the oversampling ratio, A is signal amplitude, $\sigma_{\Delta y}$ is the standard deviation of the adjacent output difference, and $\sigma_{\Delta t\_\mathrm{CT}}$ is the standard deviation of the clock jitter.

In this design, nonreturn-to-zero (NRZ) DAC pulse shaping is used to reduce clock jitter sensitivity. To minimize performance degradation, the clock circuit should have a jitter value as low as 1 ps RMS as shown in Fig. 2.

2.4. Amplifier finite gain and GBW

In a CTSD modulator, the loop stability is more sensitive to the accuracy of the first several samples of the loop impulse response than to that of the other samples. In other words, the bandwidth of the low order loops, which contribute more to those first several samples than the high order loops, are more critical for the loop stability[11].

In this design, the finite gain of the amplifier is not critical (as seen in Fig. 3). 50 dB is more than sufficient to make the SNR degradation negligible. From the results shown in Fig. 4, the gain-bandwidth product of the third amplifier has the highest requirements, which should be larger than 1.5 G. The influence of integrator time constant error is also very important, as seen in Fig. 5. The tolerance variance of RC is 20%.

2.5. Comparator offset

Comparator offset should not be ignored in 0.13 μm technology. In this design, the results shown in Fig. 6 indicate that the offset should not be higher than 20 mV since the SNDR variation increases.

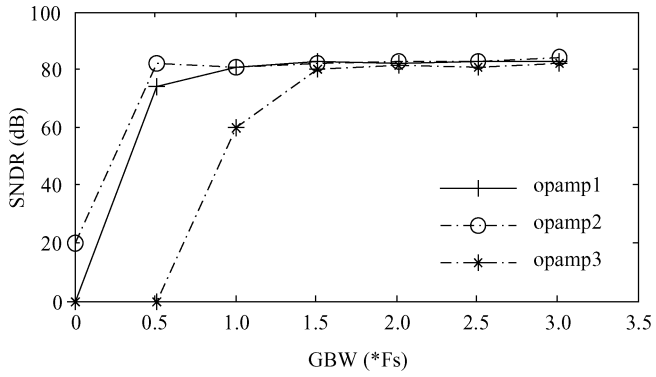

Fig. 4. SNDR versus GBW.

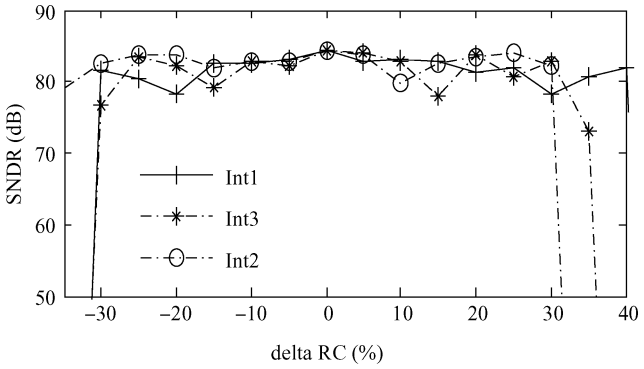

Fig. 5. Influence of integrator time constant error: SNR versus delta RC.

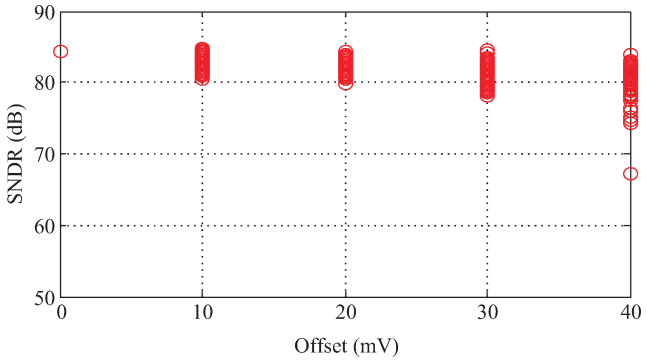

Fig. 6. Monte Carlo simulation: SNDR versus comparator offset.

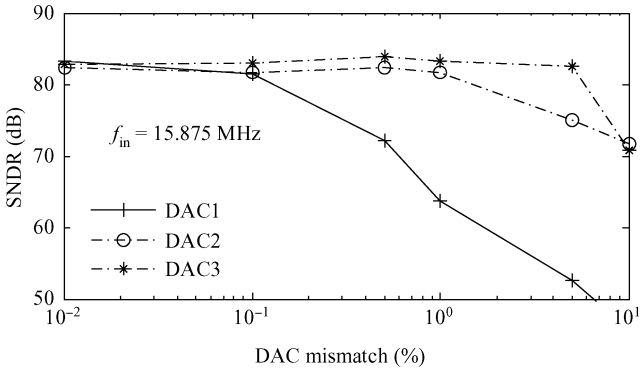

Fig. 7. Influence of DAC mismatch: SNDR versus DAC mismatch.

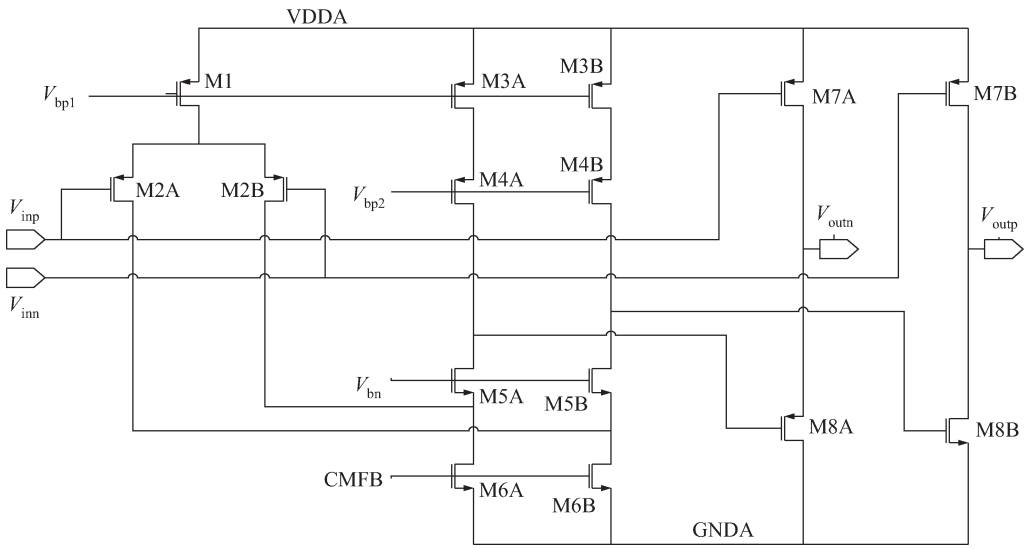

Fig. 8. Simplified schematic of a two-stage operational amplifier with class-AB output stage.

2.6. Feedback DAC mismatch

As shown in Fig. 7, the DAC1 is the major source of noise and distortion, since it is unshaped and has higher requirements than ADC accuracy. In this design, the mismatch error of the DAC1 should be as small as 0.01%.

3. Circuit design and results

With a 512 MHz sample frequency, the bandwidth requirement for the loop filter amplifiers is at least 1 GHz. A feedforward compensation amplifier is designed for this low power, low voltage design. A novel two-stage amplifier is shown in Fig. 8 for this design. A feedforward block is used with transconductances M7A and M7B to cancel out a zero and to provide class AB biasing in the output stage, which is the main innovation. The first stage is used to increase the gain and the second stage is used to enhance the output swing.

The quantizer consists of seven latched comparators. Each

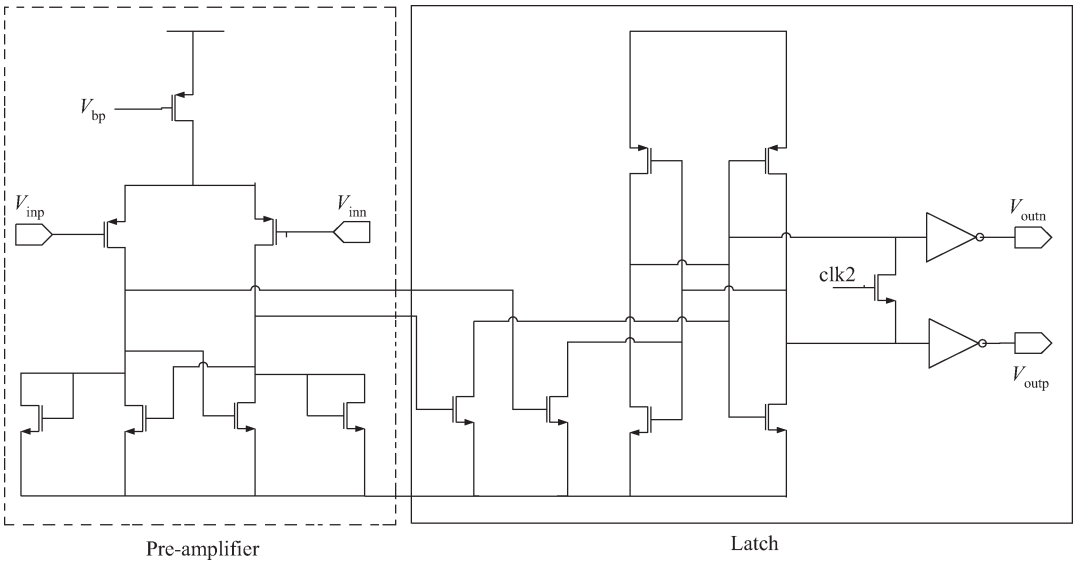

Fig. 9. Schematic of the comparator.

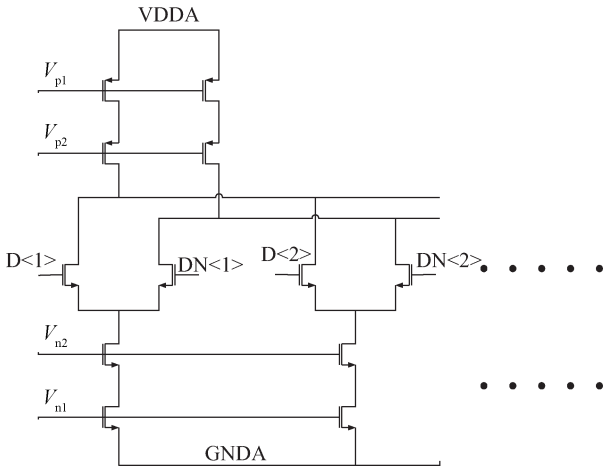

Fig. 10. Schematic of the DAC.

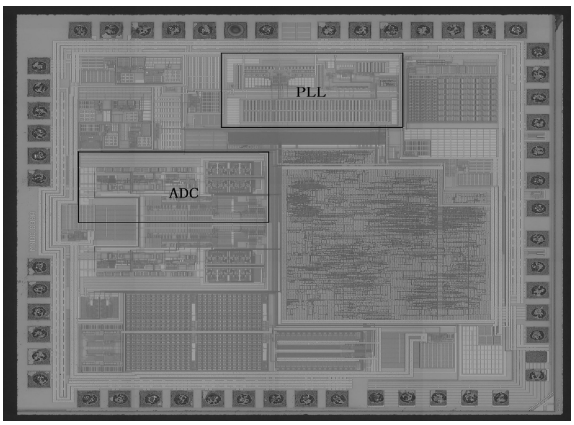

Fig. 11. Chip photo.

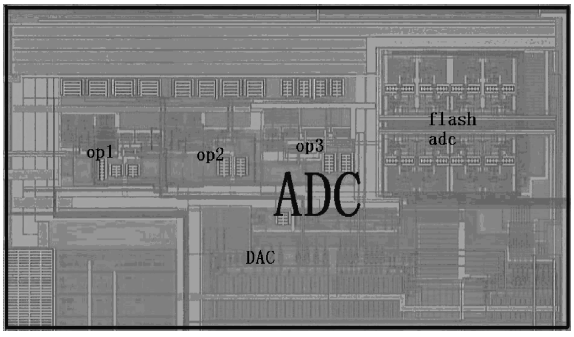

Fig. 12. ADC photo.

latched comparator is composed of a pre-amplifier stage and a latch (Fig. 9). During clk2, the preamplifier is in the input offset cancellation status and the latch is reset to reduce the hysteresis. During clk1, the output of the third integrator subtracted by reference voltage is amplified by the pre-amplifier and fed into the regenerative latch, and then is quickly amplified to the logic levels.

The current steering DAC is shown in Fig. 10 for this design. The cascade transistor is used to increase the output impedance of the current source and at the same time, to prevent the dynamic glitches caused by switch. In this modulator, in order to reduce the excess loop delay as well as the circuit complexity, no dynamic element matching (DEM) is used to shape the DAC error. So the mismatch error of the unit current cells should be as small as 0.01%.

The ADC is implemented in a 130 nm 5-metal-layer CMOS process. Figure 11 illustrates a completed chip photograph and the chip photo of proposed ADC is shown in Fig. 12. Figure 13 shows the simulated power spectral density. The input frequency is 12 MHz. The second and third harmonic distortions are well below –61.9 dB and –44 dB. Furthermore, Figure 14 shows the simulated signal-to-noise-plus-distortion ratio (SNDR) versus the normalized input signal. The sigma delta output bit stream has been recorded with a logic analyzer, so that the data can be processed off line with MATLAB. Accordingly, the fast Fourier transformation with 16384 points and the Blackman-Harris windows have been applied. The DR and the peak SNDR is 70 dB and 61 dB, respectively. The power

Table 1. Performance comparison between reported designs and this work.

Reference	Architecture	SNDR (dB)	BW (MHz)	Jitter sensi (ps rms)	Power (mW)	FOM (pJ/conv.)
[12]	3rd-order, real	74	20	0.3	20	0.12
[13]	2-2 MASH, real	56	10	N/A	122	11.83
[14]	4th-order, complex	68.8	23	3	42.6	0.41
[15]	MASH, complex	69	20	N/A	56	0.61
[16]	5th-order, real	52	10	N/A	7	1.07
[17]	4th-order, real	61	12	20	70	3.18
[18]	4th-order, real	61	15	10	70	2.54
[19]	2nd-order, complex	53	20	N/A	32	2.19
[20]	3rd-order, real, time-interleaved	57/49	10/20	N/A	87	7.5/9.43
This work	3rd-order, real	59.3	16	N/A	22	0.912

FOM = Power/[2 · BW · $2^{(\mathrm{SNDR}-1.76)/6.02}$]. Smaller FOM is better.

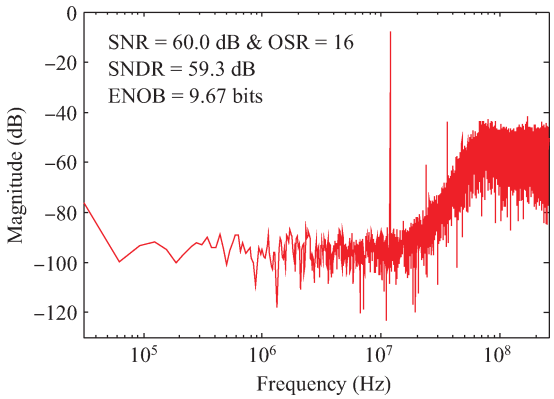

Fig. 13. Power spectral density (BW = 16 MHz).

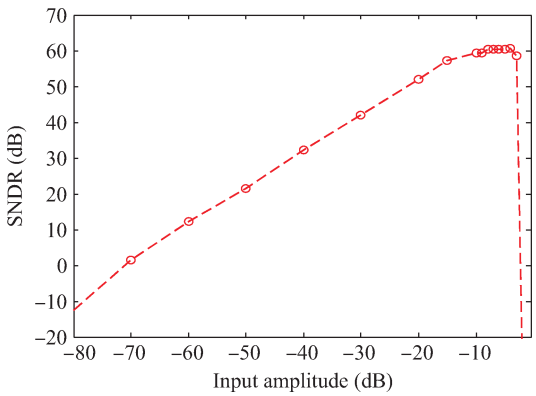

Fig. 14. Input amplitude versus SNDR.

consumption and the resulting FOM as a function of the supply voltage are shown in Table 1. Table 1 lists previously reported wideband (BW ⩾ 10 MHz) continuous time modulators. Compared with them, this work is not the best but still good.

4. Conclusion

A detailed non-idealities analysis (excess loop delay, clock jitter, finite gain and GBW, comparator offset and DAC mismatch) has been performed and developed in Matlab/Simulink in this paper. A low-voltage low-power wide bandwidth continuous time sigma delta ADC is implemented in 130 nm CMOS process based on active RC integrators. 70 dB DR is achieved in a bandwidth of 16 MHz and the power consumption is only 22 mW for a 1.2 V supply.

Acknowledgments

The authors want to appreciate the Shanghai Advanced Research Institute, Chinese Academy of Sciences to support this research.

References

[1] Norsworthy S R, Schreier R, Temes G C. Delta–sigma data converters: theory, design, and simulation. New York: IEEE Press, 1996

[2] Munoz F, Philips K, Torralba A. A 4.7 mW 89.5 dB DR CT complex DS ADC with built-in LPF. IEEE ISSCC Dig Tech Papers, 2005: 500

[3] Van der Zwan E J, Philips K, Bastiaansen C. A 10.7 MHz IF-to-baseband sigma delta A/D conversion system for AM/FM radio receivers. IEEE ISSCC Dig Tech Papers, 2000: 340

[4] Philips K. A 4.4 mW 76 dB complex delta–sigma ADC for Bluetooth receivers. IEEE ISSCC Dig Tech Papers, 2003: 64

[5] Moyal M, Groepl M, Werker H, et al. A 700/900 mW/channel CMOS dual analog front-end IC for VDSL with integrated 11.5/14.5 dBm line drivers. IEEE ISSCC Dig Tech Papers, 2003: 416

[6] Yan S, Sánchez-Sinencio E. A continuous-time sigma delta modulator with 88 dB dynamic range and 1.1 MHz signal bandwidth. IEEE ISSCC Dig Tech Papers, 2003, 46: 62

[7] Paton S, Giandomenico A D, Hernández L, et al. A70-mW 300-MHz CMOS continuous-time sigma–delta ADC with 15-MHz bandwidth and 11-bits of resolution. IEEE J Solid-State Circuits, 2004, 39(7): 1056

[8] Norsworthy S R, Schreier R, Temes G C. Delta–sigma data converters: theory, design and simulation. Wiley-IEEE Press, 1996

[9] Brigati S, Francesconi F, Malcovati P, et al. Modeling sigma–delta modulator non-idealities in SIMULINK. Proceedings of the International Symposium on Circuits and Systems, 1999, 2: 384

[10] Yan S, Sanchez-Sinencio E. A continuous-time sigma–delta modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth. IEEE J Solid-State Circuits, 2004, 39: 75

[11] Chen X, Wang Y, Fujimoto Y, et al. A 18 mW CT sigma delta modulator with 25 MHz bandwidth for next generation wireless applications. IEEE Custom Integrated Circuits Conference,

2007: 73

[12] Mitteregger G, Ebner C, Mechnig S, et al. A 20 mW 640 MHz CMOS continuous-time ΣΔ ADC with 20 MHz signal bandwidth, 80 dB dynamic range and 12 bit ENOB. IEEE J Solid-State Circuits, 2006, 41(12): 2641

[13] Breems L J. A cascaded continuous-time sigma delta modulator with 67 dB dynamic range in 10 MHz bandwidth. ISSCC Dig Tech Papers, 2004: 72

[14] Yaghini N, Johns D. A 43 mW CT complex delta sigma ADC with 23 MHz of signal bandwidth and 68.8 dB SNDR. ISSCC Dig Tech Papers, 2005: 502

[15] Breems L J, Rutten R, van Veldhoven R, et al. A 56 mW CT quadrature cascaded sigma delta modulator with 77 dB DR in a near zero-IF 20 MHz band. ISSCC Dig Tech Papers, 2007: 238

[16] Ouzounov S, van Veldhoven R, Bastiaansen C, et al. A 1.2 V 121-mode CT modulator for wireless receivers in 90 nm CMOS. ISSCC Dig Tech Papers, 2007: 242

[17] Paton S, Di Giandomenic A, Hernandez L, et al. A 12 bit continuous-time sigma delta modulator with 400 MHz clock and low jitter sensitivity in 0.13 μm CMOS. VLSI Dig Tech Papers, 2004: 82

[18] Di Giandomenico A, Paton S, Wiesbauer A, et al. A 15 MHz bandwidth sigma–delta ADC with 11 bits of resolution in 0.13 μm CMOS. European Solid-State Circuits Conference, 2003: 233

[19] Arias J, Kiss P, Prodanov V, et al. A 32-mW 320-MHz continuous-time complex delta–sigma ADC for multi-mode wireless-LAN receivers. IEEE J Solid-State Circuits, 2006, 41: 339

[20] Caldwell T, Johns D. A time-interleaved continuous-time sigma delta modulator with 20-MHz signal bandwidth. IEEE J Solid-State Circuits, 2006, 41: 1578