A 200 mA CMOS low-dropout regulator with double frequency compensation techniques for SoC applications

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Abstract: This paper presents a 200 mA low-dropout (LDO) linear regulator using two modified techniques for frequency compensation. One technique is that the error amplifier uses a common source stage with variable load, which is controlled by the output current, is served as the second stage for a stable frequency response. The other technique is that the LDO uses a pole-zero tracking compensation technique at the error amplifier to achieve a good frequency response. The proposed circuit was fabricated and tested in HJTC 0.18 μm CMOS technology. The designed LDO linear regulator works under the input voltage of 2.8–5 V and provides up to 200 mA load current for an output voltage of 1.8 V. The total error of the output voltage due to line and load variation is less than 0.015%. The LDO die area is 630×550 μm^2 and the quiescent current is 130 μA.

1. Introduction

Power management is a very important issue in portable electronic applications. The need for multiple on-chip voltage levels makes the voltage regulator a critical part of electronic system design. The LDO regulator is generally utilized to translate a voltage level or provide a stable output voltage, which has been considered as one of the important components for the power management of wireless applications.

With the rapid development of system-on-chip designs, there is a growing trend toward power-management integration. On-chip and local LDOs are utilized to power up sub-blocks of a system individually, and this can significantly reduce crosstalk, improve the voltage regulation and eliminate load-transient voltage spikes from bondwire inductances. In addition, system-on-chip designs with on-chip and local LDOs can reduce both board space and external pins significantly.

There are some requirements of the regulator, such as line regulation, load regulation, and transient response. To meet these requirements, some different compensation technologies are proposed. The most popular solution to this problem is to create a zero by using equivalent series resistance (ESR) of the output capacitor[1−3]. This kind of frequency compensation has two major drawbacks: sacrifices of cost and area, and a stability problem caused when the load current and output pole are changed. Another proposed solution to this problem is to put a bypass path in the feedback loop[4]. A common drawback in Ref. [4] is that zero moves as the output voltage of LDO changes. Moreover we cannot adapt this scheme if off-chip feedback resistors are used for all-purpose LDOs. In Refs. [5, 6], a low-dropout regulator with an impedance attenuated buffer was purposed for driving the pass device and this will lower its output resistance such that the pole at the gate of the pass device is pushed to high frequencies. In Ref. [7], the proposed circuit generated an internal lower frequency zero

and pushed parasitic poles toward an extremely high frequency such that the loop bandwidth could be extended.

In this paper, based on pole-zero tracking compensation and an error amplifier with variable load serving as the second stage, a dynamic Miller-frequency compensation technology is presented to keep the LDO stable under the full range of the load current.

2. LDO circuit implementation

In this section, both design considerations for the double frequency compensation techniques of an LDO at a system level as well as circuit level are described.

2.1. Traditional LDO analysis

A typical topology of an LDO is shown in Fig. 1. It consists of voltage reference V_{ref}, a PMOS pass element M0, feedback network R_a and R_b, protection circuits, loading elements and an error amplifier in feedback configuration used to drive the pass element. The error amplifier compares the reference voltage V_{ref} created by a bandgap reference circuit and feedback voltage V_{FB}, and then generates a voltage error signal, which is fed to the gate of the pass transistor to change its overdrive. The change of overdrive adjusts the pass transistor current and causes the output voltage to be corrected to the proper level. If the output feedback voltage increases relative to V_{ref}, the error amplifier changes the pass transistor's output to maintain a constant output voltage (V_{OUT}). The selection of the pass element is very important when high efficiency and low dropout voltage are required. As load current specification increases, the pass transistor's size should be larger.

The associated capacitor and output resistor of the pass transistor and error amplifier are depicted as C_{gd}, C_{oa}, R_{ds} and R_{oa} respectively. Figure 1 indicates that a high output

Fig. 1. Structure of traditional LDO.

Fig. 2. Error amplifier with two stages.

Fig. 3. Schematic of the second stage of error amplifier.
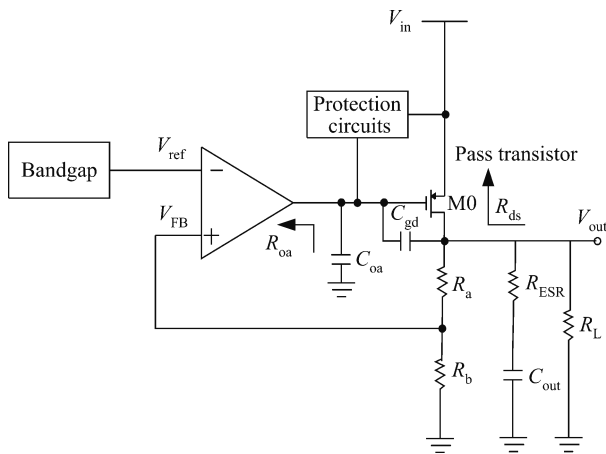
impedance of the LDO creates a low frequency pole and degenerates the phase margin of the open loop response. To understand the frequency response of the LDO, first we examine pole locations. Figure 1 shows that there are two low frequency poles that need to be taken into account. The load pole is formed by the output of the LDO and the pass transistor pole can be found at the gate of the pass transistor. The load pole ω_1 can be approximated as

$$\omega_1 \approx \frac{1}{[R_{ds}//(R_a + R_b)//R_L]C_{out}}. \qquad (1)$$

Since load varies with load current, ω_1 moves wide frequency range. Typically, a load capacitor is in the order of μF so that ω_1 is usually the first pole of the LDO. The pass transistor pole ω_2 can be approximated as

$$\omega_2 \approx \frac{1}{R_{oa}\{C_{oa} + g_{mp1}[R_{ds}//(R_a + R_b)//R_L]C_{gd}\}}, \qquad (2)$$

where g_{mp1} is the transconductance of the M0. As the maximum load current increases, the size of the pass transistor also needs to be increased. This enlarges associated capacitor C_{gd} and shifts ω_2 to the lower frequency.

Since the LDO is required to have precise output voltage and wide output current, an error amplifier with high DC gain and a wide output voltage range is a must. To meet the above-mentioned condition, a two-stage amplifier is usually used, as can be seen in Fig. 2. Therefore, an error amplifier provides an internal pole, which is usually formed by the input capacitor of the second stage. This error amplifier pole, in this paper we define as ω_3, depends on the circuit configuration.

As mentioned, there are three dominant poles in the LDO can be seen in Fig. 2. So the classical LDO suffers from a stability problem. If we can place ω_2 and ω_3 at least three times higher than unity gain frequency (UGF) of LDO, frequency response should be unconditionally stable.

2.2. Compensation of the pass transistor pole ω_2

In order to realize one pole system, first, we try to move the pass transistor pole ω_2 to a higher frequency. To increase the

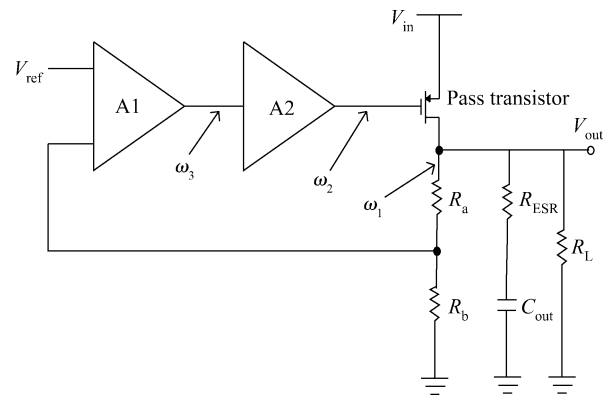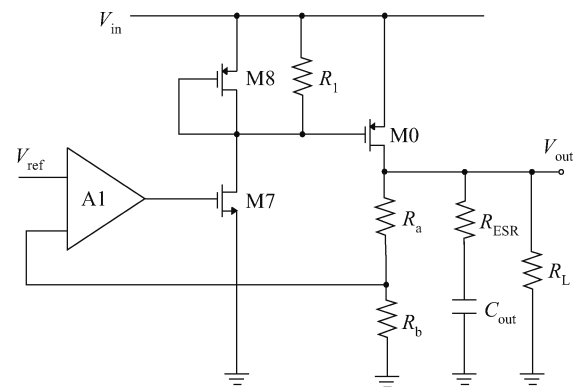maximum specification load current, the size of the pass transistor cannot be scaled-down. Thus output resistor of the error amplifier should be decreased. In Ref. [8], source follower is adapted to reduce the output resistor and the topology cannot completely turn off the pass transistor.

In this paper we choose common source stage with resistor R_1 and PMOS diode load M8 as the second stage of error amplifier is shown in Fig. 3. The output resistance of this circuit can be

$$R_{oa} = r_{ds7}//R_1//\frac{1}{g_{m8}}, \qquad (3)$$

where r_{ds} and g_m are output resistance and transconductance of MOS transistor, respectively. Thus R_{oa} is always smaller than R_1. Moreover, as the load current increases, the resistance of the PMOS diode M8 decreases. This configuration can move ω_2 to the higher frequency without increasing the quiescent current.

2.3. Pole-zero tracking frequency compensation

In this section, we examined an error amplifier pole ω_3. Note that in Fig. 2, to move ω_3 to the higher frequency, either reducing the output resistance of the first stage or scaling down the size of input capacitor of the second stage is required. However, output resistance is decided by the DC gain of the LDO and input capacitance is automatically fixed by the common source output stage circuit. Thus both parameters cannot easily be changed to modify the error amplifier pole ω_3. This results in the use of zero to achieve frequency compensation.
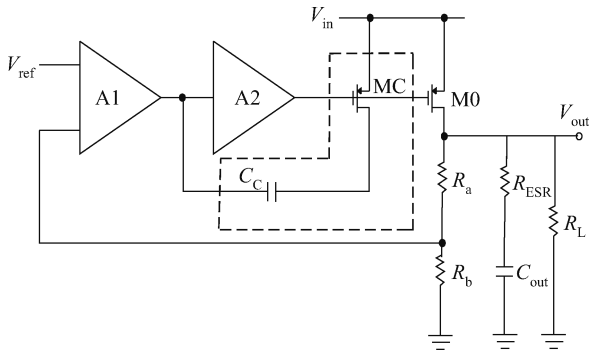
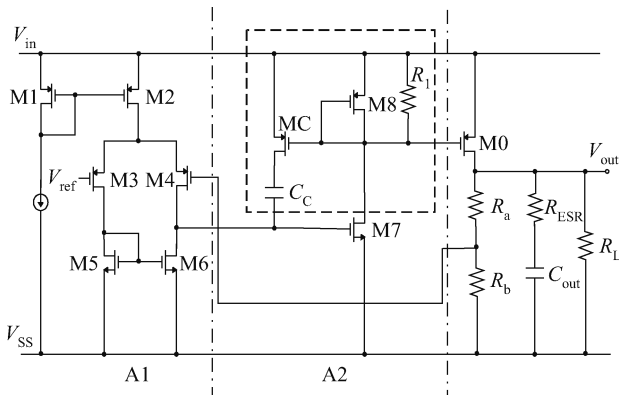Fig. 4. Schematic of the pole-zero tracking frequency compensation.

Fig. 6. Simulated loop gain of the proposed LDO.

Fig. 5. Detailed schematic of the proposed LDO.

Fig. 7. Micrograph of the proposed LDO.

There are several ways to create a zero for an LDO. Here we focus on the pole-zero tracking frequency compensation technique of an error amplifier to create a zero which is shown in the dotted frame in Fig. 4. Figure 4 shows the tracking zero is generated by a scaled mirror transistor MC operating in linear region and acting as a linear resistor R_c whose resistance value is controlled by the gate terminal[9]. Figure 5 shows the detailed compensation schematic of the proposed LDO.

An error amplifier pole ω_3 and the zero ω_Z in Fig. 5 can be approximate as[10]

$$\omega_3 \approx \frac{1}{(1 + g_{m7}r_2) r_1 C_C},\tag{4}$$

$$\omega_Z \approx \frac{1}{R_C C_C},\tag{5}$$

where $r_1 = r_{ds4} // r_{ds6}$ and r_2 are the first and second stage output resistance, respectively. From Eq. (4), we can see the pole ω_3 is controlled by the gate voltage of the pass transistor as well as output current, so the zero generated by the compensating network is tracking the output pole. At the light load, the gate–source voltage of the M8 is almost zero to turn off the pass transistor. For this reason, gate–source voltage of MC is also nearly zero and MC remains off. In spite of the relatively high gain of the second stage, ω_3 is placed at a relatively high frequency because input capacitance is only composed of the M7 and C_C is not included. As the load current of LDO increases, the gate voltage of M8 starts to decrease. Hence, if the gate–source voltage of the MC exceeds threshold voltage, MC starts to turn on and activate compensation circuit. If we
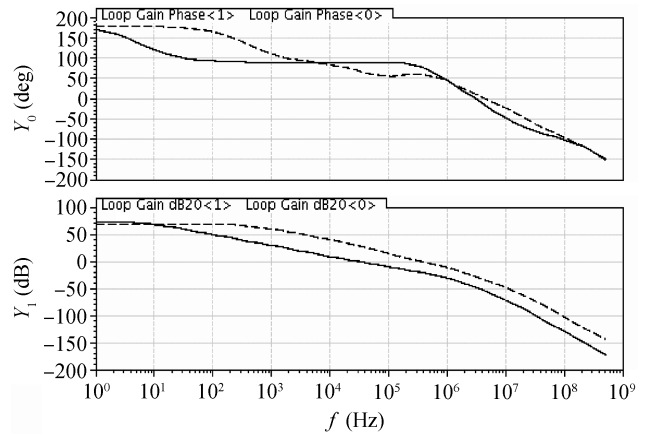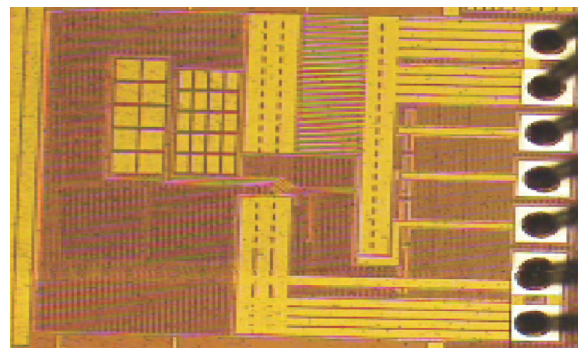
design the gain of the second stage relatively low, the Miller effect caused by C_C can be moderated. The zero is the same as the original equation in Eq. (5). When R_c and R_1 are comparable, zero can be placed just behind the second pole ω_3 thus improves the phase margin.

The simulated loop gain with an off-chip capacitor $C_{load} = 5 \mu F$ is shown in Fig. 6. Simulations are performed at light load current condition of 1 mA (solid line) and full load condition of 200 mA (dashed line). At light load condition the loop DC gain is 73.5 dB and the phase margin is 88°. At full load condition, the DC gain is 68.2 dB and the phase margin is 60°. Therefore, the proposed LDO is absolutely stable under any operational condition with an off-chip capacitor.

3. Measurement results

The proposed LDO has been implemented in HJTC 0.18 μm CMOS technology. Figure 7 shows the die micrograph of the proposed LDO, which was fabricated as part of an integrated power IC. The LDO die area is $630 \times 550 \mu m^2$. The LDO works at the input voltage of 2.8–5 V, and provides an output voltage of 1.8 V, and the LDO can deliver up to 200 mA. Figure 8 shows the measured load regulation with different temperatures of the proposed LDO. The load regulation at normal temperature is 0.15 mV/mA, and the LDO output voltage error is less than ±7.5 mV over the full temperatures and full load currents. When the input voltage changes from 2.8 to 5 V, the line regulation is shown in Fig. 9 with load
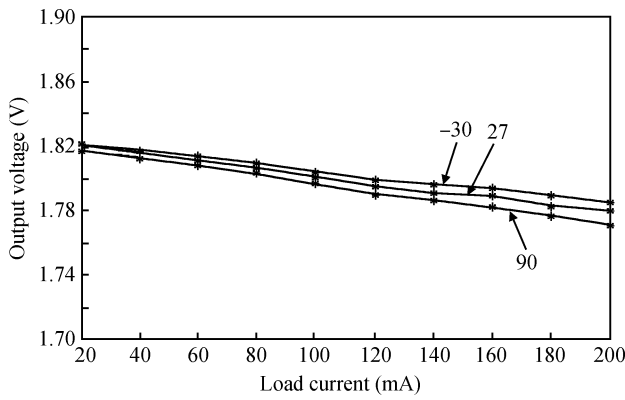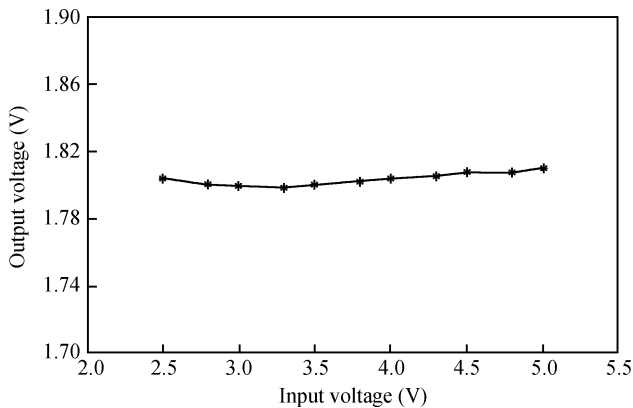
Fig. 8. Measured LDO load regulation.

Fig. 9. Measured LDO line regulation with 100 mA load current.

(a) Load transient response

(b) Up time

(c) Down time

Fig. 10. Measured LDO load transient response.

current is 100 mA. The total error of the output voltage due to line and load variations is less than 0.015%. Furthermore, when the LDO input voltage changes from 2.8 to 5.5 V, the measured line regulation is also ±2.25 mV/V. This is due to the high loop gain provided by the two high gain stages.

In order to verify the stability of the LDO, the load transient response is measured and shown in Fig. 10. When the load current is pulsating between 1 and 200 mA, the LDO provides less than 50 μs settling time and less than 20 mV overshoots and undershoots. By incorporating the proposed two stage error amplifier and the pole-zero tracking frequency compensation technique, the LDO linear regulator operates with fast transient response without any instability.
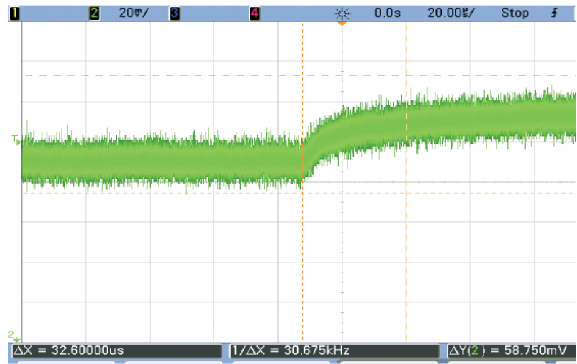
These advantages are due to the advanced frequency compensation scheme and sufficient phase margin of the open-loop response. Compared with other LDO frequency compensation methods, this work has a sufficient UGF and a suitable phase margin. Consequently, the presented LDO provides a fast dynamic response and excellent stability. The comparisons show that the design methods of the error amplifier and the proposed frequency compensation are beneficial for improving the performances of an LDO. Table 1 summarizes the performance of the proposed LDO. The quiescent current of the LDO is 130 μA over all load currents.

Figure 11 shows start-up time of the proposed LDO regulator for load current of 100 mA. The start-time is about 2.23 ms (include equipment start-up time).
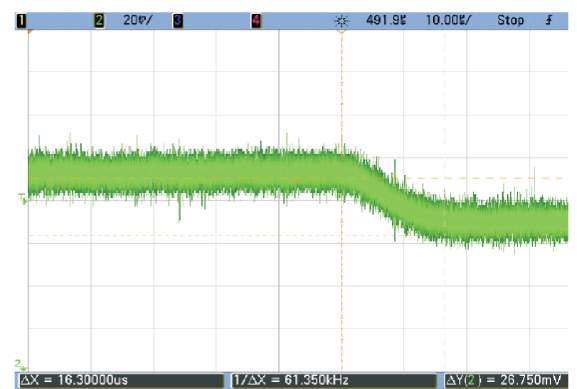
In order to provide a clearer picture of the performance

Table 1. Summary of the proposed LDO measured performances.

Parameter	Value
Technology	HJTC 0.18 μm CMOS
Chip area	630×550 μm^2
Input voltage	2.8–5 V
Output voltage	1.8 V
Line regulation	±2.25 mV/V
Line variation	0.005%
Load regulation	±0.075 mV/mA
Load variation	0.015%
Maximum output current	200 mA
Quiescent current	130 μA

improvement in the proposed LDO resulting from the double frequency compensation techniques, a comparison of the proposed LDO regulator with some reported LDOs is given in Ta-

Table 2. LDO performances comparison.

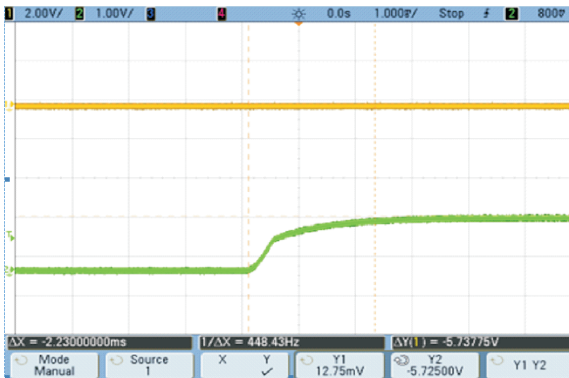| Year	2007[5]	2008[7]	2009[11]	2011[6]	This work
Technology (μm)	0.35	0.35	0.18	0.35	0.18
Chip area (mm^2)	0.264	0.409	—	0.463	0.346
Input voltage (V)	2–5.5	2–3.6	3–5.5	2.2–3.3	2.8–5
Output voltage (V)	1.8	1.8	1.8	2	1.8
Load regulation (mV/mA)	0.17	0.7	0.448	0.3	0.15
Settling (μs)	—	5 (0–100 mA)	2 (1–100 mA)	8	< 50 (1–200 mA)
Maximum output current (mA)	200	150	125	200	200
Quiescent current (μA)	340	27	150	60	130

Fig. 11. Measured start-up time for a load current of 100 mA.

ble 2. From Table 2, the proposed LDO achieves the smaller chip area, the moderate quiescent current consumption and the best load regulation characteristic compared with other reported LDOs.

4. Conclusion

In this paper, a 200 mA low-dropout linear regulator has been designed and implemented. Based on double frequency compensation techniques, the LDO achieves only a single pole within the unity-gain bandwidth of the regulation loop and a good phase margin with a small compensation capacitor. Experimental results show that the proposed LDO achieves fast load and line transient responses, small overshoots and undershoots, and excellent line and load regulations. The proposed LDO is suitable for low voltage, low power consumption and system on chip application due to its excellent stability.

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