Design of a 0.5 V CMOS cascode low noise amplifier for multi-gigahertz applications*

Liu Baohong(刘宝宏)[1,†], Zhou Jianjun(周健军)[2], and Mao Junfa(毛军发)[1]

[1]Center for Microwave and RF Technologies, Shanghai Jiao Tong University, Shanghai 200240, China
[2]Center for Analog/RF Integrated Circuits, Shanghai Jiao Tong University, Shanghai 200240, China

Abstract: This paper presents the design of 0.5 V multi-gigahertz cascode CMOS LNA for low power wireless communication. By splitting the direct current through conventional cascode topology, the constraint of stacking-MOS structure for supply voltage has been removed and based on forward-body-bias technology, the circuit can operate at 0.5 V supply voltage. Design details and RF characteristics have been investigated in this paper. To verify the investigation, a 0.5 V 5.4 GHz LNA has been fabricated through 0.18 μm CMOS technology and measured. Measured results show that it obtains 9.1 dB gain, 3 dB NF with 0.5 V voltage and 2.5 mW power dissipation. The measured IIP_3 is –3.5 dBm. Compared with previously published cascode LNA, it achieves the lowest supply voltage and lowest power dissipation with competitive RF performances.

Key words: CMOS; 0.5 V; cascode low noise amplifier; direct current split; forward-body-bias technology; multi-gigahertz applications

DOI: 10.1088/1674-4926/33/1/015006 **EEACC:** 2570

1. Introduction

With the coming nanoscale CMOS era, 0.5 V devices have become the hot area for the circuit design and 0.5 V is predicted to be technique node for the next generation of low power communication systems[1−3]. For circuits operated at 0.5 V supply, the evident advantage is the reduction of power dissipation due to the quadratic relationship between supply voltage and power dissipation. Even though the shrinking feature size of MOSFETs provides the possibility of lowering the supply voltage, its threshold voltage (V_{th}) still imposes difficulties on operating at 0.5 V supply since the downscaling rate of V_{th} is further slower than that of MOS feature size, which also results in slow development of 0.5 V radio frequency (RF) CMOS circuits.

In addition, the high data-rate requirement for wireless communication has motivated RF carrier moving toward multi-gigahertz and even tens-gigahertz due to its large capability advantages, such as long term evolution (LTE, 900 MHz–3 GHz), wireless local area networks 802.11 (WLAN 802.11, 2.4 GHz, 5 GHz) and X-band frequency modulation continuous wave (FMCW) radar. For these multi-gigahertz applications, low power dissipation is important as well as their performances. As a crucial component of wireless transceiver, the low noise amplifier (LNA) is generally required to have appropriate gain, low noise figure (NF) and good linearity as well as low power dissipation. Although there were many published LNA works known as non-cascode topology at or below 0.5 V[4,5], their poor NF characteristic restricts their application to use in only some special areas where lower power dissipation is pursued at the cost of NF and linearity. Cascode LNA is widely used due to its low noise and good isolation. However, it is difficult to be operated as low as 0.5 V because of constraints of its stacking structure and the threshold voltage (V_{th}). Even though the folded-cascode topology can be used for low voltage, the lower transit frequency (f_t) of PMOS has imposed constraint on the multi-gigahertz application when compared with NMOS, which compels more advanced technology and higher voltage to be used for appropriate RF characteristics. In this paper, a 0.5 V multi-gigahertz cascode LNA is proposed with full NMOS. It's followed to the authors' previous work of Ref. [6] and concentrated on the investigation of much lower voltage design and the verification circuit has also been successfully fabricated through 0.18 μm standard CMOS technology. Although the investigation and fabrication are respectively focused on 5 GHz and 0.18 μm CMOS technology, these developed techniques and design guidelines can also be applied to the other multi-gigahertz wireless communication methods mentioned above and is available for more advanced process technology.

2. Proposed 0.5 V cascode LNA

The conventional cascode topology LNA is shown in Fig. 1. For this kind topology, the second stage (common gate stage, CG) can reduce the Miller effects between input and output terminals, which results in good isolation between them. However, since two MOSFETs are stacked, the supply voltage will be constrained into high voltage[4].

To remove above supply constraint of conventional cascode LNA, the proposed cascode one is illustrated in Fig. 2. Unlike the conventional cascode LNA shown in Fig. 1, C_4, L_4 and L_5 are added to split DC and both NMOS bulks are connected to positive potential rather than to source terminal or ground in the conventional case.

* Project supported by the National Science Fund for Creative Research Groups of China (No. 60821062) and the National Basic Research Program of China (No. 2009CB320202).

† Corresponding author. Email: bhliu2006@gmail.com

Received 1 June 2011, revised manuscript received 29 July 2011

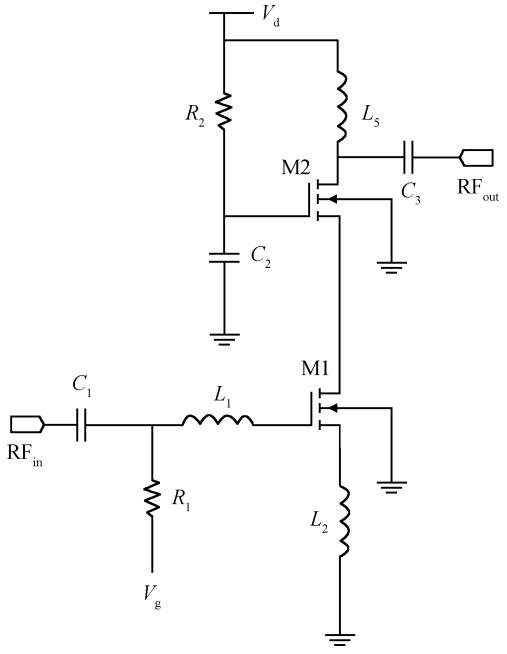

Fig. 1. Conventional cascode LNA schematic.

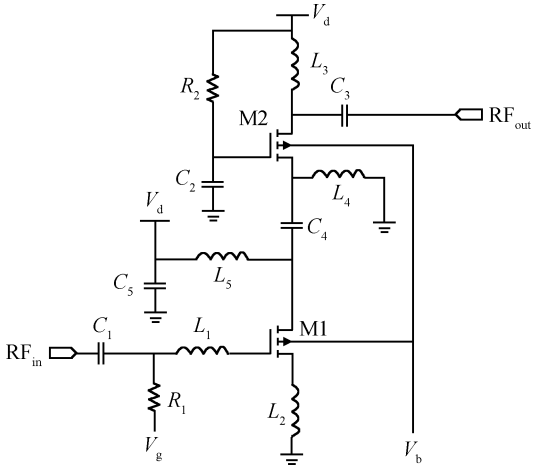

Fig. 2. Proposed ultra-low voltage cascode LNA.

2.1. Supply voltage reduction

2.1.1. DC split for removing the limitation of stacking structure

In Fig. 2, C_4 is series in DC path of traditional cascode for blocking DC while RF is allowed to pass through. To provide the proper supply voltage to M1 and M2, inductors L_5 and L_4 are respectively added between supply and ground to provide DC path. At the same time, they operate as an RF load.

By using the additional capacitor and inductors, the constraint of stacking overdrive voltages in Eq. (1) is removed and the minimum drain voltage is shown as follows:

$$V_{\text{di\_min}} = V_{\text{gsi}} - V_{\text{thi}}. \tag{1}$$

From Eq. (1), it is seen that the intrinsic limitation of the cascode LNA from the stacking structure has been removed. With only one V_{th} constraint, the supply voltage can be degraded. It should be noted that in practical circuit design, the drain voltage is generally set same as the gate voltage for simplifying the supply.

2.1.2. Forward body bias technology for threshold reduction

It's well known that V_{th} can be manipulated by the bias voltage, shown as follows:

$$V_{\text{th}} = V_{\text{th0}} + \gamma\left(\sqrt{|2\phi_{\text{F}} - V_{\text{bs}}|} - \sqrt{|2\phi_{\text{F}}|}\right), \tag{2}$$

where V_{bs} is the bulk-source potential difference, V_{th0} is the threshold voltage with zero V_{bs}, γ denotes the body effect coefficient and ϕ_{F} is the Fermi potential.

Equation (2) illustrates that a positive V_{bs} of NMOS will decrease V_{th}. Depending on active electrode on bulk terminal, body biasing strategy is introduced to adjust V_{th}, known as a dynamic threshold voltage MOSFET (DTMOS)[7]. Through deep-n-well technology, the substrate bias can be set to a positive potential known as forward-body-bias (FBB) technology. With FBB technology, V_{th} has been decreased and the reduction of supply voltage is possible. Based on the simulation through 0.18 μm CMOS technology, V_{th} of M1 and M2 will change from 0.52 V at zero V_{bs} to 0.42 V at 0.5 V V_{bs}. The reduced V_{th} provides the enough voltage headroom for 0.5 V applications.

2.2. RF characteristics analysis

In Section 2.1, the supply voltage is reduced by DC split and FBB technologies. In the following, the proposed circuit's RF characteristics will be investigated.

2.2.1. Gain

Figure 3 shows the small-signal equivalence for the circuit, where the bulk-source conductance and C_{gd} are disregarded for simplification, and G_{O1} and G_{O2} respectively demonstrate output conductance of M1 and M2. To get maximum output power at load, the following equation should be satisfied:

$$Z_{\text{IN}} = Z_{\text{S}}^*, \tag{3}$$

$$Z_{\text{OUT}} = R_{\text{LOAD}}, \tag{4}$$

$$Y_{\text{O1}}^* = Y_{\text{I2}}, \tag{5}$$

where Z and Y demonstrate impedance and admittance, respectively.

For LNA, its gain is tightly determined by its total effective transconductance. Typically, the equivalent transconductance of the first stage with input matching network is derived[8]:

$$G_{\text{m}} = \frac{I_1}{V_{\text{in}}} \approx g_{\text{m1}} Q_{\text{in}} = \frac{g_{\text{m1}}}{2\omega_0 R_{\text{s}} C_{\text{gs1}}}, \tag{6}$$

where Q_{in} is effective quality factor of input matching network, g_{m1} is M1 transconductance, ω_0 is operating angle-frequency, R_{s} is source resistance, and C_{gs1} is M1 gate–source capacitance

Assuming that Eq. (5) is satisfied, the current gain by CG stage with the inter-stage matching network can be gotten as follows:

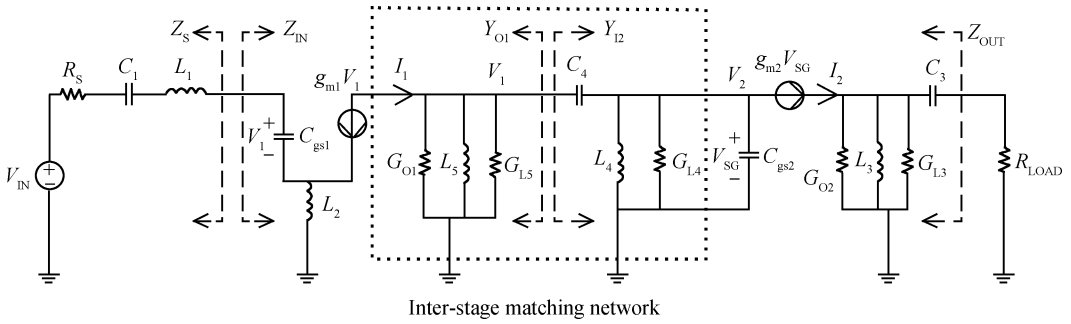

Fig. 3. Equivalent circuit of the proposed circuit.

$$A_{\text{int}} = \frac{I_2}{I_1} = \frac{1}{G_{\text{O1}} + G_{\text{L5}} + \dfrac{\omega^4 (G_{\text{L4}} + g_{\text{m2}})}{\left(\omega^2 - \omega_{\text{C4}}^2\right)^2 + \omega^2 L_4^2 \omega_{\text{C4}}^4 (G_{\text{L4}} + g_{\text{m2}})^2}} \times \frac{\omega C_4 g_{\text{m2}}}{\sqrt{\left(\omega C_4 + \omega C_{\text{gs2}} - 1/(\omega L_4)\right)^2 + (G_{\text{L4}} + g_{\text{m2}})^2}}, \tag{7}$$

where $\omega_{\text{C4}} = \frac{1}{\sqrt{L_4 C_4}}$, I_1, I_2 are M1, M2 output currents, respectively, ω is the operating angle frequency, G_{L4} and G_{L5} are parallel conductance of L_4 and L_5, respectively. g_{m2} is the transconductance of M2.

Depending on Eqs. (6) and (7), the total transconductance of the proposed circuit can be obtained:

$$G_{\text{T}} = \frac{I_2}{V_{\text{in}}} = G_{\text{m}} A_{\text{int}}. \tag{8}$$

In Eq. (8), it is seen that the total effective transconductance gets contributions from the CS stage with the input matching network and the CG stage with the inter-stage matching network. For first term, the parameters of Eq. (6) are easily determined by using published approaches[8, 9]. The second term is from the inter-stage matching network and CG stage, which are determined by L_4, L_5, C_4 and M2. The CG stage is easily determined according to the trade-off between isolation and current. So the remaining factor is to determine the inter-stage matching network to get the maximum current at the M2 drain terminal. From Eq. (7), it may be seen that A_{int} is very complicated and its maximum value depended on L_4 and C_4. To get their values efficiently, theoretical values of A_{int} obtained from a Matlab simulation for given values of G_{L5}, C_{gs2}, g_{m2} and different values of L_4 and C_4 are shown in Fig. 4.

As seen from Fig. 4, the gain varies with different L_4 and C_4. Its peak values are close to low capacitance (around 0.5 pF) or low inductance (around 0.3 nH). In the domain of low inductance or low capacitance, the gain is very sensitive to component accuracy, which means the value's offset will result in a steep drop of gain. It may also be seen that there is a flat area when the L_4 value is larger than 2 nH. This flat area provides reliability for circuit design due to insensitive gain to the device accuracy. In our circuit, the designed point for L_4 and C_4

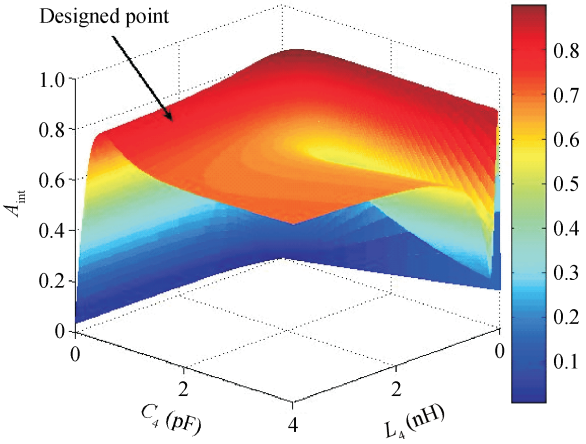

Fig. 4. Variation of current gain with different C_4 and L_4.

is chosen at the flat area rather than the peak for reliability, as shown in Fig. 4. The gain difference between the peak and the designed point is simulated to be at about 0.2 dB. Once L_4 and C_4 are determined, L_5 is easily determined according to Eq. (5). It should be noted that the peak of A_{int} is less than unity. This loss is from the output conductance of M1 rather than from the inter-stage matching network since it is not negligible in multi-gigahertz operating frequency.

2.2.2. Noise figure

It is generally required that LNA obtains noise matching for the minimum NF. In the proposed LNA, the inductive source degeneration is adapted for noise and gain matching. The input impedance and source impedance in Fig. 3 can be obtained[8]:

$$Z_{\text{in}} = \text{j}\omega L_2 + \frac{1}{\text{j}\omega C_{\text{gs1}}} + \frac{g_{\text{m1}}}{C_{\text{gs1}}} L_2, \tag{9}$$

$$Z_{\text{S}} = \text{j}\omega L_1 + \frac{1}{\text{j}\omega C_1} + R_{\text{s}}. \tag{10}$$

According to Eq. (4), the following equations will be satisfied to transfer maximum power:

$$\omega (L_1 + L_2) = \frac{1}{\omega} \left(\frac{1}{C_{\text{gs1}}} + \frac{1}{C_1} \right), \tag{11}$$

$$\frac{g_{\text{m1}}}{C_{\text{gs1}}} L_2 = R_{\text{s}}. \tag{12}$$

On the other side, noise parameters of the first stage can be obtained[9]:

$$Z_{\text{opt}} = \frac{1}{\omega C_{\text{gs1}}} \frac{\alpha\sqrt{\dfrac{\delta\left(1-|c|^2\right)}{5\gamma}} + \text{j}\left(1+\alpha\,|c|\,\sqrt{\delta/5\gamma}\right)}{\dfrac{\alpha^2\delta\left(1-|c|^2\right)}{5\gamma} + \left(1+\alpha\,|c|\,\sqrt{\delta/5\gamma}\right)^2} - \text{j}\omega L_2, \tag{13}$$

$$F_{\min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_{\text{T}}}\sqrt{\gamma\delta\left(1-|c|^2\right)}, \tag{14}$$

where all parameters are same as those in Ref. [9].

To get noise match in the input terminal, following equation has to be satisfied:

$$g_{\text{m1}}L_2 = \frac{1}{\omega}\frac{\alpha\sqrt{\dfrac{\delta\left(1-|c|^2\right)}{5\gamma}}}{\dfrac{\alpha^2\delta\left(1-|c|^2\right)}{5\gamma} + \left(1+\alpha\,|c|\,\sqrt{\delta/5\gamma}\right)^2}. \tag{15}$$

With Eqs. (11), (12), (15) and properly choosing device parameters, the designed LNA will get the minimum NF with the maximum power transferring simultaneously. However, it is specially noted that with 0.5 V supply voltage the transit angle-frequency ω_{T} will severely degrade compared with conventional high voltage cascode LNA, which results in the increase of $F_{\min}$ due to their inversely proportional relation in Eq. (14).

2.2.3. Linearity

For multi-gigahertz cascode LNA, the CG stage produces the signal distortion by its gate-source capacitance[10]. That means if C_{gs} effects on linearity has been removed CG has little deterioration on the linearity. In our proposed circuit, CG's gate–source capacitance has been resonated by the inter-stage matching network and the first stage contributes the linearity.

Considering mobility degradation of short-channel MOS, the drain current is obtained[11]:

$$i_{\text{ds}} = \frac{\mu_{\text{n}}C_{\text{OX}}}{2}\frac{W}{L}\frac{\left(V_{\text{gs}}-V_{\text{th}}+v_{\text{gs}}\right)^2}{1+\theta\left(V_{\text{gs}}-V_{\text{th}}+v_{\text{gs}}\right)}, \tag{16}$$

where μ_{n} is the carrier mobility, C_{OX} is capacitance per unit area, W, L are respectively MOS width and length, v_{gs} is input alternating voltage at gate–source terminal, and θ is the normal-field mobility degradation factor.

On the other side, the drain current can also be expressed as follows up to the third order:

$$i_{\text{ds}} \approx I_{\text{DC}} + g_{\text{m1}}v_{\text{gs}} + g_2v_{\text{gs}}^2 + g_3v_{\text{gs}}^3, \tag{17}$$

where I_{DC} is the direct current through M1, and g_2, g_3 are the first and the second derivative ratio of drain current to gate–source voltage, respectively.

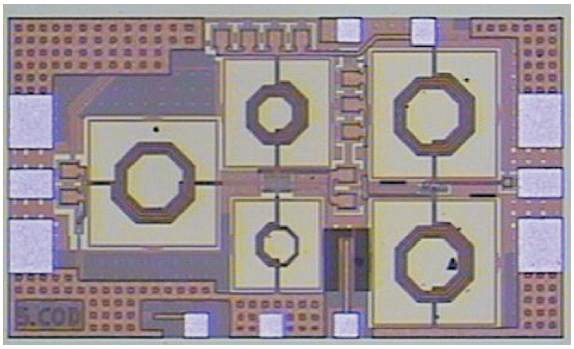

Fig. 5. Die micrograph of proposed LNA.

Based on Eqs. (16) and (17), g_{m1} and g_3 can be derived as follows:

$$g_{\text{m1}} = \frac{\partial i_{\text{ds}}}{\partial v_{\text{gs}}} = \frac{\mu_{\text{n}}C_{\text{OX}}}{2}\frac{W}{L}\frac{\left(V_{\text{gs}}-V_{\text{th}}\right)\left[2+\theta\left(V_{\text{gs}}-V_{\text{th}}\right)\right]}{2\left[1+\theta\left(V_{\text{gs}}-V_{\text{th}}\right)\right]^2}, \tag{18}$$

$$g_3 = \frac{1}{3!}\frac{\partial^3 i_{\text{ds}}}{\partial v_{\text{gs}}^3} = -\frac{\mu_{\text{n}}C_{\text{OX}}}{2}\frac{W}{L}\frac{\theta}{2\left[1+\theta\left(V_{\text{gs}}-V_{\text{th}}\right)\right]^4}. \tag{19}$$

Then IIP_3 can be obtained[11]:

$$\text{IIP}_3 = \frac{2}{3\cdot\text{Re}\left(Z_{\text{IN}}\right)}\frac{g_{\text{m1}}}{g_3} = \frac{2}{3\cdot\text{Re}\left(Z_{\text{IN}}\right)\cdot\theta}\left(V_{\text{gs}}-V_{\text{th}}\right) \times\left[2+\theta\left(V_{\text{gs}}-V_{\text{th}}\right)\right]\left[1+\theta\left(V_{\text{gs}}-V_{\text{th}}\right)\right]^2. \tag{20}$$

From Eq. (20) it can be seen that IIP_3 is determined once the overdrive voltage is fixed. However, it is noted that the above equation is only available to crudely evaluate IIP_3 since θ is different with different processes. For this reason, Eq. (20) is generally used to estimate IIP_3 at the beginning of circuit design.

3. Circuit verification and experimental results

To verify the investigation, the proposed LNA is designed to operate at 5.4 GHz for WLAN application where LNA requires low NF, proper gain and linearity[12]. It is designed through TSMC CMOS 0.18 μm technology. The input matching network is designed for simultaneous impedance and noise matching while the output terminal is matched for 50 Ω. M1 and M2 channel widths are respectively chosen to 180 μm and 90 μm for the trade-off between current consumption and RF performances. C_4, L_4 and L_5 are determined according to the gain analysis in Section 2. C_1 is used to block DC and C_2, C_5 are large enough for the goal of RF ground to reduce the parasitic parameter effect. R_1 and R_2 are large enough for gate bias and RF choke. In the layout design, all interconnection lines are modelled by electromagnetic software ADS-momentum for parasitic parameters extraction. All extracted parameters are fed into the post-layout-simulation to reduce discrepancies between simulation and measurement. To reduce substrate influence, test pads are fabricated on shielded ground with metal 1. All elements in Fig. 2 are implemented on chip. The chip area is

Table 1. Comparison between this work and published CMOS cascode LNAs and 0.5-V LNA.

Parameter	Technology (μm)	Frequency (GHz)	Supply (V)	P_d (mW)	S_{21} (dB)	NF (dB)	IIP3 (dBm)	Year
This work	0.18	5.4	0.5	2.5	9.1	3	–3.5	—
Ref. [10]	0.24	2.2	1.8	16.2[a]	8.6	1.92	–2.55	2008
Ref. [12]	0.24	5.2	2	10	10	3	0.4	2005
Ref. [13]	0.09	5.5	1	8	13	1.8	–2.6	2007
Ref. [14]	0.18	5.7	1.8	4	11.45	3.4	—	2006
Ref. [15[b]]	0.09	2.4	0.6	3	15[c]	3	–7	2010
Ref. [16]	0.18	5.25	0.5	2.5	13.9[c]	6	2.8	2005
Ref. [4]	0.18	5.1	0.4	1.03	10.3	5.3	—	2007
Ref. [3]	0.18	8.9	0.5	4	9.1	5	–8.5	2011

[a]power dissipation of differential structure. [b]simulation results. [c]voltage gain.

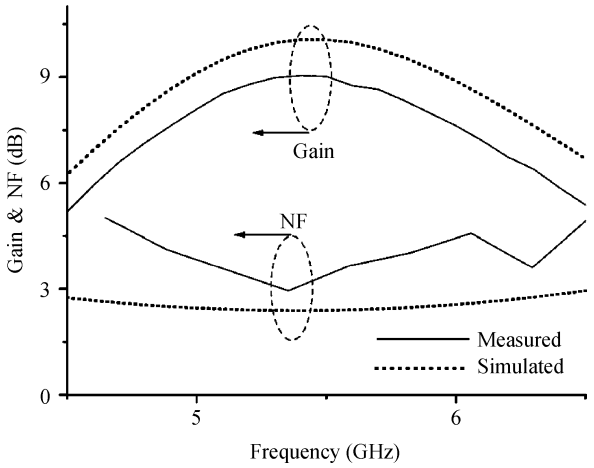

Fig. 6. Measured and simulated gain and NF.

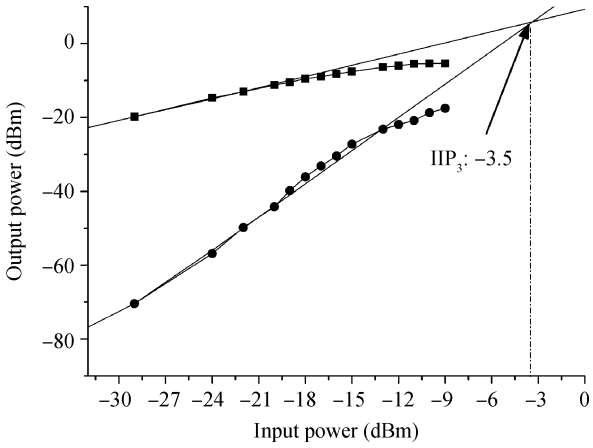

Fig. 8. Measured input 3rd-order intercept point.

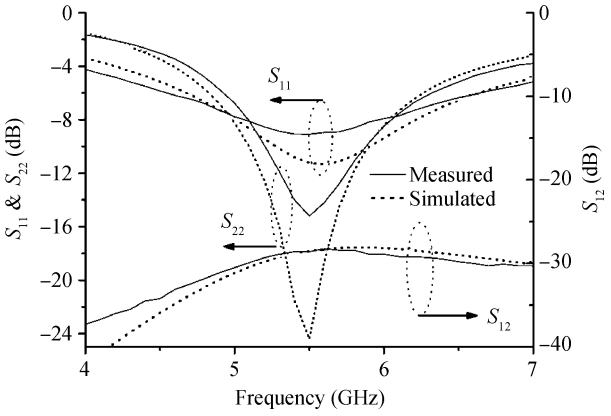

Fig. 7. Measured and simulated S_{11}, S_{12} and S_{22}.

1.11×0.64 mm^2 including all test pads. Figure 5 demonstrates the chip micrograph.

Performances are measured on-wafer by Cascade Corp. probes and Agilent microwave measurement instruments. All supply voltages are provided by DC probes. Measured gain (S_{21}) and NF are plotted in Fig. 6. It can be seen that the LNA has 9.1 dB gain and 3 dB NF at the operating frequency of 5.4 GHz. Input, output return losses and reverse isolation are plotted in Fig. 7 with values of –9.1 dB, –14 dB and –28.6 dB, respectively. At the same time, simulated S-parameters and NF are also plotted in Figs. 6 and 7. The post-layout-simulation gain is 10.1 dB and NF is 2.6 dB. The measured results coincide with simulation. Slight differences are mainly produced by the inaccurate modelling of NMOS with FBB and passive components. In Fig. 8, IIP_3 are plotted. IIP_3 is –3.5 dBm. The whole circuit operates at 0.5 V supply voltage with around 5 mA current consumption.

The measured results of this fabricated LNA and those published CMOS cascode LNA are summarized in Table I for comparison. The proposed LNA has the lowest supply voltage, the lower power dissipation in all cascode LNA while RF characteristics are competitive. At the same time, non-cascode LNA with no more than 0.5 V supply voltage are also summarized in Table 1, known as Refs. [16, 4, 3]. Even though these non-cascode LNA can get lower power dissipation, for an instant[4], their NF are as high as 5.3 dB, which imposes crucial constraints on their applications in WLAN[12]. The verification results show its great potential for the coming 0.5 V nanoscale CMOS era.

4. Conclusion

In this paper, design of 0.5 V cascode LNA for multi-gigahertz application is presented. By utilizing DC split and FBB technology, the supply voltage of cascode LNA can be reduced to 0.5 V and the power dissipation is degraded. The design detail and RF characteristics have been investigated. A 5.4 GHz verified circuit shows that it gets 9.1 dB gain, 3 dB NF

and –3.5 dBm IIP_3 at 0.5 V supply. It gets the lowest supply voltage and the lowest power dissipation with competitive RF performances compared with other published cascode LNAs. It is very suitable for ultra-low voltage and low noise applications.

References

[1] Itoh H. Adaptive circuits for the 0.5-V nanoscale CMOS era. IEEE ISSCC, 2009: 14

[2] Chatterjee S, Tsividis Y, Kinget P. 0.5-V analog circuit techniques and their application in OTA and filter design. IEEE J Solid-State Circuits, 2005, 40(12): 2373

[3] Liu B, Zhou J, Mao J. A fully integrated low voltage (0.5 V) X-band CMOS low noise amplifier. Microw Opt Technol Lett, 2011, 53(1): 17

[4] Wu D, Huang R, Wang W, et al. A 0.4-V low noise amplifier using forward body bias technology for 5 GHz application. IEEE Microwave and Wireless Components Letters, 2007, 17(7): 543

[5] Kargaran E, Kazemi M. Design of 0.5 V, 450 μW CMOS LNA using current reuse and forward body bias technique. 5th European Conference on Circuits and Systems for Communications, 2010: 93

[6] Liu B, Mao J. A low-voltage 5.4 GHz monolithic cascode LNA using 0.18 μm CMOS technology. Microwave and Optical Technology Letters, 2011, 53(2): 368

[7] Wann C, Harrington H, Mih R, et al. CMOS with active well bias for low-power and RF/analog applications. IEEE VLSI Symp, 2000: 158

[8] Shaeffer D K, Lee T H. A 1.5-V, 1.5-GHz CMOS low noise amplifier. IEEE J Solid-State Circuits, 1997, 32(5): 745

[9] Nguyen T K, Kim C H, Ihm G J, et al. CMOS low-noise amplifier design optimization techniques. IEEE Trans Microw Theory Tech, 2004, 52(5): 1433

[10] Fan X, Zhang H, Sanchez-Sinencio E. A noise reduction and linearity improvement technique for a differential cascode LNA. IEEE J Solid-State Circuits, 2008, 43(3): 588

[11] Lee T. The design of CMOS radio frequency integrated circuit. Cambridge, UK: Cambridge University Press, 1998

[12] Chiu H, Lu S, Lin Y. A 2.17 dB NF 5-GHz-band monolithic CMOS LNA with 10-mW DC power consumption. IEEE Trans Microw Theory Tech, 2005, 53(3): 813

[13] Duster J, Taylor S, Zhan J. A 1.5 dB NF, 5.8 GHz low-noise amplifier with on-chip matching. IEEE Asia Solid-State Circuits Conference, 2007: 99

[14] Asgaran S, Deen M, Chen C. A 4-mW monolithic CMOS LNA at 5.7 GHz with the gate resistance used for input matching. IEEE Microwave and Wireless Components Letters, 2006, 16(4): 188

[15] Balankutty A, Yu S A, Feng Y P, et al. A 0.6-V zero-IF/low-IF receiver with integrated fractional-N synthesizer for 2.4-GHz ISM-band applications. IEEE J Solid-State Circuits, 2010, 45(3): 538

[16] Hyvonen S, Bhatia K, Rosenbaum E. An ESD-protected, 2.45/5.25-GHz dual-band CMOS LNA with series LC loads and a 0.5-V supply. IEEE RFIC Symp, 2005: 43