A high dynamic range linear RF power detector with a preceding LNA*

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Abstract: A design of high dynamic range linear radio frequency power detector (PD), aimed for transmitter carrier leakage suppression is presented in this paper. Based on the logarithmic amplifier principle, this detector utilizes the successive detection method to achieve a high dynamic range in the radio frequency band. In order to increase sensitivity, a low noise amplifier (LNA) is placed in the front of this detector. DC coupling is adopted in this architecture to reduce parasitics and save area, but this will unavoidably cause DC offsets in the circuit which are detrimental to the dynamic range. So a DC offset cancelling (DCOC) technique is proposed to solve the problem. Finally, this detector was fabricated in the SMIC 0.13 μm CMOS process. The measured results show that it achieves a wide dynamic range of 50 dB/40 dB with log errors in $\pm$1 dB at 900 MHz/2 GHz, while draws 16 mA from a 1.5 V power supply. The active chip area is 0.27×0.67 mm^2.

Key words: logarithmic amplifier; successive detection; low noise amplifier (LNA); DC offset cancelling (DCOC); power detector (PD)

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1. Introduction

Direct conversion transmitters (DCTs) have drawn an ever-increasing attention in the wireless industry due to their simplicity, high integration and low cost[1−3]. However, the carrier leakage problem often poses a big challenge for applications where a wide dynamic range of gain control is needed, such as wideband code division multiple access (WCDMA) and time division-synchronous code division multiple access (TD-SCDMA). Since the carrier leakage only depends on offsets and matching and does not scale down with the output signal when the gain is scaling down, the signal-to-carrier leakage ratio will hardly be maintained. At lower gains, the power of carrier leakage may exceed the signal power causing error vector magnitude (EVM) to violate the limitation. Therefore, a special carrier leakage suppression technique is often needed for the DCT architecture. One usual approach is to use a calibration loop to suppress the carrier leakage signal, as displayed in Fig. 1[4, 5]. This loop is mainly composed of a PD and a calibration algorithm. The function of the PD is to detect the carrier leakage signal power level, and the calibration algorithm is designed to control the calibration circuits to generate a compensation factor for counteracting the sources causing the leakage and finally force the carrier leakage power level to the lowest. So it is the performance of the PD which determines the effectiveness of the whole calibration scheme.

In this paper, a PD targeted for DCT carrier leakage suppression is introduced. Based on the piecewise linear approximation logarithmic amplifier, this detector reaches high dynamic range and good accuracy up to high frequencies.

2. Architecture considerations

In a real PD, the minimum detectable power is determined by the noise, because the PD cannot tell the signal from noises. If the equivalent input noise voltage is $V_{\rm n}$ (nV/$\sqrt{\rm Hz}$), the minimum power that can be detected could be calculated as

$$P_{\rm n}|_{\rm dBm} = 10\lg\left[\int_0^{\infty} \frac{V_{\rm n}^2(f)}{R_{\rm S}}{\rm d}f\right] + 30. \quad (1)$$

Here constant 30 is the conversion ratio for dBm and $R_{\rm S}$ is the source impedance of 50 Ω. Equation (1) can be replaced by Eq. (2), if an equivalent input noise bandwidth $\rm BW_n$ is defined,

$$P_{\rm n}|_{\rm dBm} = 10\lg\left(\frac{V_{\rm n}^2}{R_{\rm S}}{\rm BW_n}\right) + 30. \quad (2)$$

So, for a PD with an equivalent input noise of 2.5 nV/$\sqrt{\rm Hz}$ and a $\rm BW_n$ of 2 GHz, the equivalent input power is –66 dBm. If a much smaller power needs to be detected, one effective way is to add a LNA ahead of the PD. Assume the input noises for LNA and PD are $V_{\rm n,\,LNA}$ and $V_{\rm n,\,PD}$ respectively and the dB

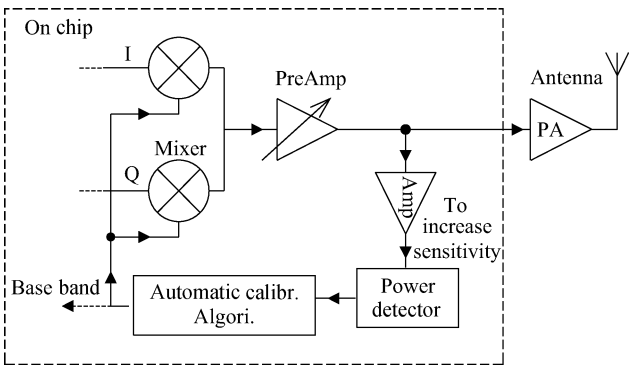

Fig. 1. Power detector used for DCT carrier leakage suppression.

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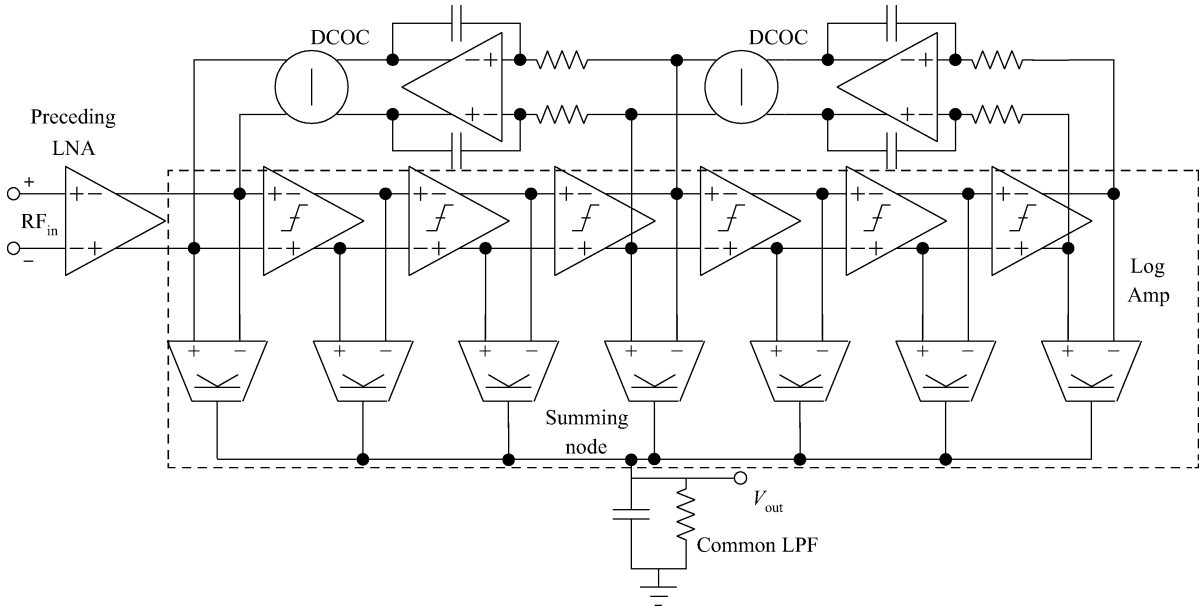

Fig. 2. Power detector architecture.

gain of LNA is A, thus the input noise power with the same $\mathrm{BW_n}$ is

$$P_{\mathrm{n1}}|_{\mathrm{dBm}} = 10\lg\left(\frac{V_{\mathrm{n,LNA}}^2 A^2 + V_{\mathrm{n,PD}}^2}{R_{\mathrm{S}}}\mathrm{BW_n}\right) + 30 - A. \quad (3)$$

Therefore, the difference between Eq. (2) and Eq. (3) is

$$\Delta P = A - \mathrm{NF_{LNA}}. \quad (4)$$

For an LNA with noise figure (NF) of 2 dB and gain of 26 dB, the improved power sensitivity is about 24 dB.

Figure 2 shows the whole block diagram of the proposed detector. It is based on a logarithmic amplifier which mainly consists of six limiting amplifiers, seven rectifiers and one low pass filter. At the front, a preceding LNA is added to increase sensitivity. When a small signal is fed to the input, after being amplified by several stages, it will become large enough to make the later stages enter into the limiting state. First we suppose that the Kth stage is just going into the limiting state. So there is

$$\left|A^K V_{\mathrm{RFin}}\right| = |V_{\mathrm{L}}|, \quad (5)$$

where A stands for the small signal gain of the limiting amplifier, and V_{L} stands for the limiting voltage. Then suppose that the function of one of the rectifiers and the low pass filter can be expressed as

$$V_{\mathrm{DC}} = C\left\langle \|V_{\mathrm{in}}\| \right\rangle, \quad (6)$$

where C is a constant, $\langle\ \ \rangle$ means averaging with time and $\|\ \ \|$ means the rectifying function. Then, the output voltage can be calculated as

$$\begin{aligned} V_{\mathrm{out}} &= C\left[\sum_{i=0}^{K}\left(\left\langle\left\| A^i V_{\mathrm{RFin}}\right\|\right\rangle\right) + \sum_{K+1}^{N}\left(\left\langle\|V_{\mathrm{L}}\|\right\rangle\right)\right] \\ &= C\left[\left\langle\|V_{\mathrm{RFin}}\|\right\rangle\sum_{i=0}^{K}A^i + (N-K)\left\langle\|V_{\mathrm{L}}\|\right\rangle\right] \\ &= C\left[\frac{A^{K+1}-1}{A-1}\left\langle\|V_{\mathrm{RFin}}\|\right\rangle + (N-K)\left\langle\|V_{\mathrm{L}}\|\right\rangle\right]. \end{aligned} \quad (7)$$

Generally, the condition $A^{K+1} \gg 1$ often satisfies, ignoring 1 and substituting Eqs. (5) and (6) into Eq. (7) yield

$$\begin{aligned} V_{\mathrm{out}} &= C\left[\frac{A}{A-1} + \left(N + \log_A\left|\frac{V_{\mathrm{RFin}}}{V_{\mathrm{L}}}\right|\right)\right]\left\langle\|V_{\mathrm{L}}\|\right\rangle \\ &= \left[\frac{A}{A-1} + \left(N + \log_A\left|\frac{V_{\mathrm{RFin}}}{V_{\mathrm{L}}}\right|\right)\right]V_{\mathrm{DCL}} \\ &= \frac{V_{\mathrm{DCL}}}{20\lg A}\times 20\lg\left|\frac{V_{\mathrm{RFin}}}{V_{\mathrm{L}}A^{-[A/(A-1)+N]}}\right|, \end{aligned}$$

$$\begin{aligned} \mathrm{Slope} &= \frac{V_{\mathrm{DCL}}}{20\lg A}, \\ V_{\mathrm{Y,intercept}} &= V_{\mathrm{DCL}}\left(\frac{A}{A-1} + N - \log_A|V_{\mathrm{L}}|\right). \end{aligned} \quad (8)$$

It is obvious that the output is a logarithmic outcome of the input. The slope and the intercept voltage $V_{\mathrm{Y,\,intercept}}$ will only depend on A, if other parameters like limiting voltage V_{L}, stage N and the rectified limiting voltage V_{DCL} are constant. It is certain that both the limiting voltage V_{L} and stage N parameters can be designed.

Each limiting amplifier stage can DC or AC coupled with others. AC coupling is not preferred because it will add parasitic load to each amplifier, deteriorate GBW and increase area.

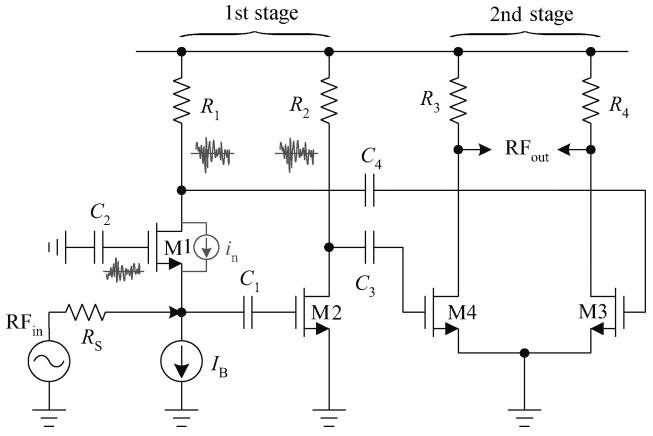

Fig. 3. Two stage wideband noise cancelling LNA.

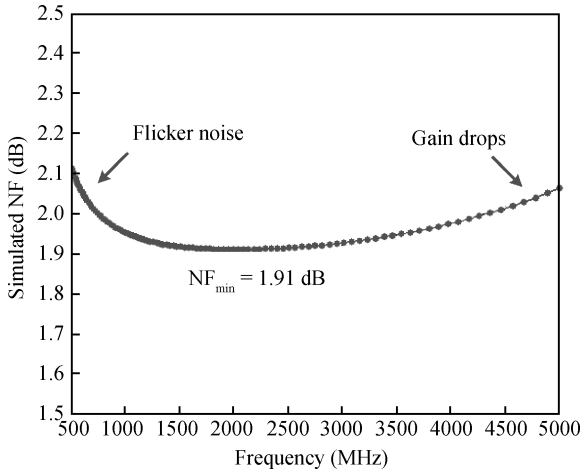

Fig. 4. Simulated NF of the wideband LNA.

However, one problem, the DC offsets due to mismatches between MOS transistors will inevitably occur with DC coupling. Suppose there is a DC offset in the first stage, after being amplified by several stages, it can become large enough to saturate the later stages, which will result in a very poor dynamic range of PD. Therefore, the DCOC circuits, as shown in Fig. 2 should be added to solve this problem. What's more, to save power, the PD can be shut down in the non-working mode.

3. Circuit implementations

3.1. Preceding LNA

In this paper, a two-stage wideband noise cancelling LNA is adopted, as seen in Fig. 3. The first stage is of a single-to-differential stage to save an input pad and a balun, the noise generated from common gate transistor M1 can be cancelled because the resulted noises at differential outputs are common mode with same amplitude if the gains of common gate stage and common source stage are the same[6]. The simulated NF is less than 2.1 dB over a wideband frequency range, as shown in Fig. 4 and the gain is 27 dB with a 3 dB BW over 2 GHz. However, low noise and high gain have inevitably incurred with a penalty of power consumption that is 13 mA from a 1.5 V power supply. In Fig. 5, the simulated output difference of the

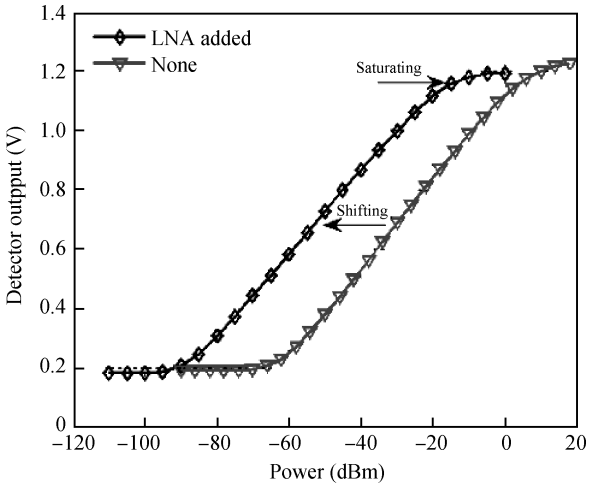

Fig. 5. Simulated PD with/without a preceding LNA.

PD with/without a preceding LNA is displayed at 900 MHz. The sensitivity enhancement is about 24 dB. In addition, it is worth paying attention to that given the total gain of the PD is fixed, adding a LNA has just shifted the detection range. When the gain is used up, the PD will enter into the saturating state, as is shown in the figure.

3.2. Limiting amplifier

The logarithmic amplifier marked by the dotted rectangle in Fig. 2, also known as a demodulated logarithmic amplifier[7], is composed of six limiting amplifiers and seven rectifiers and one low pass filter. The limiting amplifier is shown in Fig. 6(a). It consists of a differential input pair and two folded NMOS diode load. The small signal gain of this amplifier can be expressed as

$$A_v = \frac{g_{m,M1,2}}{g_{m,M3,4}} = \sqrt{\frac{(W/L)_{M1,2} I_{D1,2}}{(W/L)_{M3,4} I_{D3,4}}}. \tag{9}$$

Clearly, the gain is independent of any technology parameters and only depends on the geometry sizes and biasing currents of the input and load MOS transistors. Taking dynamic range, power consumption and noise performance into consideration, a final gain of 9.5 dB is designed for each stage.

For bandwidth consideration, assume N identical limiting amplifier stages are used, the –3 dB bandwidth f_s of each stage related to the total –3 dB bandwidth f_{tot} is given as

$$f_s = \frac{f_{tot}}{\sqrt{2^{\frac{1}{N}} - 1}}. \tag{10}$$

If f_{tot} equals 2 GHz, f_s must be 5.72 GHz. When the power budget is constrained, it is hard to reach such a bandwidth. In order to boost the bandwidth of the limiting amplifier without increasing power consumption budget, one technique, known as active inductor load[8, 9], as shown by the resistor adding between the drain and the gate of the load transistor in Fig. 6(a) is adopted. The equivalent small signal circuit is displayed on the right side in Fig. 6(b). The total load impedance Z_{out} can be figured out as

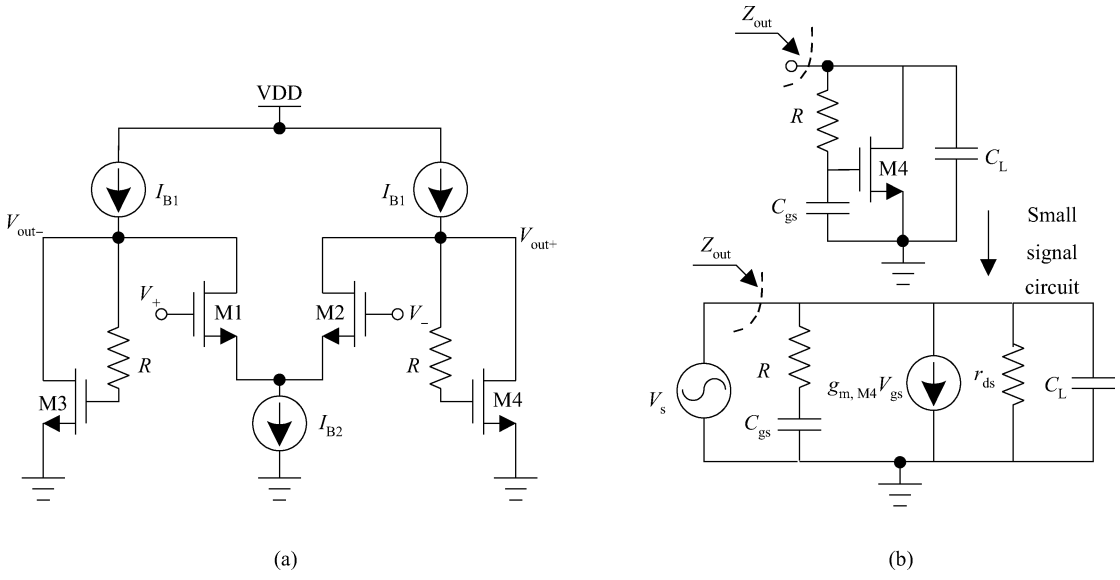

Fig. 6. Limiting amplifier with active inductor load.

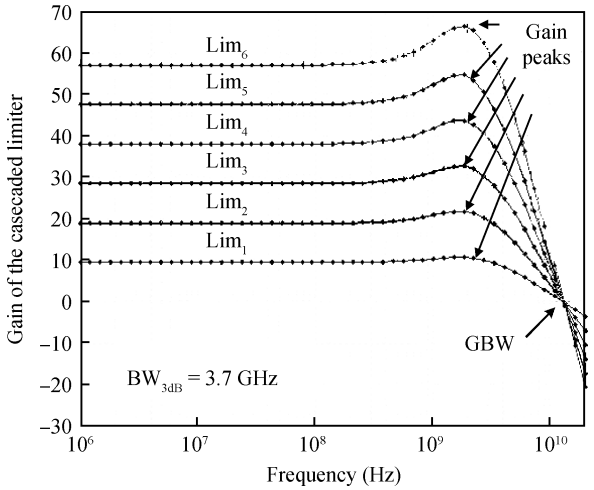

Fig. 7. Z_{out} versus frequency with different resistor R.

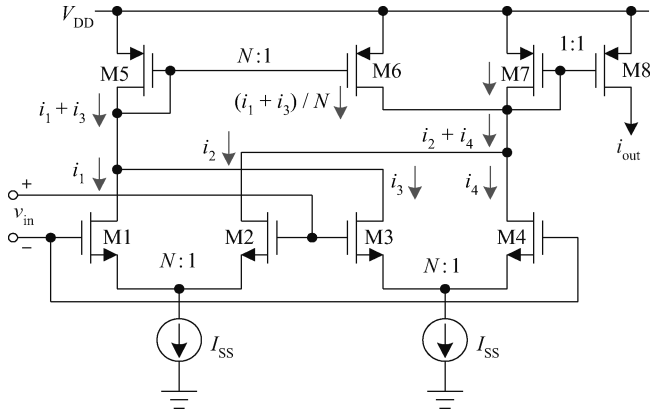

Fig. 8. Full rectifier with two identical unbalanced source-coupled pairs.

$$Z_{out} = \frac{1}{\dfrac{g_{m,M4} + SC_{gs4}}{1 + RSC_{gs4}} + SC_L + \dfrac{1}{r_{ds4}}} = \frac{1}{\dfrac{g_{m,M4} + SC_{gs4}}{R\left(\dfrac{1}{R} + SC_{gs4}\right)} + SC_L + \dfrac{1}{r_{ds4}}}. \tag{11}$$

Once the resistor R equals $1/g_{m,M4}$, the bandwidth can be $1 + C_{gs4}/C_L$ times larger than before. In fact, the active inductor load function can be simply understood as follows: when frequencies is low, the load equals $1/g_{m,M4}$, when frequencies go up, the parasitic capacitor C_{gs4} of the load MOS transistor shorts to ground, the load becomes R. If R is bigger than $1/g_{m,M4}$, this will result in a typical characteristic of inductors. Thus, the frequency response of the amplifier will extend to high frequencies. Figure 7 shows the simulated gain of the cascaded limiting amplifiers. Because of active inductor load, gain peaks appear and the enhanced bandwidth is 3.7 GHz.

3.3. Rectifier

The rectifier in Fig. 8 which rectifies the signal from the limiting amplifier is based on two identical unbalanced source-coupled pairs[10] with different W/L ratios. The ratios are all marked in the figure. Compared with rectifiers using the same architecture in previous works[11, 12], this newly-modified rectifier innovates the ratio between transistors M5 and M6 from 1 : 1 to N : 1, which results the same rectifying function but with the lowest power consumption as demonstrated by the following analysis. With knowledge of the Kirchhoff voltage and current law, there is

$$V_{in} = V_{GS2} - V_{GS1}, \quad V_{in} = V_{GS3} - V_{GS4}, \tag{12}$$

$$i_{D1} + i_{D2} = I_{SS}, \quad i_{D3} + i_{D4} = I_{SS}, \tag{13}$$

$$i_{out} = \Delta i = \Delta i_{D,12} + \Delta i_{D,34} = \left(i_{D2} - \frac{i_{D1}}{N}\right) + \left(i_{D4} - \frac{i_{D3}}{N}\right). \tag{14}$$

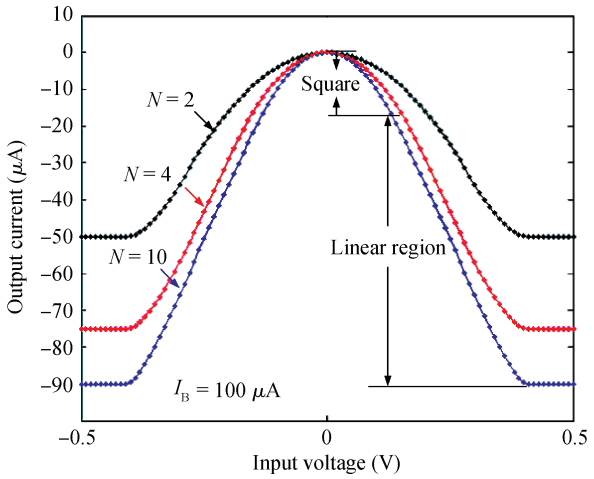

Fig. 9. Transfer function of the rectifier with different W/L ratio N.

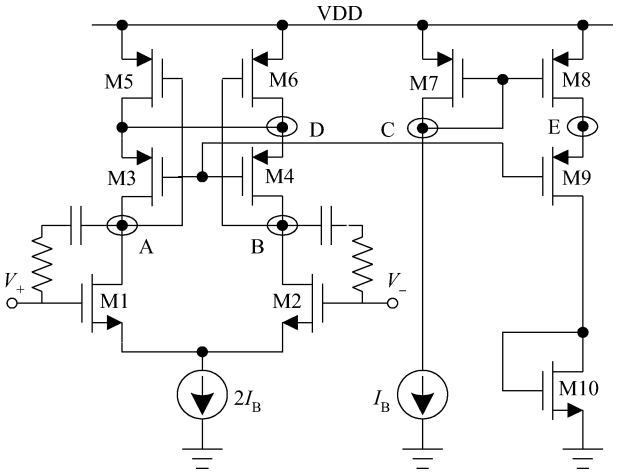

Fig. 10. A low pass filter and a differential op-amp.

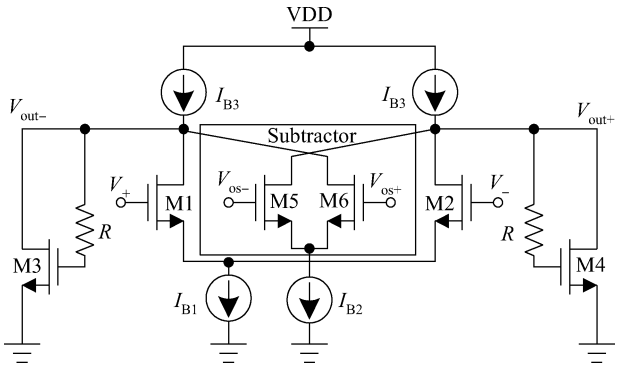

Fig. 11. Subtractor in parallel with limiting amplifier.

Suppose each MOS transistor works in saturation mode and matches well. So substituting the gate source voltages of Eq. (12) in the form of drain currents generates

$$\sqrt{\frac{i_{D2}}{\beta}}-\sqrt{\frac{i_{D1}}{N\beta}}=V_{in},\sqrt{\frac{i_{D4}}{\beta}}-\sqrt{\frac{i_{D3}}{N\beta}}=-V_{in}. \tag{15}$$

Combine Eqs. (13)–(15) and solve for the rectified output current i_{out}. It can be calculated out as

$$i_{out}=\begin{cases}\dfrac{N-1}{N}I_{SS}, & V_{in}^2\geqslant\dfrac{I_{SS}}{\beta},\\ 2\dfrac{N-1}{N+1}\beta V_{in}^2, & V_{in}^2\leqslant\dfrac{I_{SS}}{N\beta},\\ -\dfrac{I_{SS}}{N}+\dfrac{N-1}{N+1}\beta V_{in}^2-\dfrac{2\sqrt{\beta}\,|V_{in}|}{N+1}\times & \\ \quad\sqrt{(N+1)\,I_{SS}-N\beta V_{in}^2}, & \dfrac{I_{SS}}{\beta}\geqslant V_{in}^2\geqslant\dfrac{I_{SS}}{N\beta},\end{cases} \tag{16}$$

where $\beta=\mu C_{ox}W/2L$, I_{SS} is the tail current source. Figure 9 presents the transfer function of the rectifier with different W/L ratios N. For full rectifier design, the ratio N must be large enough, because the intermediate input voltage range of Eq. (16) is the desired one. So in this design a ratio of 10 is selected.

3.4. DC offset cancelling (DCOC) circuit

Due to DC coupling, DCOC circuits are needed to remove the dc offsets. If not, a small voltage offset due to mismatches after being amplified by several stages, will become large enough to saturate the later stages. Thus the dynamic range would be heavily limited.

The DCOC circuit consists of a low pass filter, a differential op-amp and a subtractor. Figure 10 presents the low pass filter and the differential op-amp. In order to avoid attenuating the desired signals, the time constant of the low pass filter must be sufficiently large. However, large capacitors will cost large chip area, which is too costly. In this design, the Miller effect is ably utilized to increase the effective caps of the filter, which has saved the chip areas to a large extent. To maximize the DCOC capacity, the output swing of the different op-amp must be as large as possible, so the transistor M5 and M6, which are used for common mode feedback should be forced to work in the linear region. To accomplish this goal, the replica biasing method is exploited. Assume all transistors work in the saturation region. Transistors M5, M6, M7 and M8 have the same DC currents and dimensions, that is

$$I_{D5}=I_{D6}=I_{D7}=I_{D8},$$
$$(W/L)_5=(W/L)_6=(W/L)_7=(W/L)_8. \tag{17}$$

According to the square law, nodes A, B and C must be exactly at the same voltage, that is

$$V_A=V_B=V_C. \tag{18}$$

Transistors M3, M4 and M9 also have the same DC currents and dimensions. Applying the square law again, there must be

$$V_D=V_E. \tag{19}$$

Therefore, according to Eqs. (17)–(19), transistors M5, M6 and M8 work in the same mode. Once transistor M8 works in the linear region, transistors M5 and M6 will follow. So, transistor M10 is designed to have small dimension to make sure that M8 works in the desired linear region. The remaining part

Table 1. Comparison between published works with the same architecture.

Parameter	Ref. [11]	Ref. [12]	This work
Process	0.35 μm CMOS	0.18 μm CMOS	0.13 μm CMOS
Supply voltage (V)	3.0	1.8	1.5
Power consumption (mW)	30	16	24
Frequency range (MHz)	$\sim$ 900	1–1800	10–2000
Sensitivity (dB)	–50 @ 450 MHz	–45 @ 900 MHz	–70 @ 900 MHz
(Log error at $\pm$3 dB)	–30 @ 900 MHz	–34 @ 1.8 GHz	–48 @ 2 GHz
Dynamic range (dB)	50 @ 450 MHz	39 @ 900 MHz	50 @ 900 MHz
(Log error within $\pm$1 dB)	25 @ 900 MHz	29 @ 1.8 GHz	40 @ 2 GHz
Slope (mV/dB)	7.0	22.0*	12.1
Active area (mm^2)	0.5	1.02 $\times$ 0.47	0.27 $\times$ 0.67

*The slope varies with different frequencies.

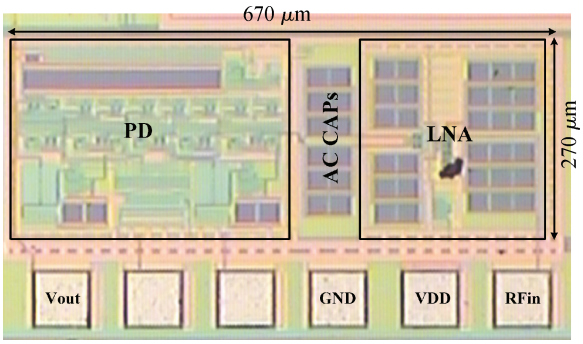

Fig. 12. Die microphotograph.

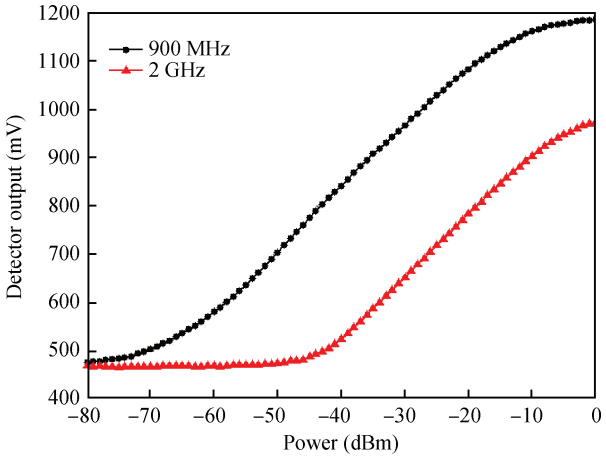

Fig. 13. Input power versus detected output voltage.

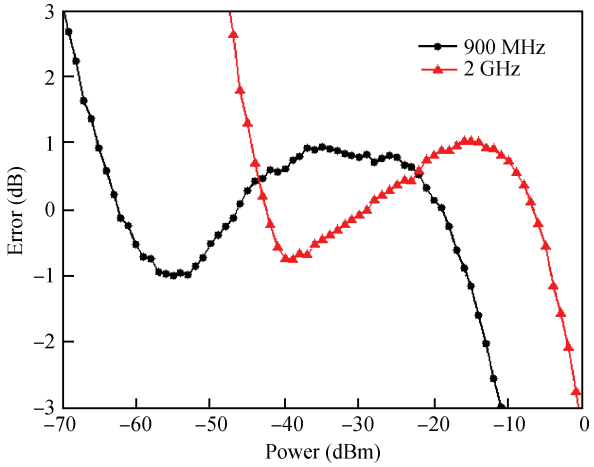

Fig. 14. Log errors of the detector.

is the subtractor, which is combined into the limiting amplifier, as shown in Fig. 11.

4. Measurement results

The chip was fabricated by the SMIC 0.13 μm CMOS process. It consumes 16 mA from a 1.5 V power supply. The die microphotograph is shown in Fig. 12 and its active area is 0.27 $\times$ 0.67 mm^2. Because of the preceding LNA, the measurement is easily done without adding any external matching components and the measured input return loss is less than $-$9.5 dB up to 2 GHz. The detector outputs are depicted in Fig. 13. It demonstrates that the sensitivity of this PD reaches several scores of microvolt at 900 MHz. This is due to the LNA has amplified the faint signals before it reaches the detector. The log errors, the difference between the best fitting line and the actual measurement line is shown in Fig. 14. It shows that within $\pm$3 dB and $\pm$1 dB error range, the satisfied dynamic ranges are 60 dB/45 dB, 50 dB/40 dB at 900 MHz/2 GHz, respectively. The dynamic range deteriorates at 2 GHz because of the gain loss of the limiting amplifier. This can be alleviated by a careful layout scheme and a less strict power consumption budget. Finally, Table 1 summarizes and compares the results of this work to some published ones with the same architecture.

5. Conclusion

A power detector targeted for DCT carrier leakage suppression has been introduced. Based on the logarithmic amplifier principle and successive detection method, it reaches high dynamic range in the radio frequency band. The performance of the detector is enhanced by some special circuit techniques such as a preceding LNA, an active inductor load, etc. The detector achieves a wide dynamic range of 60 dB/45 dB with log error in $\pm$3 dB, 50 dB/40 dB with log error in $\pm$1 dB at 900 MHz/2 GHz, respectively. Beside the aimed application, this detector can also be used for RF power measurement and control, radar applications, etc.

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