A dual-mode analog baseband with digital-assisted DC-offset calibration for WCDMA/GSM receivers*

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Abstract: A dual-mode analog baseband with digital-assisted DC-offset calibration (DCOC) for WCDMA/GSM receiver is presented. A digital-assisted DCOC is proposed to solve the DC-offset problem by removing the DC-offset component only. This method has no bandwidth sacrifice. After calibration the measured output residual offset voltage is within 5 mV at most gain settings and the IIP_2 is more than 60 dBm. The baseband is designed to be reconfigurable at bandwidths of 200 kHz and 2.1 MHz. Total baseband gain can be programmed from 6 to 54 dB. The chip is manufactured with 0.13 μm CMOS technology and consumes 10 mA from a 1.5 V supply in the GSM mode including an on-chip buffer while the core area occupies 1.2 mm^2.

Key words: analog baseband; digital-assisted DCOC; reconfigurable; receiver
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1. Introduction

With the rapid development of cellular mobile communication, the market is moving toward 4G in order to support higher date rates and better mobility. The 4G system is aiming at seamlessly integrating existing telecom standards while sharing as many hardware blocks as possible without sacrificing performance[1]. As for the analog baseband, parameters such as gain, bandwidth, channel-selectivity, noise and linearity should be digitally programmed to be fully compatible with a wide range of wireless standards.

Most of the receivers in mobile terminals adopt direct-conversion structure to ease the image rejection requirement of the system[2, 3]. A simplified direct-conversion receiver architecture is shown in Fig. 1. The analog baseband amplifies the down-converted signal and selects the desired signal channel. One of the critical problems in direct-conversion receivers is the DC-offset[4] which is mainly from LO leakage and component mismatch. The amplified DC-offset at high gain mode would saturate the signal path. Furthermore, DC-offset affects the symmetry of the circuits and degrades the linearity performance such as IIP_2. For these reasons, DC-offset Calibration (DCOC) is necessary. Traditionally DCOC is implemented by employing a high-pass transfer function to filter out the DC and low-frequency components. This kind of analog method usually takes up large chip area and places a limitation on the whole linearity performance because the output signal of PGA may be limited by the analog DCOC.

This paper presents a reconfigurable analog baseband designed for WCDMA/GSM dual-mode receivers with digital-assisted DCOC which overcomes the disadvantages of the analog DCOC. The whole baseband circuit consists of three stages of programmable gain amplifiers (PGAs) with automatic DCOC and a fourth-order Chebyshev low pass filter (LPF) with automatic frequency tuning (AFT).

2. Architecture

The linearity requirement is quite stringent in both WCDMA and GSM systems because of the strong out-of-channel block interference specified in the protocols[5]. The noise is less difficult since there are the LNA and Mixer before the analog baseband in the receiver. The block diagram of the proposed analog baseband is shown in Fig. 2, which provides a good trade-off between linearity and noise. One PGA with good linearity performance is placed before LPF with a max gain of 18 dB. Another two PGAs after the LPF provide a gain of 18 dB and 12 dB, respectively. In order to drive an ADC with large sampling capacitor, a buffer with 6 dB gain is implemented.

According to the Friss equation (1), the first PGA (PGA1) can suppress the noise of the LPF by a factor of A_{PGA1}; other noise can be further suppressed by PGA2 and PGA3. The total noise performance of the analog baseband is determined by the

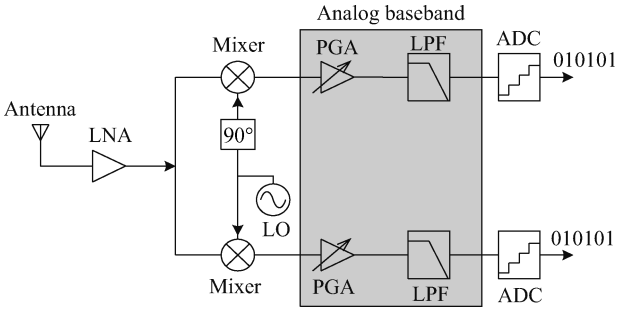

Fig. 1. Simplified block diagram of the direct-conversion receiver.

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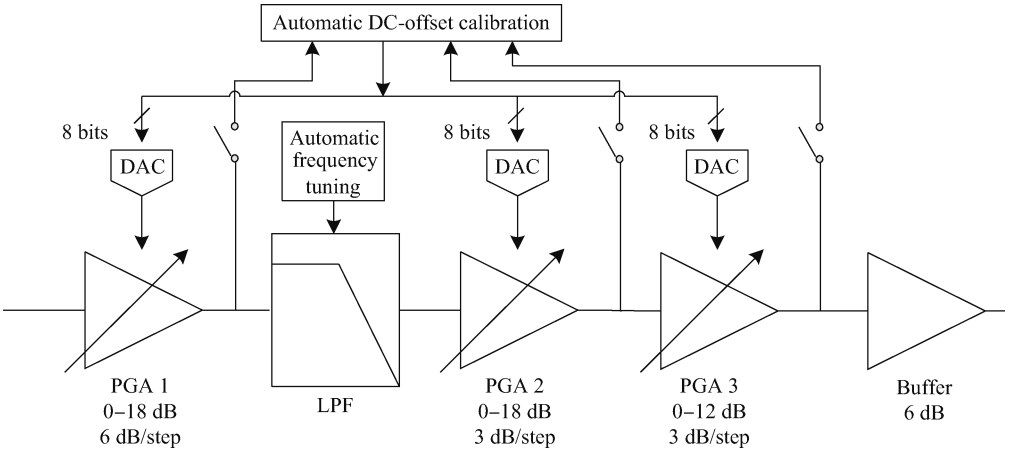


Fig. 2. Block diagram of the proposed analog baseband.

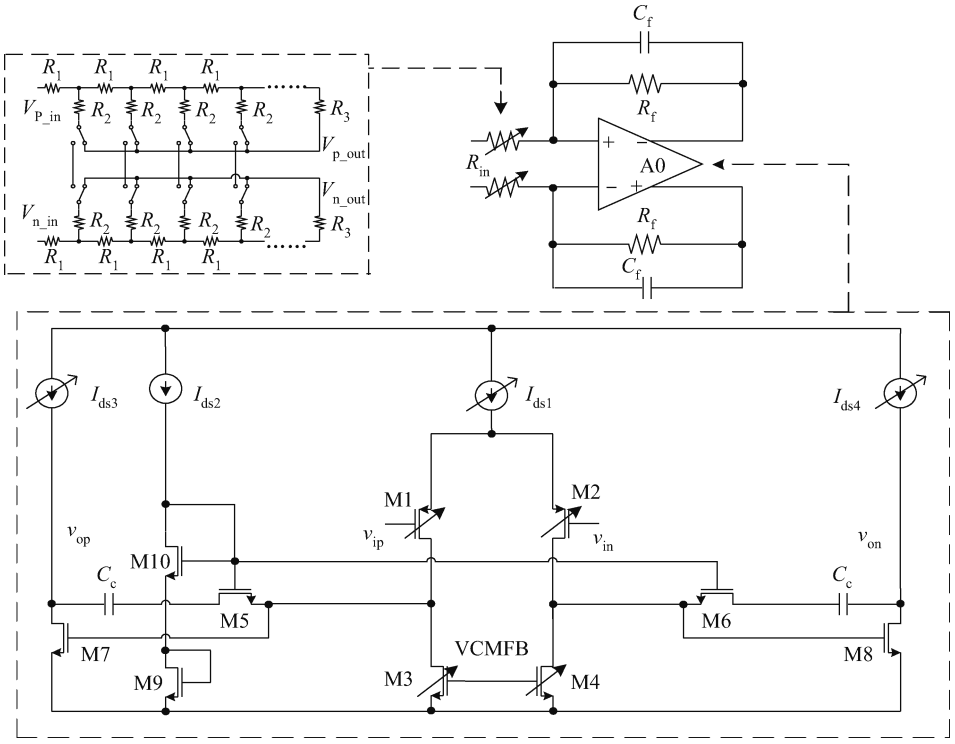


Fig. 3. Proposed PGA structure.

noise factor of the first PGA stage. So PGA1 should be optimized for its noise performance.

$$\mathrm{NF_{tot}} = \mathrm{NF_{PGA1}} + \frac{\mathrm{NF_{LPF}} - 1}{A_{\mathrm{PGA1}}} + \cdots + \frac{\mathrm{NF_{buffer}} - 1}{A_{\mathrm{PGA1}} \cdots A_{\mathrm{PGA3}}}, \quad (1)$$

where NF_x is the noise factor of this stage and A_x is the voltage gain of the stage.

The linearity requirement for PGA1 is also very stringent under the condition of weak in-channel signal with strong out-of-channel blocks. Since the LPF can greatly attenuate the out-of-channel block, the out-of-channel linearity problem is alleviated for the two PGAs after the LPF. With decreasing supply voltage and shrinking of the CMOS channel length, linearity becomes a major design challenge. The closed-loop PGA structure and active-RC LPF are good candidates for linearity considerations since they can take advantage of the high loop gain. The stability problem should be taken into consideration carefully by adopting the feedback structure. The reconfigurable operational amplifier used in the PGAs should have gain bandwidth (GBW) as large as possible with enough phase margin (PM).

3. Analog baseband design

3.1. PGA and DCOC

The operational amplifier with resistive feed-back (OPAMP-R) as shown in Fig. 3 is the most common PGA structure in narrowband analog baseband for its good linearity and wide dynamic range. The OPAMP is a two-stage RC miller-compensation structure optimized for GBW and PM. It is designed to be programmable by changing the bias currents

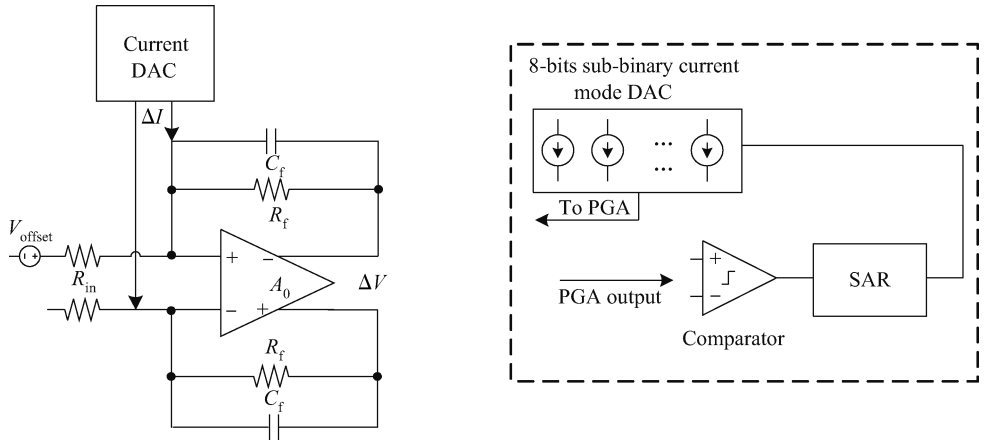


Fig. 4. Principle of digital-assisted DC-offset calibration.

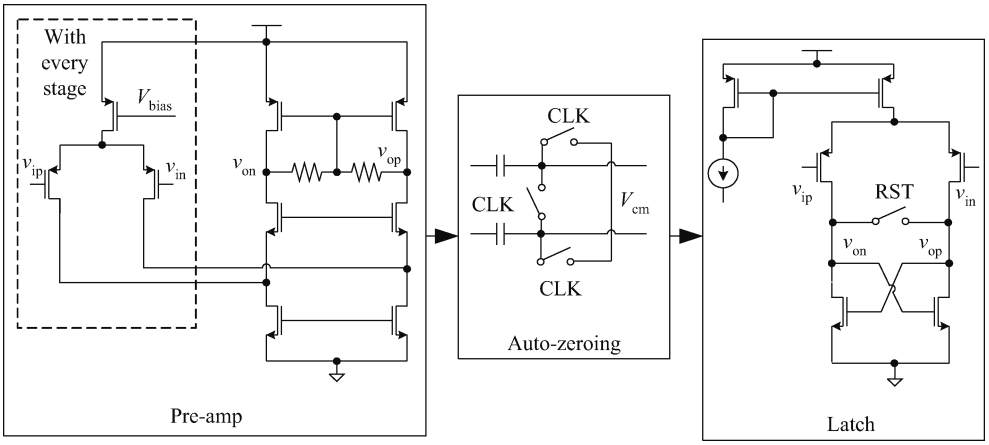


Fig. 5. Auto-zeroing comparator structure.

and input transistors for the different bandwidth requirements of WCDMA and GSM systems. The PGA gain can be obtained using the feedback analysis in Eq. (2):

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{A_0}{1+\beta A_0} \approx \frac{1}{\beta} = \frac{R_{\text{f}}}{R_{\text{in}}}, \tag{2}$$

where A_0 is the OPAMP open-loop gain and β is the feedback factor.

The gain can be programmed by changing the ratio of R_{f} and R_{in}.The practical way is to change either R_{f} or R_{in}. R_{f} variation will lead to a change of loop feedback factor which may cause the stability problem. R_{in} is the load of the previous stage and a simple change in R_{in} will affect the characterization of the previous stage. A differential shortened circuit structure[6] is used here for the gain programming without affecting the loop and the load of the previous stage. The input resistor network is like an R–$2R$ structure. Since the OPAMP input is a virtual ground, by shortening the differential input resistors the connection point of the two resistors is still a virtual ground so the input resistance remains the same during the gain variation. Different gain steps can be achieved by the proper ratio of R_1, R_2 and R_3.

DC-offset is a key problem in direct-conversion receivers as mentioned above. The method used in other works to solve the DC-offset problem is to introduce a feedback loop filtering away the low-frequency components[7]. In order to ease the bandwidth sacrifice, this method consumes a large chip area using large resistors and capacitors to make the high-pass cutoff frequency low enough. Another great disadvantage of this method is the settling time problem. A step pulse such as gain change is introduced; the settling time $\tau \propto RC$ is quite long, where R and C are the resistance and capacitance in the DCOC feedback loop which are quite large. In order to solve these problems a digital-assisted DC-offset calibration method, shown in Fig. 4, is presented. A comparator is used to sense the output residual voltage offset of every PGA stage at different gain settings and a successive approximation register (SAR) algorithm is employed to calculate the calibration value in the digital domain before the circuits start to work. A digital-to-analog convertor (DAC) converts the digital calibration value according to the different gain settings into analog current to calibrate the offset out.

The relationship between the output offset voltage and the injecting current of the DAC is

$$V_{\text{outoffset}} = \Delta I \cdot R_{\text{f}} + V_{\text{offset}}, \tag{3}$$

where ΔI is the injecting current of the DAC and R_{f} is the feedback resistance. It is clear that an appropriate ΔI can compensate the input offset voltage. Since the R_{f} is about several kΩ, in order to cover large output offset and have small residual off-

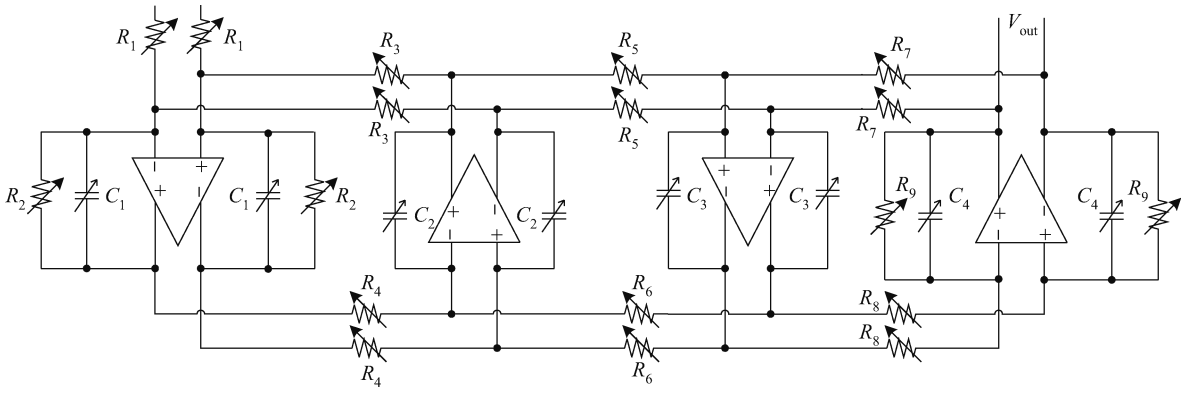


Fig. 6. The 4th-order LC ladder LPF structure.

set voltage, the full range should be larger than 50 μA while the LSB is less than 0.1 μA. The binary current mirror DAC is not suitable for the sake of matching. Since missing codes are not allowed in the SAR algorithm while redundancies are not problematic, a current division network in the radix of 1.67 is introduced. The SAR algorithm can be improved by introducing the redundancies. The calibrated values for different gain settings are stored in a look-up-table (LUT). Since the calibrated value is obtained ahead of time, the settling time is dependent on the PGA bandwidth instead of the large RC value in the analog DCOC.

Another issue with the calibration we should consider is the offset of the comparator itself. An auto-zeroing structure is adopted here to calibrate the offset of the comparator as shown in Fig. 5. A pre-amplifier and auto-zeroing capacitors are placed before the latch to calibrate the offset of the pre-amplifier and reduce the offset of latch to $1/A_{\rm pre}$, where $A_{\rm pre}$ is the gain of the pre-amplifier. For the sake of power saving, the pre-amplifier is a folded-cascode structure sharing the telescopic stage. The folded stage with every PGA is only turned on while this stage is under calibration.

3.2. LPF and AFT

The active-RC filter following the first stage of PGA is implemented for filtering out the out-of-channel blocks. The filter utilizes the LC ladder structure to accomplish the 4th-order low-pass-filter as shown in Fig. 6. The OPAMP structure used in the filter is similar to the ones used in PGA with programmable GBW. With different bandwidth requirements of WCDMA and GSM, passive RC devices are designed to be reconfigurable while sharing as many root components as possible.

The cut-off frequency of LPF can be tuned from 200 kHz to 2.1 MHz, which means a large RC variation. Capacitance increase will affect the load of OPAMP and result in the stability problem. Larger capacitors consume more chip area while the increasing resistance leads to larger in-band noise. However the noise from LPF has little effect on the whole baseband since there is a PGA placed before it. The OPAMP's limited bandwidth has an effect on the transfer function of the LPF. In order to get an accurate cut-off frequency, the OPAMP used in

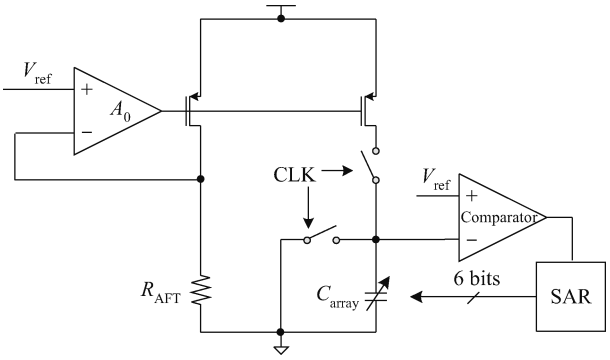


Fig. 7. AFT structure.

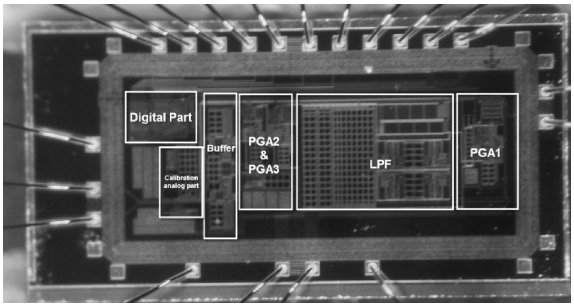


Fig. 8. Chip microphotograph.

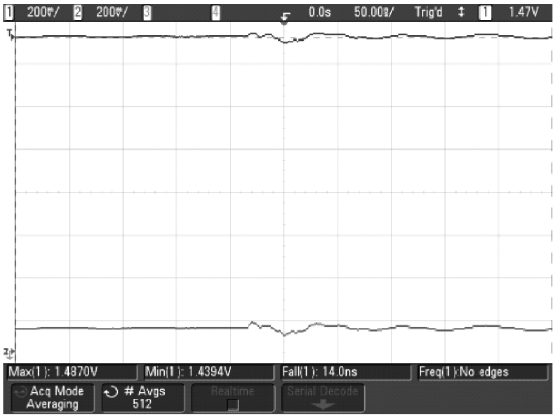
LPF should meet the GBW requirement

$$\mathrm{GBW} \geqslant \left| \frac{A(\mathrm{j}\omega_{\rm c})}{\delta} - 1 \right| |[1 + A(\mathrm{j}\omega_{\rm c})]\omega_{\rm c}|\,, \qquad (4)$$

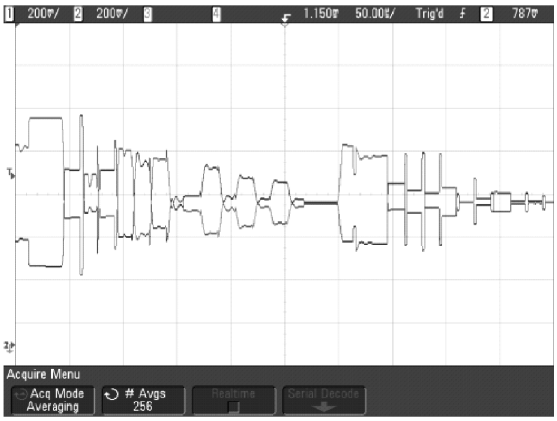
where the δ is the error tolerance and $A(\mathrm{j}\omega_{\rm c})$ is the OPAMP open loop gain at the frequency of $\omega_{\rm c}$.

The LC ladder structure is widely adopted since it is less sensitive to the component value. However the PVT variations may cause the large deviation of bandwidth a lot. So an automatic frequency tuning (AFT) circuit as shown in Fig. 7 is introduced to tune the capacitor arrays automatically against the variations.

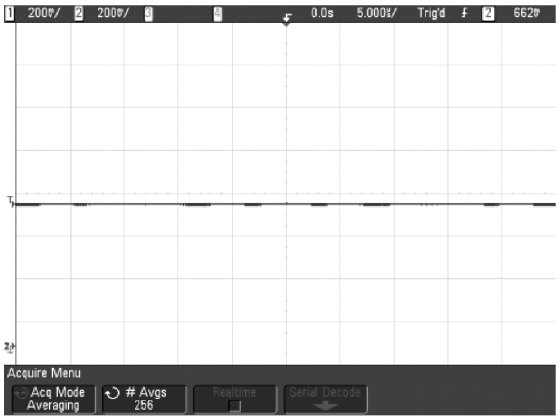
The resistance and capacitance are the same as those used in the LPF. The current flowing through the resistor $R_{\rm AFT}$ is $I = V_{\rm ref}/R$ and the current is mirrored to charge the capacitor arrays at a frequency of f_1. With a clock duty cycle of 50%



(a) Before calibration



(b) During calibration



(c) After calibration

Fig. 9. Measured digital-assisted DC offset calibration.

the charging time of the capacitor array is $\tau_{\text{charge}} = 1/2 \cdot f_1$. Since $I = C\frac{\mathrm{d}V}{\mathrm{d}t}$ the capacitor array output voltage is $V_{\text{Carray}} = \int_{t_1}^{t_2} \frac{V_{\text{ref}}}{RC}\mathrm{d}t$.

First, the capacitor array is charged, the output voltage V_{Carray} is compared with the V_{ref} and a digital tuning value is obtained. Then the capacitor array is discharged for re-starting the charging at next clock cycle. After the calibration is finished the capacitor array output voltage is quite close to the V_{ref} under the SAR algorithm. So the RC will be very close to the τ_{charge} from a crystal-oscillator reference clock; the bandwidth can be tuned to the targeted frequency.

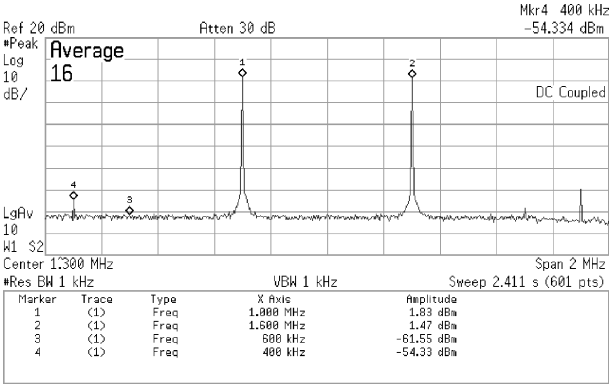


Fig. 10. Measured in-channel linearity in WCDMA mode.

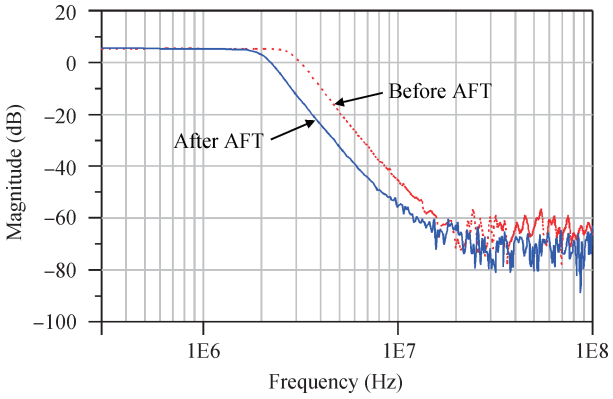


Fig. 11. Measured AFT in WCDMA mode.

4. Experimental results

The proposed analog baseband is manufactured in SMIC 0.13 μm CMOS process. The core area is 1.2 mm^2 excluding pads. The chip is tested in the circuit-on-board (COB) package. A microphotograph of the bonded chip is depicted in Fig. 8.

The DCOC is measured using the oscilloscope to sense the two differential output voltages. The calibration procedure is shown in Fig. 9. Before the calibration, the output offset voltage is quite large and whole baseband is inactive, while during calibration the output voltage is calibrated out by the SAR algorithm and the corresponding digital calibration values are stored in LUT. After calibration the residual offset is quite small. The measured residual output offset is within 5 mV at most gain settings by using the voltage-meter.

Since offsets of every PGA stage are calibrated out, the whole baseband is free of offset and is quite symmetrical which can lead to good linearity. The measured in-channel linearity in WCDMA mode is shown in Fig. 10. With two-tone of 1 MHz and 1.6 MHz inputs, the measured second order intermodulation (IM2) harmonic at 600 kHz is less than –62 dB.

The measured frequency response of AFT in WCDMA mode is shown in Fig. 11 with a buffer gain of 6 dB. The dotted line is the frequency response before AFT; the cutoff frequency is about 3 MHz. The solid line is the frequency response after AFT; the cutoff frequency is tuned to 2.07 MHz, meeting the WCDMA system specifications. The cutoff frequency after AFT in GSM mode can be tuned to 197 kHz which is very

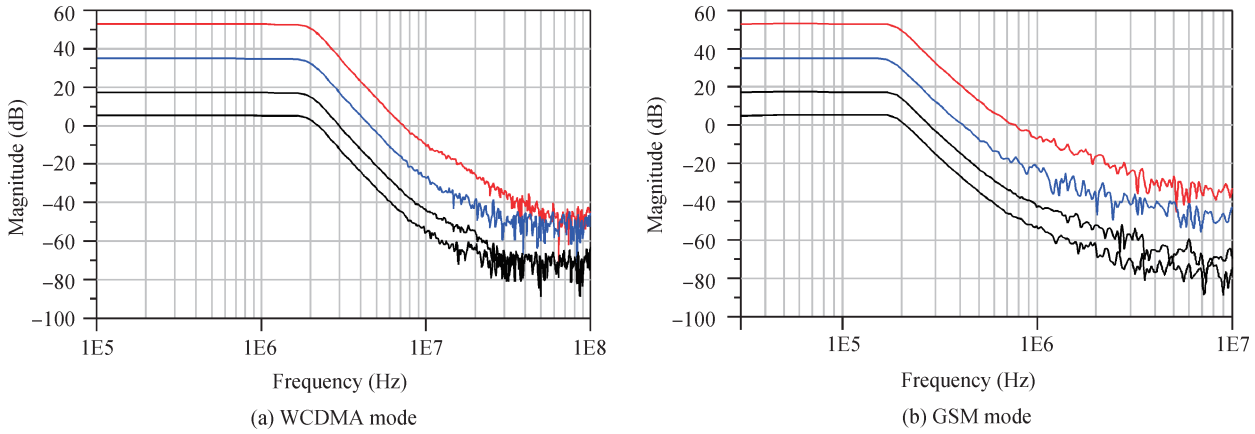


Fig. 12. Measured baseband frequency response.

Table 1. Performance summary and comparison

Reference	This work	Ref. [7]	Ref. [8]	Ref. [9]
Supply voltage (V)	1.5	3.3	2.5	1.2
Process (μm)	0.13	0.35	0.13	0.13
Gain range (dB)	5.3–53.3 (both modes)	63 max	–6 to 68	0–39
Noise figure (dB)	23.8 (@ WCDMA) 33 (@ GSM)	33.3 (@ WCDMA) 70.6 (@ GSM)	20.8	28.4
In-channel linearity IIP_3 (dBm)	20.4 (WCDMA @ gain = 5.3 dB) 7 (GSM @ gain = 5.3 dB)	40 (WCDMA) 28 (GSM)	21 (@ gain = 3 dB)	> 24 (@ min gain)
In-channel linearity IIP_2 (dBm)	> 60 (both modes @ gain = 5.3 dB)	Unknown	Unknown	Unknown
Out-of-channel linearity IIP_3 (dBm)	14.1 (WCDMA @ gain = 53.3 dB) 17 (GSM @ gain = 53.3 dB)	Unknown	9.5 (@ gain = 41 dB)	40.34 (@ min gain)
Current consumption (mA)	29* (@ WCDMA) 10* (@ GSM)	14 (@ WCDMA) 9.6 (@ GSM)	20.5 (@ WCDMA) 22 (@ WLAN)	29.3 (@ max bandwidth)
Chip area (mm^2)	1.2	Unknown	1.66	1.56

*Including on chip buffer with current consumption of 5 mA.

close to the expected 200 kHz. The whole baseband frequency response is shown in Fig. 12 with every PGA gain stage.

The measured gain range is from 5.3 to 53.3 dB in both modes. The noise figure is 23.8 dB in WCDMA mode and increased to 33 dB in GSM mode due to large flicker noise. Under a 1.5 V supply, the chip consumes 29 mA and 10 mA current in WCDMA and GSM mode, respectively, including an on-chip buffer. The main performance features of the proposed analog baseband are summarized and compared in Table 1.

5. Conclusion

A dual-mode analog baseband for WCDMA and GSM receivers implemented in 0.13 μm CMOS process has been presented in this paper. The system architecture and circuit design considerations for the analog baseband have been discussed. In circuit implementation the digital-assisted DCOC and AFT are introduced to do the performance calibration rather than the traditional analog methods. The measured results indicate that the digital-assisted calibration method is effective at low area and power consumption, and does not degrade any analog performance. The proposed analog baseband meets the specifications of WCDMA/GSM system requirements.

References

[1] Giannini V, Craninckx J. Baseband analog circuits for software defined radio. Springer, 2008
[2] Gharpurey R, Vanduru N, Dantoni F, et al. A direct conversion receiver for the 3G WCDMA standard. IEEE J Solid-State Circuits, 2003, 38(3): 556
[3] Reynolds S K, Floyd B A, Beukema T, et al. A direct conversion receiver IC for WCDMA mobile systems. IEEE J Solid-State Circuits, 2003, 38(9): 1555
[4] Razavi B. Design considerations for direct-conversion receivers. IEEE Trans Circuits Syst, 1997, 44(6): 428
[5] 3rd Generation Partnership Project. UE Radio Transmission and Reception (FDD), Technical Specification. TS25.101, V5.7.0
[6] Daniel L K, Shah M, Godambe N, et al. A single-chip triband (2100, 1900, 850/800 MHz) WCDMA/HSDPA cellular transceiver. IEEE J Solid-State Circuits, 2006, 41(5): 1122
[7] Zhou Zhujing, Li Zhisheng, Li Ning, et al. A highly linear filter and VGA with DC-offset correction for GSM/WCDMA receivers. Chinese Journal of Semiconductors, 2007, 28(3): 372
[8] D'Amico, Baschirotto S, de Matties M, et al. A CMOS 5 nV/$\sqrt{\text{Hz}}$-IRN 74 dB-gain-range 82 dB-DR multi-standard baseband chain for Bluetooth UMTS and WLAN. IEEE J Solid-State Circuits, 2008, 43(7): 1534
[9] Giannini V, Craninckx J, D'Amico S, et al. Flexible baseband analog circuits for software-defined radio front-ends. IEEE J Solid-State Circuits, 2007, 42(7): 1501