A 10-bit 100-MS/s CMOS pipelined folding A/D converter*

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Abstract: This paper presents a 10-bit 100-MSample/s analog-to-digital (A/D) converter with pipelined folding architecture. The linearity is improved by using an offset cancellation technique and a resistive averaging interpolation network. Cascading alleviates the wide bandwidth requirement of the folding amplifier and distributed interstage track/hold amplifiers are used to realize the pipeline technique for obtaining high resolution. In SMIC 0.18 μm CMOS, the A/D converter is measured as follows: the peak integral nonlinearity and differential nonlinearity are $\pm$0.48 LSB and $\pm$0.33 LSB, respectively. Input range is 1.0 $V_{P\text{-}P}$ with a 2.29 mm^2 active area. At 20 MHz input @ 100 MHz sample clock, 9.59 effective number of bits, 59.5 dB of the signal-to-noise-and-distortion ratio and 82.49 dB of the spurious-free dynamic range are achieved. The dissipation power is only 95 mW with a 1.8 V power supply.

Key words: analog-to-digital converter; pipelined folding; resistive averaging interpolation; offset cancellation
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1. Introduction

In a modern communication system, the A/D converter plays an important role of digitizing the input signal and is the key media connecting the analog world with digital processors. Based on nonlinear analog signal preprocessing, the folding technique greatly reduces the number of complicated analog circuits and ensures high speed, as compared to the traditional flash structure. Many innovative techniques such as interpolation, averaging and cascading have been reported to simplify or improve the folding architecture, but its resolution is limited to usually 6–8 bits due to device mismatch in CMOS processes, which lead to large offsets in amplifiers and comparators[1−3]. Pipelined technology is widely applied to acquire over 10-bit resolution, which enables operational amplifiers with feedback to generate a residue signal and drive the next stage sub-ADC[4, 5]. The refinement of pipelining can speed up the interpolation and cascaded folding architecture.

In this paper a 10-bit 100-MS/s A/D converter with pipelined folding architecture is proposed. A three-stage sub-ADC conversion with distributed track/hold amplifiers is included. The 3 × 3 folding factor is realized by using a two-stage cascaded folding circuit. A resistive averaging interpolation network is used to interpolate voltage. Random noise and nonlinear distortion from the input offset are reduced dramatically. A low kickback preamplifier with offset cancellation eliminates the input offset voltage and improves the resolution of the folding A/D converter.

2. A/D converter architecture

The block diagram of the presented A/D converter is shown in Fig. 1. The pipelining technique, cascaded folding, resistive averaging interpolation, distributed interstage track/holds and error correction are used to acquire the design targets of a 10-bit and 100-MHz rate.

After sample and hold, the analog input is collected to a preamplifier array. Four dummy preamplifiers are added individually at the top and bottom of the reference resistor ladder to avoid the boundary effect of zero-crossing (ZX)[2]. The averaging interpolation is used to improve conversion linearity. The coarse sub-ADC with 18 comparators extracts the 4-bit MSB code and high/low overflow bits based on 18 differential output voltages of the preamplifiers. The outputs of the preamplifier array are interpolated and folded to increase the conversion speed. A fold module uses two-stage cascaded folding amplifiers and two interpolations. 12 outputs from the first-stage of 3× folding are 2× interpolated. The second-stage folded signal is also collected to the resistive averaging network. A 2× interpolated signal drives the medium sub-ADC to generate 3 MLSB bits and an error-correction bit. At the same time, 4× interpolation is employed to obtain the input for the last-stage subranging ADC. Distributed interstage track/holds are used behind each folding stages to relieve the settling requirement of the folding amplifiers for high-speed conversion and intermediate folded signals are isolated to realize the pipelined architecture. The multiplexers are controlled by the output from the previous sub-ADC. Their results are 4× interpolated to determine the LSBs. Finally, the outputs of three sub-ADCs are transferred to the error-correction and driver block to acquire 10-bit digital code. Two times folding and four times interpolating are adopted to reduce the number of folders and comparators. Only 20 folders and 50 comparators are employed for folding order $F = 9$ and 10-bit resolution.

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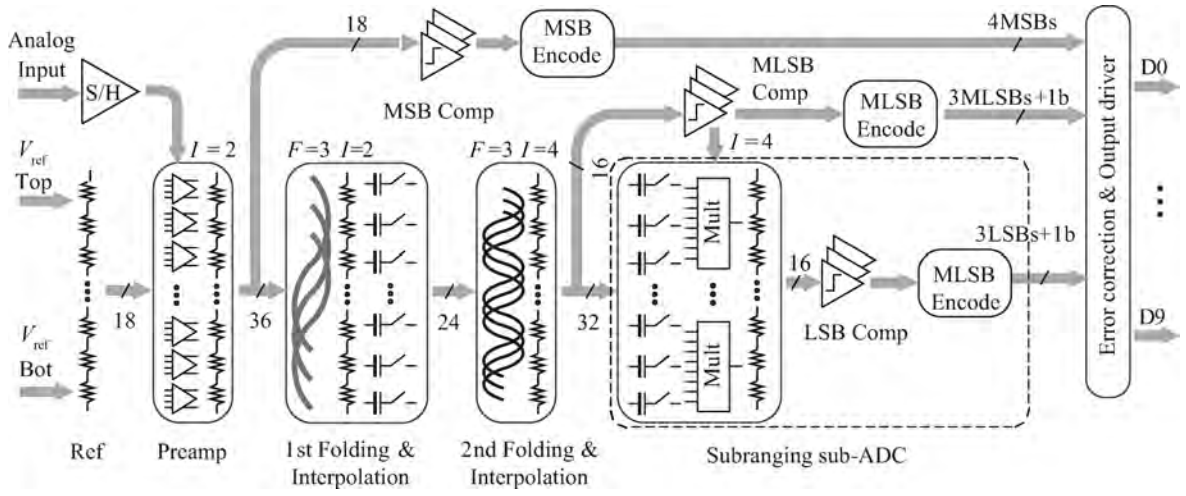

Fig. 1. Block diagram of the pipelined folding A/D converter.

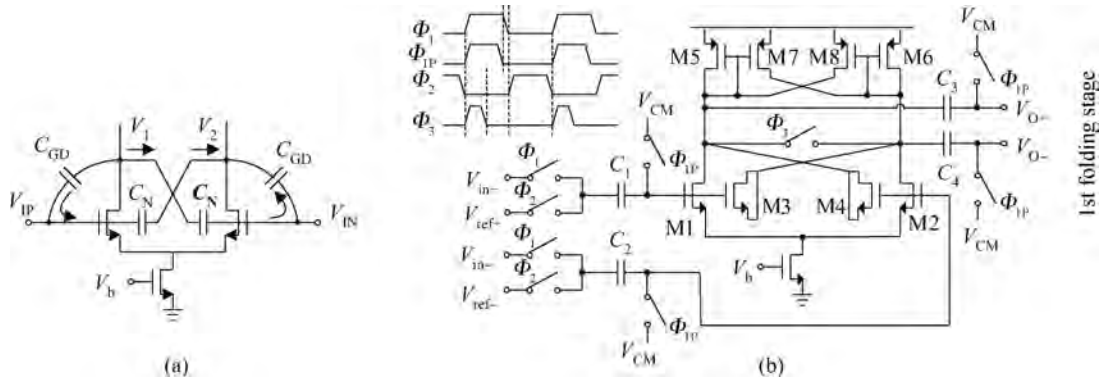

Fig. 2. (a) Neutralization technique. (b) Preamplifier with offset cancellation.

3. Circuit implementation

3.1. Offset cancellation preamplifier

As the beginning of analog preprocessing, an analog input is compared with reference voltages in a preamplifier array. When the sampling signal is equal to a reference voltage, the preamplifier outputs a ZX. The preamplifier is the most important circuit that affects the precision of an A/D converter.

Large voltage variations on the drain nodes are coupled to the input of the preamplifier through the parasitic capacitances of the input differential pair. This coupled-voltage will disturb input signals as the output impedance of the previous stage circuit is not equal to zero, which is kickback noise. It is proved that the neutralization technique can alleviate the kickback noise effectively[6, 7], as shown in Fig. 2(a). Since the voltage variations at the drains are complementary, if two capacitances with a value $C_N = C_{GD}$ are cross-connected, the charging currents in C_N and C_{GD} can cancel out each other (the arrows on Fig. 2(a) represent the currents flowing when V_1 increases and V_2 decreases).

The input offset of the preamplifier is another major error source limiting the resolution of the converter. For a differential pair with a resistive load, the input offset is approximated by

$$V_{OS} = \frac{V_{GS} - V_{TH}}{2}\left(\frac{\Delta R_D}{R_D} + \frac{\Delta\beta}{\beta}\right) - \Delta V_{TH}, \qquad (1)$$

where ΔV_{TH}, $\Delta\beta$ and ΔR_D are mismatches in thresholds, current factors and the load resistors, respectively. Obviously, it can reduce the offset effect to size transistors, but its availability is not ideal[8].

The schematic of the preamplifier with offset cancellation is shown in Fig. 2(b). As neutralized capacitors, M3 and M4 are half the size of M1 and M2 in order to decrease the kickback noise. M5, M6, M7 and M8 constitute the cross-coupled PMOS loads to increase the operation speed. Switched-capacitor circuits at the input and output stages separate the preamplifiers from other stages. It avoids interference from inter-stage noise and enables the employment of the offset canceling technique. When Φ_1 is high, the differential signals, V_{in+} and V_{in-}, are sampled at the C_1 and C_2 capacitors, respectively. The other side of the capacitors is connected to the common mode voltage V_{CM} (around $0.6V_{DD}$). After short reset-time Φ_3, the output offset voltage is AV_{OS} stored in the C_3 and C_4 capacitors. Φ_{1P} is switched off before Φ_1 to prevent charge injection in C_3 and C_4. During the amplifying phase Φ_2, the reference voltages from the resistor ladder, V_{ref+} and V_{ref-}, are applied to the capacitors C_1 and C_2. Considering the input capacitors of the

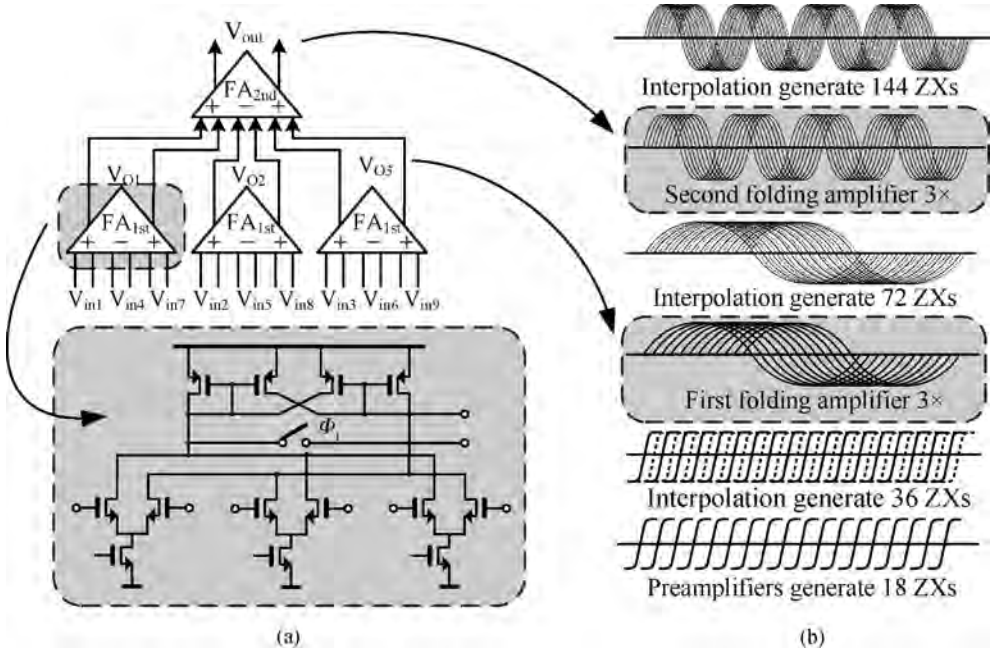

Fig. 3. (a) Cascaded folding scheme and single folding amplifier. (b) Graphical representation of cascaded 9× folding and 2× interpolation three times to achieve 144 ZXs.

preamplifier, C_{p1} and C_{p2}, the input voltage at phase Φ_2 can be expressed by

$$\begin{aligned} V_{IN}(\Phi_2) = &\left[\frac{V_{ref+}C_1}{C_1+C_{p1}} - \frac{(V_{in+}-V_{cm})\,C_1}{C_1+C_{p1}}\right. \\ &\left. + \frac{V_{cm}C_{p1}}{C_1+C_{p1}} + V_{OS}\right] \\ &- \left[\frac{V_{ref-}C_2}{C_2+C_{p2}} - \frac{(V_{in-}-V_{cm})\,C_2}{C_2+C_{p2}} + \frac{V_{cm}C_{p2}}{C_2+C_{p2}}\right] \\ = &\frac{C_1}{C_1+C_{p1}}(V_{ref}-V_{in}) + V_{OS}. \end{aligned} \tag{2}$$

According to Kirchhoff's voltage law, when a clock period is over the transferred voltage of the output node

$$V_O(\Phi_2) = AV_{IN}(\Phi_2) - AV_{OS} = \frac{C_1}{C_1+C_{p1}}A\,(V_{ref}-V_{in})\,. \tag{3}$$

The offset still is transferred to the output at Φ_2 and canceled out with the stored offset at the prior clock. Only the voltage difference between the input and the reference voltage is amplified, so the outputs without the preamplifier offset are transferred to the first folding stage. In the actual design, the offset is not eliminated absolutely because of process mismatch and charge injection. The gain of the preamplifier is not too large, otherwise AV_{OS} can overflow the output. To guarantee accuracy greater than 10 bits for a 1 $V_{P\text{-}P}$ input, the gain is 6 and the offset-cancellation capacitor is 108 fF.

3.2. Pipelined folding

Higher resolution requires a higher folding degree, so a higher gain of the folding amplifier is needed to acquire enough output voltage swing to drive the next stage circuits. Additionally, the frequency-multiplier effect requires a larger bandwidth of single folding amplifier[9]. It can be expressed as

$$BW_F \geqslant \frac{\pi}{2}Ff_{in,\,max}, \tag{4}$$

where F is the folding degree and $f_{in,\,max}$ is the input signal frequency. Contrasted with the traditional single-stage folding amplifier, the cascaded scheme makes circuit design more flexible. A full-differential cascaded folding architecture is used in this work, as shown in Fig. 3(a). The folding circuit is composed of two-stage folding triplets. A folding factor of three is achieved in each folding stage and the second stage folding amplifier combines three folding output signals of the first stage. Nine-time folding is obtained in total. The advantage of the two-stage/cascaded folding scheme is that a larger output swing and gain can be achieved easily. The folding amplifier of each stage has one pole and the total bandwidth of the cascaded folder can be calculated by

$$\begin{aligned} BW_{total} = &\frac{1}{\sqrt{2}}\Big[\left(BW_{1st}^4 + BW_{2nd}^4 + 6BW_{1st}^2BW_{1nd}^2\right)^{1/2} \\ &- \left(BW_{1st}^2 + BW_{2nd}^2\right)\Big]^{1/2} \\ \approx &\,0.32(BW_{1st} + BW_{2nd}), \end{aligned} \tag{5}$$

where BW_{1st} and BW_{2nd} are the bandwidth of the first stage and the second stage separately. Comparing Eq. (4) with Eq. (5), it is obvious that the cascaded folding amplifier relaxes the bandwidth requirement.

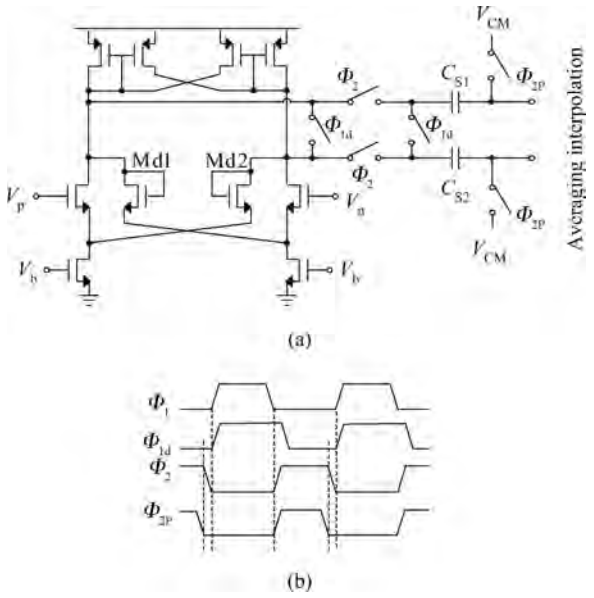

Fig. 4. (a) Distributed interstage track/hold amplifier. (b) Timing diagram.

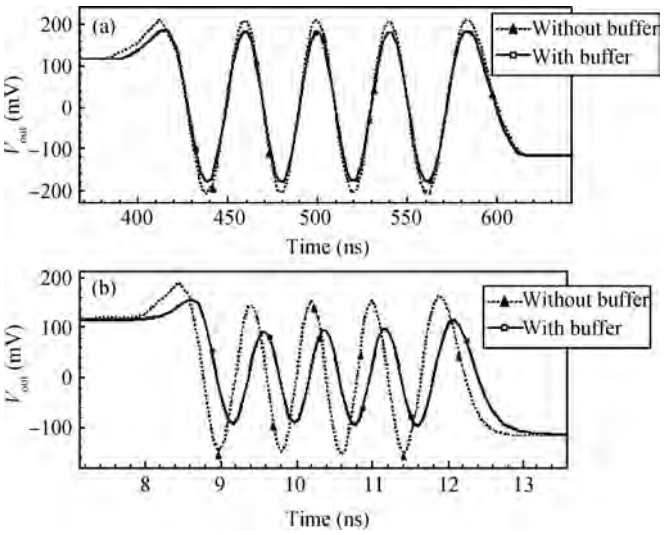

Fig. 5. (a) Folding output for 1 MHz input. (b) Folding output for 50 MHz input.

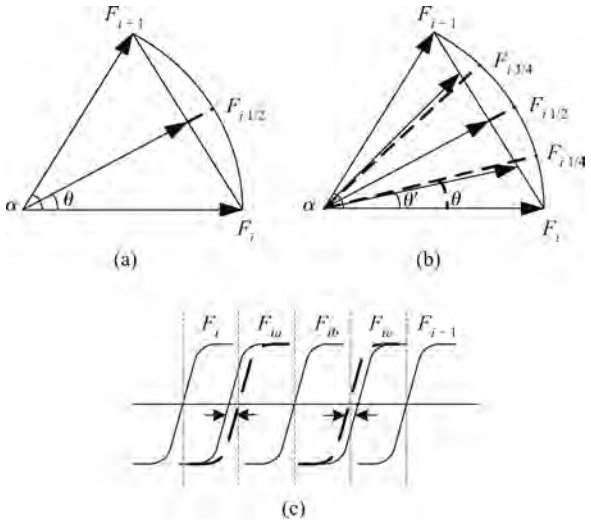

Fig. 6. Phase diagrams of (a) 2× interpolation and (b) 4× interpolation. (c) Effect of 4× interpolation phase error.

Two adjacent folding input signals of each folder in both stages folding amplifier have the same constant phase difference of $\pi/3$ because of the same folding rate of 3, but the phase of the folding output is decided by the number of folding amplifiers at each stage. As described in Section 2, there are 12 folding amplifiers in the first stage so their output phase difference is $\pi/12$ to achieve 36 ZXs, while the second stage folds 24 differential signals for a 3-time rate to output voltage waves with a phase difference of $\pi/8$. After 9× folding, 144 ZXs are obtained to reach high 7-bit resolution (for 4 MSBs and 3 MLSBs), as shown in Fig. 3(b).

Since the settle time of the folding stages should be within one clock, the common cascaded folding architecture requires a strict limitation on the analog input frequency. To overcome the drawback, a distributed implementation of the track/hold function to realize the pipeline technique[8, 10]. In this work, the distributed interstage track/hold amplifier consists of a buffer amplifier with minor output impedance and a switch capacitor circuit, as shown in Fig. 4. The amplifier with a conventional cross-coupled PMOS load samples the previous stage folding output in the sampling capacitor, C_{S1} and C_{S2} during the Φ_2 (Φ_{2P}). Md1 and Md2 introduce the positive feedback loop to make the output turn over more quickly. When the holding period, Φ_{1d} has a slightly longer reset time than the reset clock in folding amplifiers and the sampling clock in preamplifiers, Φ_1. It avoids backward flows due to the switch transition from the next stage circuit and facilitates the output signal to settle more rapidly.

The distributed track/hold amplifier connected to the outputs of the each folding circuit as an interfacing buffer separate each folding stage[11]. Each stage of the folding amplifier can settle independently with pipelining and the speed advantage of single stage folding ADC still remains. One additional benefit of the buffer amplifier is that more suitable folded signals without dc level shifting at high frequency due to capacitive effects on the output nodes of the folding circuit are obtained. The output signals of the proposed circuit at input frequency of 1 and 50 MHz during transient analysis compared with the folding circuit without the buffer amplifier are shown in Fig. 5. The dynamic performance of the folding ADC is improved. The gain variance of the buffer amplifier affects the linearity, but it can be ignored compared with the descent on precision from the dc level shifting without the buffer amplifier obviously.

3.3. Resistive averaging interpolation

Interpolation can reduce the number of parallel folding amplifiers to avoid power and area penalties. The combination of the interpolation and averaging techniques is used widely to improve the DNL[12]. As shown in Fig. 3(b), resistive averaging interpolation networks are employed in this design many times. The differential folding outputs are equidistantly phase shifted with a normalized amplitude, but an error of phase shifting is found when the interpolating rate is larger than 2. Figures 6(a) and 6(b) show the phase diagrams when the interpolat-

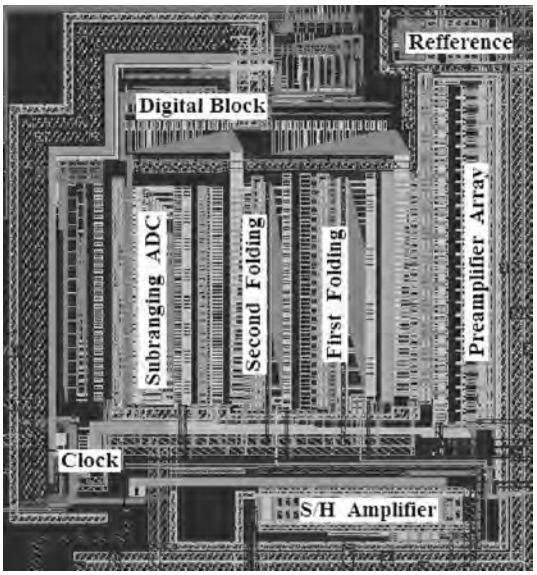

Fig. 7. Layout of the chip.

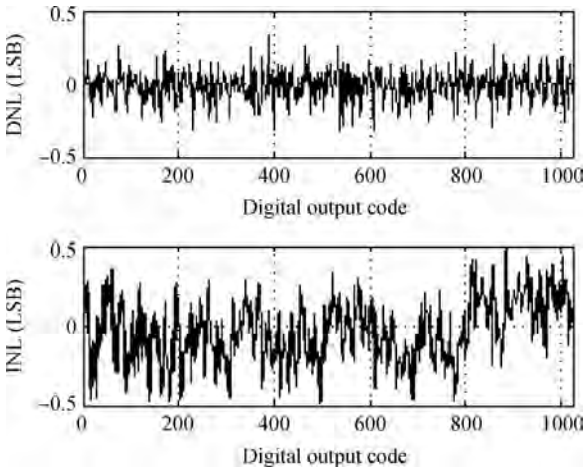

Fig. 8. Measured DNL/INL performance.

ing rate is 2 and 4, respectively. From the figures it is evident that the phase of the middle interpolated signal ($F_{i1/2}$) is correct. The largest error of phase shifting is found at 1/4 and 3/4 of the interpolation ladder. The caused effect in ZXs is shown in Fig. 6(c). The phase of 4× interpolated signal $F_{i1/4}$ can be given by

$$\theta' = \frac{\alpha}{2} - \arctan\left(\frac{1}{2}\tan\frac{\alpha}{2}\right), \tag{6}$$

where α is the phase difference of two contiguous folding output signals, F_i and F_{i+1}, while the ideal phase, θ, is equal to $\alpha/4$. As previously described, 4× interpolation is used in the last stage conversion in this work and 8 folding outputs in full scale are gained. So a phase error of 0.055° can be calculated according to Eq. (4). It results in a relative phase error of 0.24%. Since the 4× interpolation between two folding output signals has a corresponding resolution of 4-bit, this phase error results in an INL error of 0.039 LSB. The effect of phase error in the resolution can be ignored.

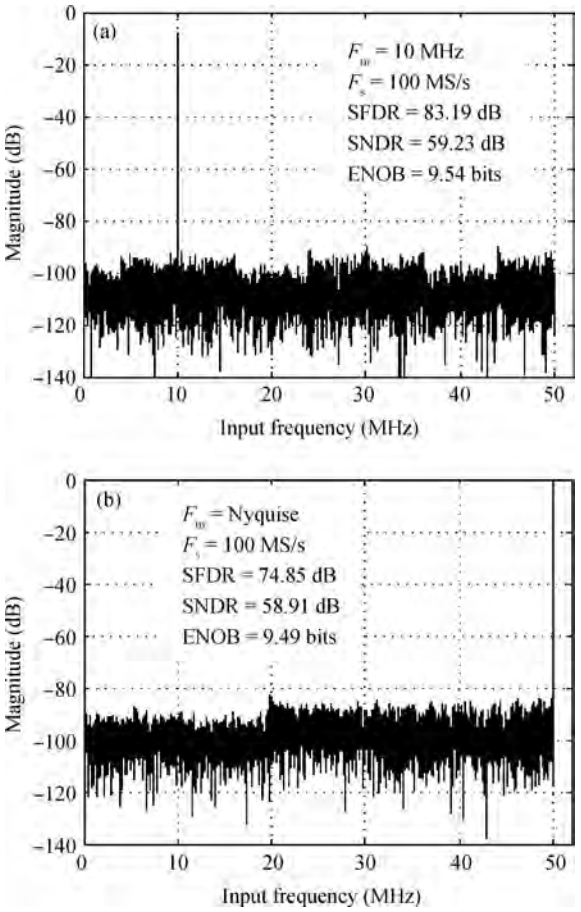

Fig. 9. 8192-point FFT spectra at 100 MS/s for (a) $F_{\rm in} = 10$ MHz and (b) $F_{\rm in} = 50$ MHz.

4. Experimental results

The prototype A/D converter is realized in an SMIC 0.18 μm 1-poly 6-metal CMOS process. The chip area is 1.45 × 1.58 mm^2, as shown in Fig. 7. The analog and digital blocks dissipate 94 mW and 1 mW, respectively, both at 1.8 V power supply. Preamplifiers, folding amplifiers, comparators and distributed track/hold amplifiers dissipate most power.

The analog input full-scale range is 1 V and the input capacitance is 2.8 pF used in the sample-and-hold amplifier. Figure 8 shows the static performance of the A/D converter. The measured DNL and INL are less than ±0.33 LSB and ±0.48 LSB using the histogram method at 100 MS/s.

The FFT spectra of the A/D converter for input frequencies of 10 MHz and 50 MHz, both at 100MS/s, are shown in Fig. 9. Better dynamic performance is achieved as compared with the previous works[10, 12]. The measured results of 10 MHz input frequency include an SFDR of 83.19 dB, a total harmonic distortion (THD) of 77.98 dB, and an SNDR of 59.23 dB. When the A/D converter operates with a Nyquist-rate input, the SFDR is 74.85 dB, THD is 71.72 dB and SNDR is 58.91 dB. Figure 10 shows the dynamic performance versus input frequency and sampling rate, respectively. The SNDR value shows a flat response across input frequency up to 50 MHz at 100 MS/s. The SFDR and THD vary 8.34 dB and 6.26 dB, respectively, in Fig. 10(a). The peak ENOB of 9.59, SNDR of 59.5 dB and SFDR of 82.49 dB for 20 MHz input at rated full sam-

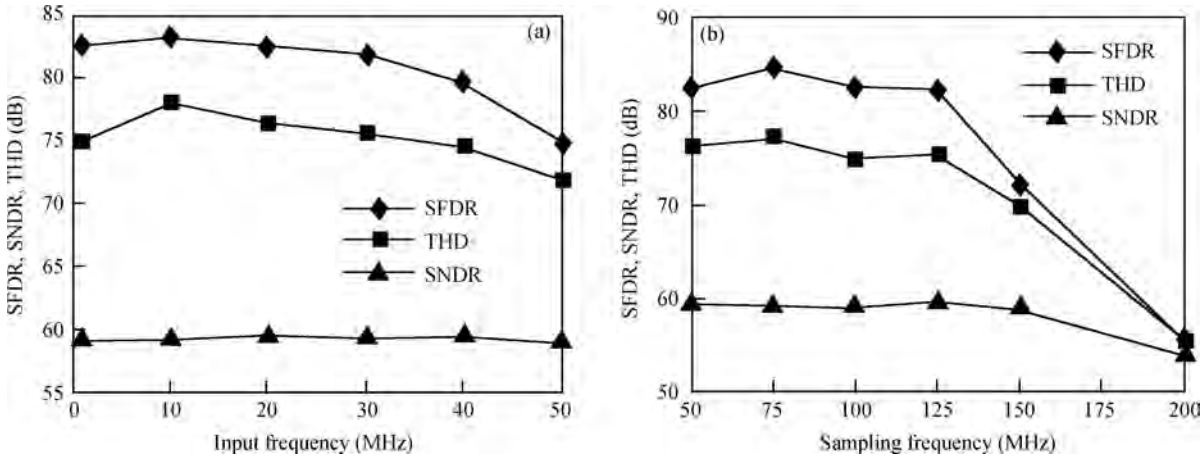

Fig. 10. Measured dynamic performance versus (a) input frequency at 100 MS/s and (b) sampling rate with 1 MHz input frequency.

Table 1. Performance comparison of high-solution folding A/D converters.

Parameter	Ref. [10], 2001	Ref. [14], 2002	Ref. [15], 2007	Ref. [16], 2007	Ref. [13], 2011	Ref. [17], 2011	This work
Process	0.5 μm CMOS	0.12 μm CMOS	0.13 μm CMOS	0.35/0.13 μm CMOS	0.18 μm CMOS	65nm CMOS	0.18 μm CMOS
Resolution (bit)	8	10	10	10	8	7	10
Sampling rate (MS/s)	100	100	200	200	1000	1000	100
Supply (V)	5	1.2	1.8	3.3/1.2	1.8	1.2	1.8
Power (mW)	165	180	195	286	1700	110	95
DNL/INL (LSB)	0.4/1.3	—	1.01/1.92	0.7/1.5	0.28/0.4	—	0.33/0.48
SNDR (dB)	42.3 (F_{in} = 1 MHz)	—	53.5 (F_{in} = 2.4 MHz)	54.1 (F_{in} = 10 MHz)	46.5 (F_{in} = 373 MHz)	39.1 (F_{in} = 250 MHz)	59.5 (F_{in} = 20 MHz)
ENOB (bit)	6.73	8.83	8.6	8.69	7.4	6.2	9.59
Active area (mm^2)	1.68	0.43	3.24	0.45	17.52	0.87	2.29
FOM (pJ/Conv)	15.5	3.96	2.5	3.46	6.71	1.50	1.23

ple frequency are obtained. When the input frequency is about 1MHz, the tested sampling rate varies from 50 to 200 MHz in Fig. 10(b). The converter is functional even up to 150 MS/s with only slight performance degradation and even an 8.7-bit ENOB achieved at 200 MS/s. However, many extra sample and store capacitors applied in preamplifiers and distributed track/hold amplifiers can increase the signal attenuation and settle time, so it is difficult to attain such high converted speed as Ref. [13] at the cost of great power consumption and chip area.

The common figure of merit (FOM) commonly used for the Nyquist-rate ADC is

$$\mathrm{FOM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \times f_{\mathrm{Sample}}} = 1.23\,\mathrm{pJ/Conv.} \qquad (7)$$

Table 1 shows the performance comparison of the proposed A/D converter with several previous works on folding A/D converters with high resolution. The proposed A/D converter has advantages of a superior FOM, a relatively simple circuit configuration, high resolution, low power consumption and perfect performance. The performance summary at 100 MS/s and 1.8 V of the proposed A/D converter is listed in Table 2.

5. Conclusion

The systematic design of a 10-bit 100-MS/s Nyquist-rate pipelined folding A/D converter in 0.18 μm CMOS has been presented. In this work, an effective architecture with offset cancellation, cascaded folding of 3 × 3, pipeline, distributed track/hold and resistive interpolation averaging is implemented successfully. It can reduce the number of the comparators, relax the requirement of bandwidth and improve linearity. Measurements yielded good results: a DNL/INL figure is $\pm 0.33/\pm 0.48$ LSB. Over 80 dB SFDR is achieved at low input frequencies. The A/D converter of Nyquist-rate input can still operate with a good performance. A perfect ENOB of 9.59 bits and a FOM of 1.23 pJ/Conv are realized.

Table 2. Performance summary of the proposed A/D converter.

Parameter	Value
Process	0.18 μm CMOS
Resolution	10 bits
Sampling rate	100 MS/s
Supply	1.8 V
Input range	$\pm$500 mV
Input capacitance	2.8 pF
Power	95 mW
DNL/INL	$\pm$0.33/$\pm$0.48 LSB
SNDR/SFDR/THD	59.23 dB/83.19 dB/77.98 dB @ $F_{\text{in}} = 10$ MHz
	59.50 dB/82.49 dB/76.36 dB @ $F_{\text{in}} = 20$ MHz
	58.91 dB/74.85 dB/71.72 dB @ $F_{\text{in}} = 50$ MHz
ENOB	9.54 bits @ $F_{\text{in}} = 10$ MHz
	9.59 bits @ $F_{\text{in}} = 20$ MHz
	9.49 bits @ $F_{\text{in}} = 50$ MHz
Chip area	2.29 mm^2

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