CMOS linear-in-dB VGA with DC offset cancellation for direct-conversion receivers

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Abstract: A low-power high-linearity linear-in-dB variable gain amplifier (VGA) with novel DC offset calibration loop for direct-conversion receiver (DCR) is proposed. The proposed VGA uses the differential-ramp based technique, a digitally programmable gain amplifier (PGA) can be converted to an analog controlled dB-linear VGA. An operational amplifier (OPAMP) utilizing an improved Miller compensation approach is adopted in this VGA design. The proposed VGA shows a 57 dB linear range. The DC offset cancellation (DCOC) loop is based on a continuous-time feedback that includes the Miller effect and a linear range operation MOS transistor to realize high-value capacitors and resistors to solve the DC offset problem, respectively. The proposed approach requires no external components and demonstrates excellent DCOC capability in measurement. Fabricated using SMIC 0.13 μm CMOS technology, this VGA dissipates 4.5 mW from a 1.2 V supply voltage while occupying 0.58 mm^2 of chip area including bondpads. In addition, the DCOC circuit shows 500 Hz high pass cutoff frequency (HPCF) and the measured residual DC offset at the output of VGA is less than 2 mV.

Key words: linear-in-dB; VGA; DC offset cancellation
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1. Introduction

The VGA is an indispensable block for communication systems to maximize the dynamic range of the receivers. An important requirement for a CMOS VGA is a decibel-linear gain control characteristic, where the gain of the VGA changes exponentially with the control signal. This exponential gain control is required to achieve a wide dynamic range and to maintain the AGC loop settling time independent of the input signal level[1].

As in all CMOS implementation, there are two approaches used to realize VGAs depending on whether the control signal is digital or analog. The digitally controlled VGAs use a series of switchable resistor techniques to control gain, which with fine programmable gain steps have proven to be a good solution in terms of noise and linearity in CMOS processes[2,3]. Also, the gain curve should not deviate from the nominal case significantly with process variations. In digitally controlled VGAs, gain varies as a discrete function of the control signal, which can lead to a discontinuous signal phase that can cause problems in many systems. In order to reduce the amount of jumps, a large number of control bits are required with digitally controlled VGAs. Therefore, for applications that require smooth gain transitions, VGAs controlled by analog signal are preferred. Many different exponential control circuits have been proposed recently, such as pseudo-exponential[4,5], Taylor series approximation equations[6], signal summing[7], master-slave control[8], etc. Many applications require a wide dynamic gain range, so that many VGAs must be used if we employ the proposed exponential control circuit, resulting in higher power consumption and larger chip size. Moreover, the circuit suffers from poor linearity which becomes even more pronounced with mismatch of the differential pair devices. The designs need to maintain good linearity across the whole gain range and DC offset cancellation needs to be addressed, particularly at high gain settings.

In a direct-conversion receiver, the main causes of DC offset are layout mismatch and self-mixing of the leakage LO signal. Extraneous DC offset located in the down-converted signal spectrum may corrupt the signal, degrade sensitivity and dynamic range of the receiver system, and even saturate the subsequent analog baseband stages if a high gain is required. Thus DC offset cancellation is inevitably becoming a challenge in the design of direct conversion receivers. In this work, a wide-range low-power high-linearity VGA with continuous-time feedback calibration loop is presented.

Figure 1 shows the baseband architecture for communication systems. We aim to design an analog controlled low-power wide-range VGA, the VGA uses two cascade gain stages to provide over 60 dB gain range with continuous tuning. The

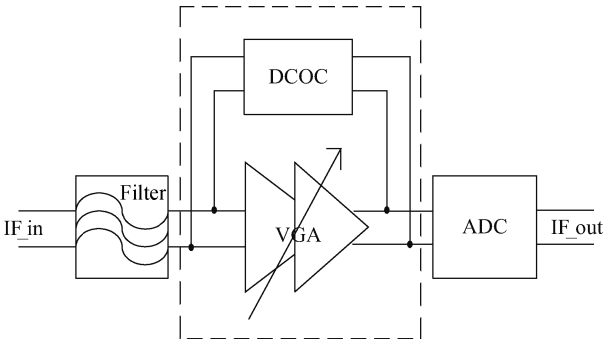

Fig. 1. Schematic of baseband.

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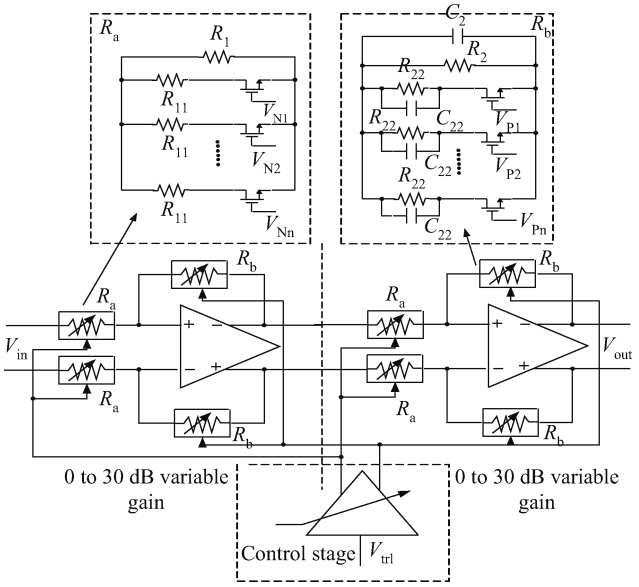

Fig. 2. Schematic of the chain including the two-stage VGA and the gain control circuit.

DCOC circuit is used to remove DC offsets introduced from the VGA and the previous circuits.

2. VGA circuit design

The block diagram of the VGA chain including two-stage variable gain amplifiers and a control circuit is shown in Fig. 2. Since it is very difficult to use a single VGA to realize a very wide dynamic range of gain tuning, we propose to utilize two stages of individual VGAs to attain the required 60 dB range and decibel linearity. The gain of each VGA stage is in the range 0 to 30 dB. Thus, the total target gain of this two-stage VGA varies from 0 to 60 dB. As can be seen in Fig. 2, a fully differential resistive feedback topology with complementary control ramps is adopted. Employing a high gain amplifier in a differential feedback network leaves the amplifier inputs in virtual ground configuration and hence improves the nonlinearity of the amplifier itself. Assuming an ideal OPAMP, the closed loop voltage gain is given by

$$\text{Gain} = \frac{R_\text{b}}{R_\text{a}}. \tag{1}$$

The gain of the variable gain amplifier is made variable by varying the feedback resistor R_b and the input resistor R_a. In order to obtain the exponential characteristic, we need differential ramp operation which is the input resistance and the feedback resistance can be varied in opposite directions dependent on the control voltage. Thus, with increasing AGC control voltage, the control voltages of the input resistors ramp up, while the control voltages on the feedback resistors ramp down, increasing the closed-loop amplifier gain exponentially. Using this technique, a two-stage 60 dB linear-in-dB VGA with continuous analog tuning was designed with a comparable linearity and noise performance relative to the PGA implementation of the same circuit.

A multiple-ramp controlled mechanism is used to gradually change the resistance network of R_a and R_b. The cost is additional voltage-ramp circuitry which leads to a slight increase in area and power. The dashed line in Fig. 2 shows resistor networks that are used to construct a highly linear wide-range trim mechanism. Here, as for R_a network, R_s is the resistance of MOS transistor switch, if we choose R_1 and R_{11}, such that $R_{11} \gg R_\text{s}$ and $R_{11} \gg R_1$ then, the nonlinearity introduced by the switch becomes insignificant when the switch is fully on. The only nonlinear region of the switch is when the switch is not fully on or fully off.

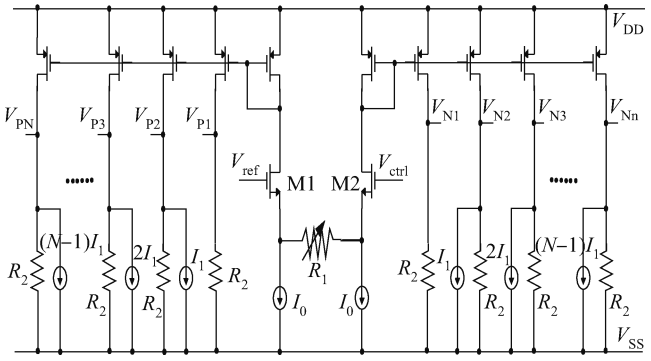

Fig. 3. Schematic of the differential ramp voltage circuit.

2.1. Control circuit design

The differential ramp voltage generation circuit is shown in Fig. 3[9]. The input control voltage V_ctrl is compared with a reference voltage V_ref and the difference current running through R_1 causes the current in one of the diode connected devices to increase and the current through the other one to decrease. By mirroring this current into a resistor, a control voltage proportional to the input voltage difference can be obtained. Multiple control voltages with the desired amount of offset can be obtained by simply pulling a fixed amount of offset current from each of these mirrored branches. The ramp voltage, for example, can be written down as follows:

$$V_\text{N} = (V_\text{ctrl} - V_\text{ref})\,\frac{R_2}{R_1} - [(N-1)\,I_1]\,R_2. \tag{2}$$

The resistor ratio in the first term defines the slope of the characteristics, whereas the second term is the fixed offset. In order to have flexibility in the design, resistor R_1 is trimmable with a two-bit slope control word, enabling us to adjust the slope of the control ramps and hence the VGA characteristics. A bandgap-driven current source utilizing the same type of resistor allows the ramp control voltages to be temperature insensitive to first order.

The number of ramps was chosen to be 10 for accurate and smooth gain curve and area cost consideration. Figure 4 shows the VGA gain characteristics with 10 control ramps for various slop settings. For a 10-ramp design the current consumption of the ramp generation circuit is 200 μA from a 3.3 V supply. This circuit works from 3.3 V providing the control voltages for the switches. The switches with 3.3 V gate drive can allow larger signal swing without significant linearity degradation.

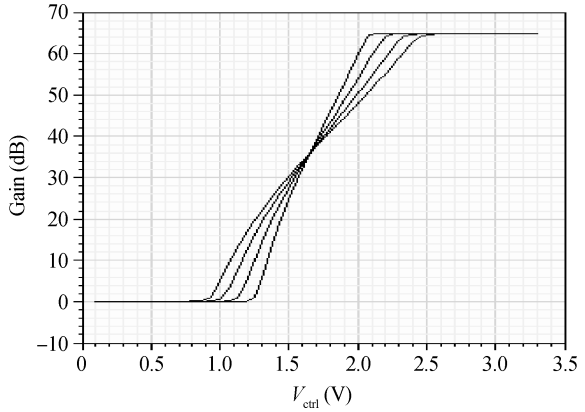

Fig. 4. Simulated VGA gain characteristics.

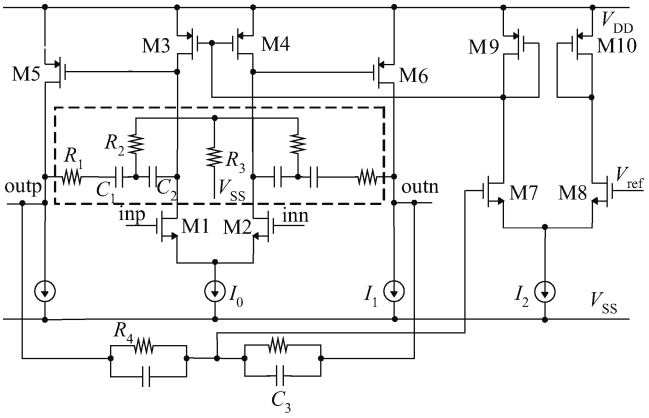

Fig. 5. Two-stage OPAMP with the proposed Miller compensation.

2.2. Operational amplifier

Since the performance of VGA mainly depends on the OPAMP, high-performance OPAMP is required. In general, DC gain, gain-bandwidth product (GBW) and phase margin (PM) characteristics are major considerations about OPAMP design. High DC gain, large GBW and proper PM always indicate high linearity, precise gain and reliable stability. The schematic architecture of the proposed OPAMP is shown in Fig. 5.

The amplifier is a two-stage, fully differential Miller-compensated OPAMP with a unity gain bandwidth greater than 750 MHz with 0.5 pF differential load capacitance. A phase margin of 60 degree is allocated for both common-mode and differential-mode loops. The NMOS devices, in Fig. 5 compare the common-mode level with desired reference level and inject proper amount of common-mode currents into the differential output nodes of the first stage.

It is difficult to achieve high open-loop gain at the down converted signal band like 10 MHz and keep reliable stability at the same time with the conventional two-stage OPAMP. To settle this problem, one new approach has been introduced to improve the conventional Miller compensation[10].

To gain further insight into this new approach, a review of the conventional Miller compensation is presented first. As shown in Fig. 6(a), A_{V1} and A_{V2} represent two stages of the OPAMP. R_Z and C_C are incorporated in series to form Miller

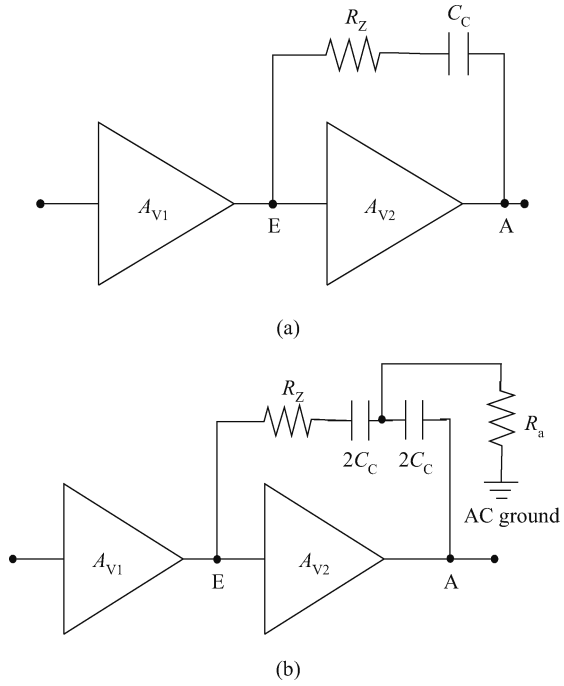

Fig. 6. (a) Conventional Miller compensation. (b) Proposed Miller compensation.

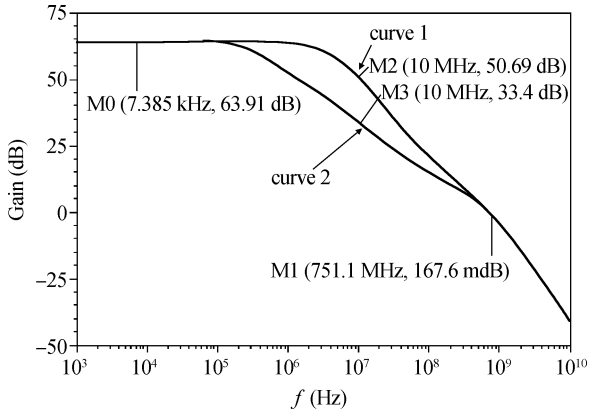

Fig. 7. Simulated frequency response of the OPAMP.

compensation. Due to Miller effect, C_C founds an equivalent capacitor at node E, whose value is $(1+A_{V2})$ times bigger than C_C. The dominant pole at node E and the non-dominant pole at node A are separated from each other much farther than they were before compensation. This effect on poles is called pole splitting, which is beneficial for gaining high PM. R_Z is used to cancel the effect of right half-plane zero (RHZ) introduced by the feedforward path of C_C.

As illustrated in Fig. 6(b), the proposed approach based on conventional Miller compensation can attain higher gain at 10 MHz and extend closed-loop bandwidth at the cost of a small increase in die area. Since the equivalent impedance of $2C_C$ is much higher than R_a at low frequency, most of the feedback current from node A flows to the ac ground through R_a. At high frequency, the influence of R_a could be neglected due to its much higher impedance value compared to the impedance of $2C_C$. A similar frequency response to the conventional Miller compensation at high frequency can be obtained. R_3 in Fig. 5

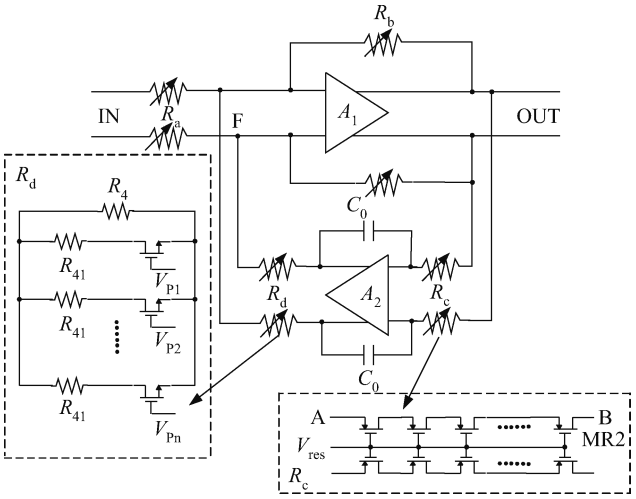

Fig. 8. Simplified architecture of VGA and its DCOC loop.

is used for keeping the CMFB loop stable. A comparison result of the open-loop frequency response of the OPAMP with the conventional and the improved Miller compensation is given in Fig. 7.

2.3. DCOC circuit design

In order to solve the DC offset problem, the AC-coupling method may be regarded as an intuitive solution, and it requires huge capacitor area and accompanied unavoidable in-band loss. The second method for removing DC offset is continuous time feedback as shown in Ref. [11]. The output voltage is sensed by the RC filter and cancelled via a feedback loop with an amplifier. Continuous-time feedback is adopted to realize a high-pass characteristic. The proposed approaches are realization of a large-value capacitor or resistor to implement a high-pass filter with a low cutoff frequency, which are costly for huge chip size. To minimize the chip size, a larger resistor or capacitor should be implemented outside the die. Using the external components needs the additional pin and increases the application dimension.

To solve the above problems, we proposed an improved DC offset cancellation circuit which is based on continuous time feedback technique. At the same time, the Miller effect and a linear range operation MOS transistor are used to realize a large-value floating capacitor and resistor, respectively. The proposed approach is realization of a large-value floating capacitor and large-value resistor to implement a high-pass filter with a low cutoff frequency.

Simplified architectures of one stage of VGA and its DCOC loop are shown in Fig. 8. Stage 2 employs a similar architecture. A_1 is the main amplifier, and A_2 is the feedback amplifier. C_0 is used as Miller capacitor and the equivalent capacitance C_1 approximates to the product of the compensation capacitor C_0 and the gain of A_2, as described in the following equation.

$$C_1 = (1 + A_2)\, C_0 \approx A_2 C_0. \tag{3}$$

As can be seen in Fig. 8, VGA output DC offset voltage at low frequency is extracted by the low-pass filter formed by R_c and C_1 at first, and then is amplified by A_2, and converted to feedback current at node F through R_d, which has opposite phase with the offset current in the VGA core to nullify the DC offset current.

Without large die area consumption, a large capacitance C_1 and resistance R_c are obtained with a small capacitor C_0 whose value is set as 3 pF and linear range operation transistor in this design, respectively. The transfer function of VGA and DCOC loop can be derived as

$$H(s) = \frac{V_o}{V_i} = \frac{\left(-\dfrac{R_b}{R_a}\right)(s + \omega_0)}{s + \left(A_2 \dfrac{R_b}{R_d} + 1\right)\omega_0}, \tag{4}$$

and

$$\omega_0 = \frac{1}{R_C C_1} = \frac{1}{C_0 R_C A_2}. \tag{5}$$

Generally, $A_2 R_b / R_d$ is much larger than 1. Hence, the high pass cutoff frequency can be expressed approximately as

$$\omega_{HPF} = \left(A_2 \frac{R_b}{R_d} + 1\right)\omega_0 \approx A_2 \frac{R_b}{R_d}\omega_0 \approx \frac{R_b}{C_0 R_C R_d}. \tag{6}$$

From Eq. (6), we can see ω_{HPF} is decided by R_C, C_0 and R_b/R_d, in order to achieve lower ω_{HPF}, we need increase R_C, C_0 or R_b/R_d. Considering that a required HPCF is below a few hundred Hz, from Eq. (6), the DC offset cancellers in Fig. 8 need a few MΩ resistance which is the cause of increasing chip size and ultimately unit cost. To solve this problem, a few MΩ resistance can be implemented with the linear range operation transistor as shown in Fig. 8.

In Fig. 8, resistor R_C (dashed line), we design $V_{GS} > V_{TH}$ and $V_{DS} \ll 2(V_{GS} - V_{TH})$, the MOS transistor operates in linear range, the current is as follows:

$$I_{DS} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})\, V_{DS}, \tag{7}$$

where V_{DS} is drain-to-source voltage of the MOSFET and V_{TH} is thermal voltage. From Eq. (7), we can see the current I_{DS} is linear of V_{DS}, this linear relation means the channel of source to drain can be seen as a linear resistor. Therefore, the resistance of MOS channel under this state is as follows:

$$R_{on} = \frac{1}{\mu C_{ox} \dfrac{W}{L} (V_{GS} - V_{TH})}. \tag{8}$$

From the above equation, the resistance of MOS operating linear region in depend upon W/L, V_{GS}, V_{TH} and temperature. Therefore the resistance MOS channel is varied by PVT (process, supply voltage and temperature). The channel resistance of MOS strongly varies with temperature and this resistance is also affected by the process variation, especially V_{TH} variation which deteriorates the yield of fabricated IC. To solve the PVT problem, the MOS channel resistance value is made by the current ratio of through reference resistor and MOS channel[12,13]. Figure 9 shows a self-resistance calibration circuit. The circuit maintains that both end voltages of MOS (MR_1) are equal to that of the resistor (R_R). The bias condition of MOS for a large resistance refers to the bias condition of MR_1 in Fig. 9. The resistance of the MOS channel is maintained by changing the V_{GS} or W/L. The R_C on the fabricated VGA cell in Fig. 8 is as follows:

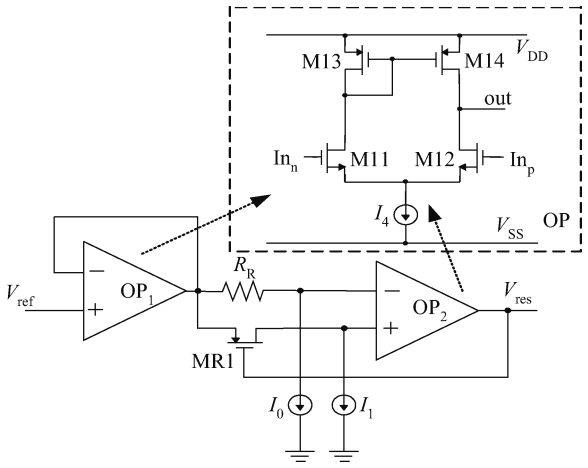

Fig. 9. Linear range resistor with calibration circuit.

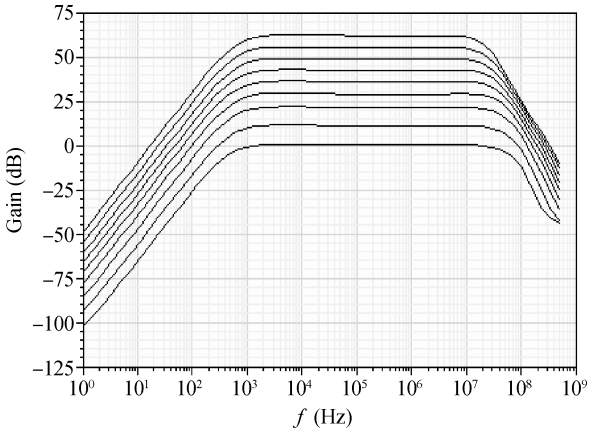

Fig. 10. Frequency response of VGA with DCOC loops.

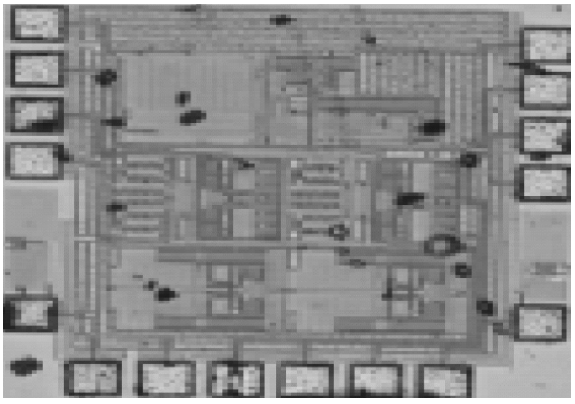

Fig. 11. Die photograph of the proposed VGA and DCOC.

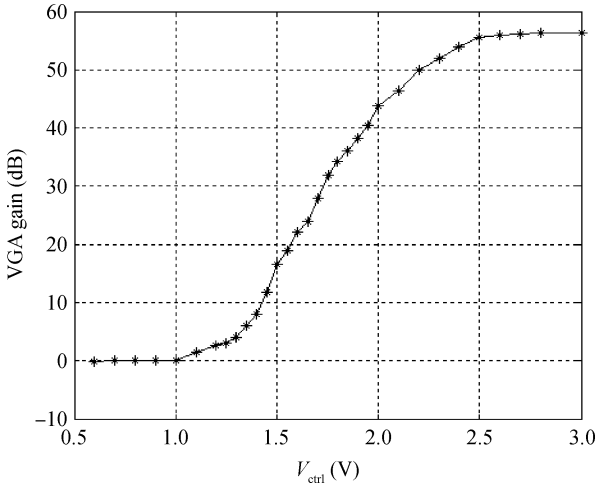

Fig. 12. Measured gain versus control signal of the VGA.

$$R_C = R_R \frac{I_0}{I_1} \frac{L_2/W_2}{L_1/W_1} M, \tag{9}$$

where R_R is the reference resistor, I_0 and I_1 are current for R_R and MR1, L_1 and L_2 are length of MR1 and MR2, W_1 and W_2 are width of MR1 and MR2, M is the number of series transistors for R_C. R_C is referred to R_R.

Considering the continuous-time feedback DC offset canceller, the HPCF of DC feedback is varied with the gain of the amplifier. In order to overcome the disadvantage of a higher gain with a higher HPCF, we keep the value of R_b/R_d constant to make ω_{HPF} independent of VGA gain changing in this design.

In addition to ω_{HPF}, DC attenuation can also be obtained from the transfer function as

$$H(0) = \frac{-R_b/R_b}{A_2\,(R_bR_d) + 1} = \frac{-R_b/R_a}{A_2\,(R_b/R_d) + 1}. \tag{10}$$

So the relative DC attenuation can be expressed as

$$\frac{\dfrac{-R_b/R_a}{-R_b/R_a}}{A_2(R_b/R_d) + 1} \approx A_2(R_b/R_d). \tag{11}$$

Table 1. Summary of the proposed VGA measured performances.

Parameter	Value
Technology	0.13 μm CMOS
Supply voltage	1.2 V
dB-linear gain range	0–57 dB
BW3dB	> 10 MHz
IIP3 (0 dB)	10 dBm
IIP3 (57 dB)	−48 dBm
NF (30 dB)	16 dB
NF (57 dB)	15 dB
AGC settling time	0.2 μs
Residual DC offset	2 mV
I_{total}	3.7 mA
VGA current	2.5 mA
Ramp current	0.2 mA
DCOC current	1 mA

Equation (11) indicates that the relative DC attenuation is constant regardless of the VGA with different voltage gain if the ratio R_b/R_d is constant, and thus the HPCF of DC feedback loop is constant with gain variation. We can change either A_2 or the constant (R_b/R_d) to get the appropriate relative DC attenuation. Figure 10 demonstrates the simulated frequency response of the VGA with DCOC loops.

Table 2. VGA performance comparison.

Parameter	This work	Ref. [14]	Ref. [15]	Ref. [16]	Ref. [5]
Technology (μm)	0.13	0.35	0.18	0.18	0.18
Die area (mm^2)	0.58	2.55	0.42	—	0.4*
V_{dd} (V)	1.2	3.3	1.8	1.8	1.8
I(mA)	3.7**	9.1**	11.4	12.2	3.6
Gain range (dB)	0–57	0–60	–39 to 55	–30 to 65	–52 to 43
Gain error (dB)/Linear gain (dB)	±1 /50	—	±1 /79.4	±2 /90	±1 /90
V_{ctrl} (V)	0.8–2.5	0–2.5	0.15–1.5	0.7–0.9	0.4–1.4
BW3dB (MHz)	> 10	⩾ 2.87	⩾ 4	⩾ 400	⩾ 32
IIP3 (dBm)	−48 to 10	−4 to 16.2	−59 to −11***	−35 to 10	−48 to −17***
NF (dB) /max gain	15	5.2	6.8	13.8	—
DCOC f_c (Hz)	500	67K	—	—	—
Residual offset (mV)	2 mV/55 dB	8 mV/60 dB	—	—	—
Year (Ref.)	—	2009	2007	2007	2006

*Chip area excluding bondpads. **VGA and DCOC current. *** P_{1dB} value.

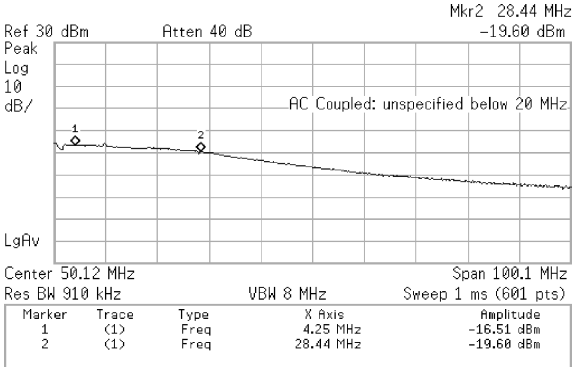

Fig. 13. Measured frequency response of the VGA.

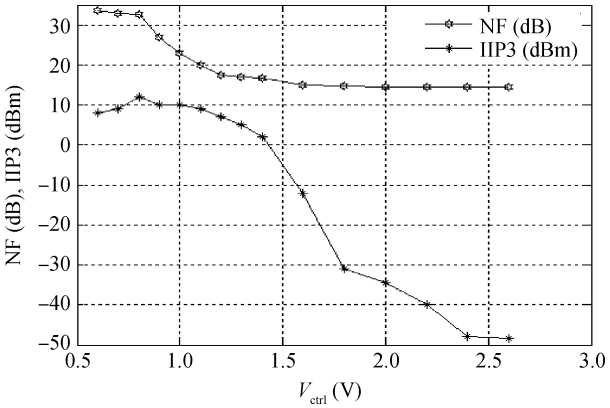

Fig. 14. VGA NF and IIP3 measurement results.

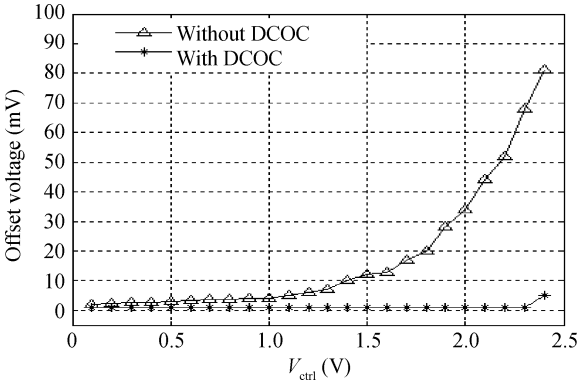

Fig. 15. Measurement results of DC-offset at the output of VGA.

3. Measurement results

The proposed VGA has been implemented in SMIC 0.13 μm CMOS technology with the supply voltage V_{DD} = 1.2 V, and the DC current is 3.7 mA. Figure 11 shows the die micrograph of the proposed VGA, the VGA die area is 740 × 780 μm^2 including bondpads. Figure 12 shows the measured gain characteristics at a frequency of 4 MHz as a function of control voltage V_{ctrl}. The VGA has 57 dB (0–57 dB) linear-in-decibel gain characteristics when the control voltage range of 0.8–2.5 V. Figure 13 shows the frequency response of the proposed VGA at 30 dB gain settling. The measured bandwidth of the VGA is up to 10 MHz with a gain control range of 57 dB.

The measured input third intercept point (IIP3) and noise figures of the proposed VGA are presented as a function of the control voltage in Fig. 14. The IIP3 varies from 10 to –48 dBm. It is maximized at the minimum gain state and, as the gain increases, it decreases so that decreasing the allowable input signal swing results in the reduction of P_{1dB}, as shown in Fig. 14. The minimum NF is 15 dB at a maximum gain of 57 dB and the NF increases as the gain decreases.

The proposed DCOC technique shows good cancellation capability in test, as shown in Fig. 15. The residual DC offset measured at the output of VGA is less than 2 mV.

The measurement results are summarized in Table 1 and a comparison with previous studies is given in Table 2. From the comparison, we can see the proposed VGA design achieves a large dynamic range, good noise performance and IIP3 with comparable power consumption. Moreover, it can remove dc offset with accelerated setting time.

4. Conclusion

A low-power high-linearity dB-linear VGA with a novel DC offset cancellation technique is proposed. An OPAMP utilizing an improved Miller compensation approach is adopted in the VGA design. By adopting the differential-ramp based technique to enhance the linearity, the IIP3 is 2 dBm at 10 dB

gain setting. Moreover, the DC offset canceller use the Miller effect and a linear range operation MOS transistor to realize large capacitance and resistance. This proposed DCOC technique requires no external components and demonstrates good cancellation capability. Since there is no need for large capacitance and resistance, the chip area is small and suitable for IC integration.

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