

Total dose irradiation and hot-carrier effects of sub-micro NMOSFETs

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Abstract: Total dose irradiation and the hot-carrier effects of sub-micro NMOSFETs are studied. The results show that the manifestations of damage caused by these two effects are quite different, though the principles of damage formation are somewhat similar. For the total dose irradiation effect, the most notable damage lies in the great increase of the off-state leakage current. As to the hot-carrier effect, most changes come from the decrease of the output characteristics curves as well as the decrease of trans-conductance. It is considered that the oxide-trapped and interface-trapped charges related to STI increase the current during irradiation, while the negative charges generated in the gate oxide, as well as the interface-trapped charges at the gate interface, cause the degradation of the hot-carrier effect. Different aspects should be considered when the device is generally hardened against these two effects.

Key words: sub-micro; total dose irradiation; hot-carrier effect

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1. Introduction

Advances in VLSI technology have driven MOS devices to deep sub-micro and even nano scales. Besides the advantages of low power and high speed, the thinning of the gate oxide has greatly enhanced the radiation hardness of MOS devices^[1]. However, some new problems will threaten the performance of devices used in space, such as the decrease of feature size. Issues of current leakage due to irradiation^[2,3] and reliability problems^[4] resulting from high electrical fields are two important aspects, and will be discussed in this paper.

As the gate oxide is much thinner than before, some parameters, such as threshold voltage or trans-conductance, may have better tolerance to radiation. However, previous works^[5,6] have shown that problems related to current leakage due to irradiation still exist and are even more severe in small devices. These factors will enlarge the consumption current and finally threaten the reliability of circuit. Research on the total dose irradiation effect is important to the application of sub-micro devices.

In addition, there are several reliability problems^[7,8] that arise due to the high electric field in sub-micro devices, as the supply voltage is not scaling down according to the device size. The hot-carrier effect is one of these issues. Hot carriers may yield interface traps at Si/SiO₂ interface, be trapped in the oxide or generate new oxide traps, all of which can degrade the device performance over time and finally invalidate the device or circuit^[9-11]. The hot-carrier effect has become one of the most important factors that limit the lifetime of VLSI and the maximal device densities^[12].

The principles of damage formation for total dose irradiation and the hot-carrier effect are similar, while both of them

degrade the device parameters by inducing trapped charges in the oxide or at the oxide/bulk interface. As two important problems affecting sub-micro devices, the manifestations of the damage they induce and the way they affect the device must be discovered. This is of great significance to the general hardness and damage evaluation of total dose irradiation and hot-carrier damage. In this paper, total dose irradiation and hot-carrier effects of sub-micro NMOSFETs are contrastively studied, and the mechanisms of the trapped charge that influences the device parameters are analyzed. It will provide technical support for the total dose and hot-carrier hardness of the sub-micro devices used in space.

2. Experiment

The studied samples are NMOSFETs with a 0.25 μm process, while the width/length of the channel is 0.3/0.24 and the gate oxide is 5 nm. Total dose irradiation and hot-carrier stress experiments are performed on the samples.

The total dose irradiation experiment: samples are irradiated up to 50, 100, 300, 500, 800, 1000, 1200 and 1500 Gy(Si) with ⁶⁰Co γ -rays at the Xinjiang Technical Institute of Physics & Chemistry, Chinese Academy of Sciences, with a dose rate of 0.5 Gy(Si)/s. The bias condition during irradiation is the ON state for the NMOSFET, i.e. $V_G = 2.5$ V, $V_S = V_D = 0$ V. Electrical measurements are obtained prior to irradiation and after step-stress irradiations.

The hot-carrier stress experiment: the stress voltage is chosen to maximize the substrate current, as $V_D = 3.5$ V, $V_G = 1.8$ V for samples in this paper. We periodically interrupted the electrical stresses according to logarithmic time to measure characteristics curves in order to obtain the main parameters.

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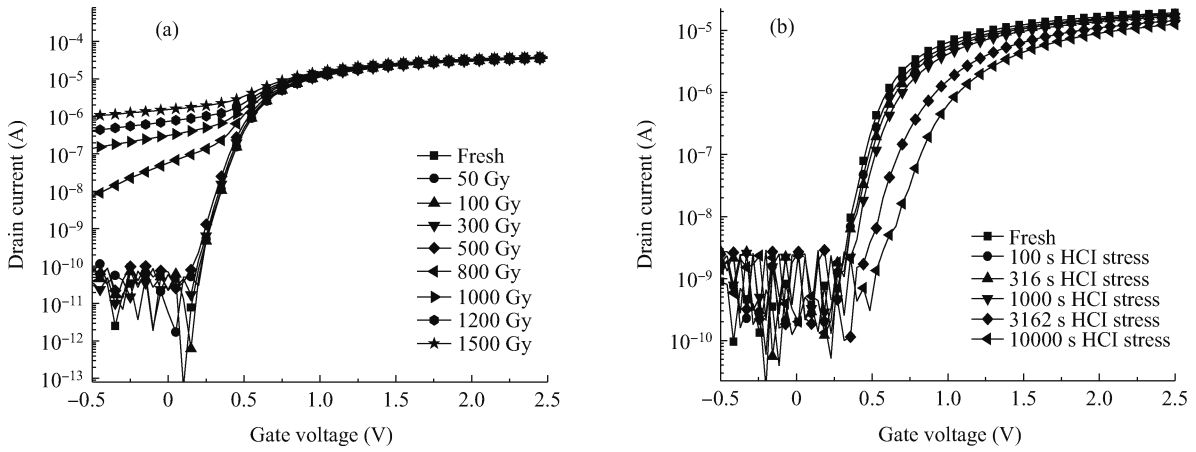


Fig. 1. Sub-threshold curves altering with (a) total dose and (b) HCI stress.

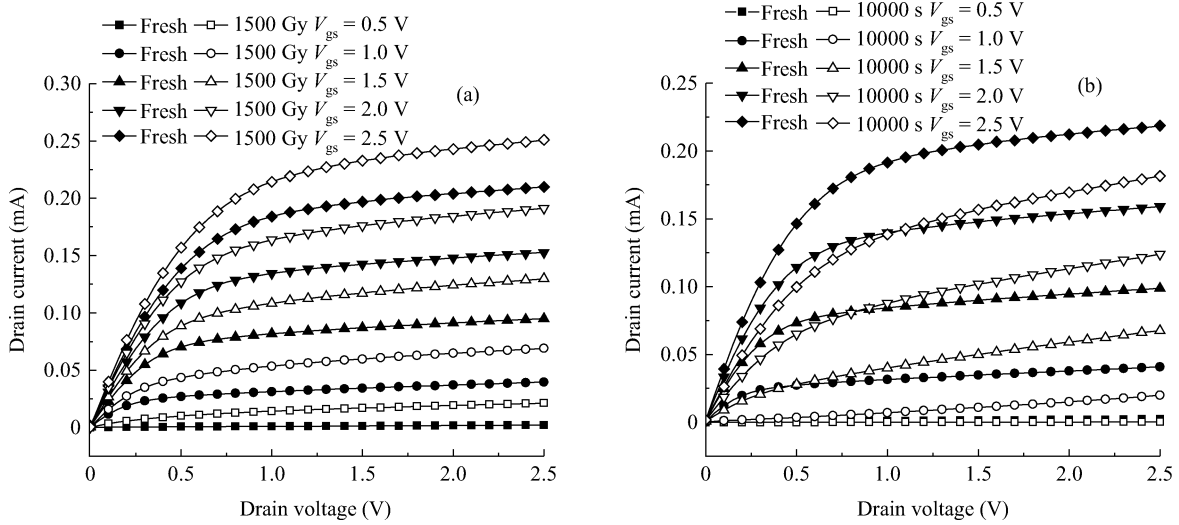


Fig. 2. Output characteristics curves changing with (a) total dose and (b) HCI stress.

3. Experiment results

Figure 1 shows the sub-threshold characteristics altering with total dose and HCI stress time. It is clearly seen that the off-state leakage current is greatly elevated during irradiation, while the threshold voltage changes little. Contrastively, after HCI stress, there is no obvious increase of the off-state leakage current but the threshold voltage shifts a great deal, going with the sub-threshold slope decreasing.

Figure 2 shows the output characteristic curves changing with total dose and HCI stress time. We can see that the curves integrally shift up after irradiation, while after HCI stress not only do the curves shift down but also the slope increases, meanwhile the current in the saturation region can not be saturated.

The trans-conductance curves after total dose and HCI stress are shown in Fig. 3. We can find that the trans-conductance only increases a little during irradiation. Contrastively, the trans-conductance decreases significantly after HCI stress and the whole curves greatly shift positively.

The manifestations of the damage that these two effects induced are quite different, as the experiments results show: radiation enormously enhances the off-state leakage current, which

can add to the power dissipation and threaten the reliability of devices and circuits. HCI stress can significantly reduce the trans-conductance and current between the source and drain, as well as accrete threshold voltage. In addition, the current in the saturation region can not be saturated, which does not occur in the radiation experiment.

4. Discussion

4.1. Total dose irradiation effect

When a device is irradiated, electron-hole pairs are created in the oxide. The separation, transportation and reaction of the electron-hole pairs can generate excessive charges, such as oxide-trapped charge and interface-trapped charge, which can affect the device parameters^[13]. Using the sub-threshold $I-V$ characteristic technique, these two kinds of trapped charges can be measured separately. It is believed that the slope of the sub-threshold curve is determined by the amount of interface traps and the shift along X axis of the curve is most related to the oxide traps^[14, 15]. For example, the small change of sub-threshold slope in Fig. 1(a) indicates that there are few interface traps generated during irradiation and the small shift of the

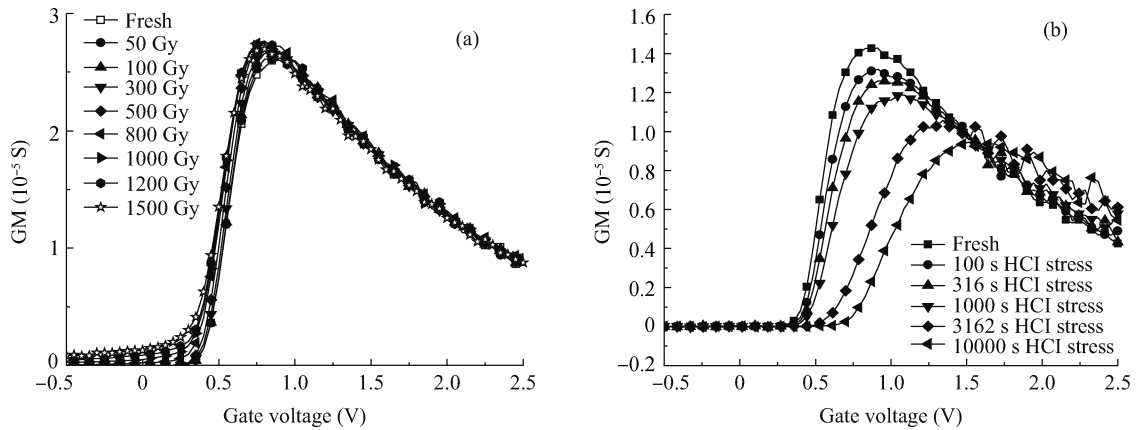


Fig. 3. Trans-conductance curves after (a) total dose and (b) HCI stress.

trans-conductance curve in Fig. 3(a) implies that there are few oxide-trapped charges in the gate oxide.

Figure 1(a) shows that the most significant change after irradiation is the elevation of the off-state leakage current; at least four decades' worth of increase is evident. The leakage current has become an important issue for MOS performance.

The increase of current can result from two aspects, the influence of the gate oxide or the isolation oxide, i.e. the STI here. However, the small altering of threshold voltage and trans-conductance shown in Figs. 1(a) and 3(a) indicates that the charges from the gate oxide are not sufficient to enhance the current to such a degree, and the gate oxide can not be main factor for the current increasing. Therefore, the leakage current mainly comes from the STI oxide.

When the device is irradiated, there will be a mass of oxide-trapped and interface-trapped charges generated at the STI oxide or at the oxide/bulk interface, which is much more than that of gate oxide due to its softer and thicker oxide layer. These excessive charges can form a leakage passage at the contact region between the channel and the STI along both sides of channel width^[1, 16]. The leakage passage will increase the off-state leakage current. The current increment in the saturation region in Fig. 2(a) is also due to the addition of leakage current from the STI passage.

In fact, as the gate oxide is much thinner than before, close to or below 5–10 nm, the impact of the gate oxide during irradiation is extremely low, and the STI is becoming the Achilles' heel of modern MOSFETs with respect to radiation hardness. Considering the millions of transistors included in VLSI, the influence of the STI on radiation must be paid much more attention.

4.2. Hot-carrier effect

The operating voltage scales less rapidly than the feature size, causing increasing electrical fields inside the device. The carriers may get enough high kinetic energy to be "hot carriers" in the high field. Hot carriers can lose energy through impact ionization and yield a large substrate current. Meanwhile the carriers generated from impact ionization can also become hot carriers. Hot carriers can gain sufficient energy to surmount the Si–SiO₂ barrier or tunnel into the oxide layer, inducing trapped charges in the oxide or at the interface. The generated trapped

charges can degrade parameters and finally reduce the reliability of the device over time. Previous works^[17–19] have pointed out that the hot-carrier effect can be classified to three stress regions, near the critical point of saturation ($V_{gs} \geq V_{ds}$), the saturation state ($V_{gs} \approx V_{ds}/2$), and just entering strong inversion ($V_{gs} \approx V_{ds}/4 - V_{ds}/2$).

The biggest damage caused by HCI is the lowering of trans-conductance, as shown in Fig. 3(b). It is believed that in the medium gate voltage stress region, the device is at a saturation state, having a large impact ionization rate and inducing abundant hot carriers. The generation of interface-trapped charges can reach a peak value and then reduce the trans-conductance a great deal. The reduction of the maximal trans-conductance comes from the effect of interface-trapped charges, while the shift of curves is due to the influence of oxide-trapped charges. As seen in Fig. 1(b), the decrease of sub-threshold slope reflects the generation of interface-trapped charges, while the shift of whole curves reveals negative charges in the oxide^[14]. When the channel is short enough, positive and negative charges will be induced in the PN depletion region near the drain boundary and in the channel, increasing the electrons in the channel region^[20], then, the channel resistance is decreased and the current increases when the voltage between the source and drain increases, as seen in Fig. 2(b).

4.3. Summary

The injection of trapped charges for total dose irradiation and the hot-carrier effect is discussed and contrasted. Charges from the STI region form the leakage passage and then enhance the current during irradiation. As to the hot-carrier effect, the negative charges generated in the gate oxide, as well as the interface-trapped charges, are the reasons for parameter degradations.

5. Conclusions

The principles of damage for total dose irradiation and the hot-carrier effect are similar, since they both change parameters through inducing trapped charges in the oxide or at the oxide/bulk interface of a device. These two effects are important issues affecting the reliability of sub-micro devices and circuits. However, the manifestations of the damages they induce

are quite different. The experimental results in this paper show that the main problem of the total dose effect is the off-state leakage current, while for the hot-carrier effect, degradations of transconductance and the current between source and drain, as well as threshold voltage, are all obvious. Through charge analyzing, it is found that the oxide-trapped and interface-trapped charges due to the STI is the main reason for current leakage during irradiation, while the oxide-trapped and interface-trapped charges related to the gate oxide are responsible for the degradation of the hot-carrier effect.

For sub-micro MOSFETs, the gate oxide is now much thinner than before. The STI is becoming the Achilles' heel of modern MOSFETs with respect to radiation hardness; however, the main issue for hot-carrier hardness remains the gate oxide and its interface. For MOS transistors of different sizes, the rule can be similar. Therefore, different aspects must be considered when devices are hardened against these two effects.

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