A 3 to 5 GHz low-phase-noise fractional-N frequency synthesizer with adaptive frequency calibration for GSM/PCS/DCS/WCDMA transceivers*

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Abstract: A low-phase-noise Σ–Δ fractional-N frequency synthesizer for GSM/PCS/DCS/WCDMA transceivers is presented. The voltage controlled oscillator is designed with a modified digital controlled capacitor array to extend the tuning range and minimize phase noise. A high-resolution adaptive frequency calibration technique is introduced to automatically choose frequency bands and increase phase-noise immunity. A prototype is implemented in 0.13 μm CMOS technology. The experimental results show that the designed 1.2 V wideband frequency synthesizer is locked from 3.05 to 5.17 GHz within 30 μs, which covers all five required frequency bands. The measured in-band phase noise are –89, –95.5 and –101 dBc/Hz for 3.8 GHz, 2 GHz and 948 MHz carriers, respectively, and accordingly the out-of-band phase noise are –121, –123 and –132 dBc/Hz at 1 MHz offset, which meet the phase-noise-mask requirements of the above-mentioned standards.

Key words: phase-locked loop; loop stability analysis; voltage controlled oscillation; phase noise
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1. Introduction

The wireless communication market is undergoing a transition from 2G to 3G and thus a multi-mode mobile handset that supports both generation standards is necessary to cater for users' ever increasing demand for wireless connectivity that enables them to access a network anywhere, anytime, seamlessly. To design such a system, a high-performance frequency synthesizer generating LO signals covering different standards is one of the most challenging parts.

In this paper, a low-noise wideband frequency synthesizer with adaptive frequency calibration is proposed which covers GSM/DCS/PCS/WCDMA bands for both transmitter and receiver. The frequency plan and system architecture are introduced. The detailed circuit implementation of the low-K_{VCO} low-phase-noise VCO, the high-resolution quick-converging adaptive frequency calibration (AFC) technique and other optimized building blocks are presented.

2. Frequency plan and system architecture

The frequency specifications for GSM and WCDMA standards are listed in Table 1. The designed multi-mode frequency synthesizer has to be compatible with four GSM and two WCDMA standards. The minimum channel spacing is 200 kHz, which requires fractional-N architecture for reasonable reference clock frequency and loop bandwidth. To cover the whole frequency range, the VCO needs to oscillate from 3296 to 4340 MHz. This range is expanded to 3–4.8 GHz if 10% variation is taken into account. The 1800/1900/2100 bands could be obtained by divide-by-two circuits and 800/900 bands by divide-by-four circuits.

The block diagram of the proposed Σ–Δ fractional-N frequency synthesizer is shown in Fig. 1. Once the system starts, the SW1 is open, SW2 and SW3 are closed and the AFC loop is working. After the AFC is finished, the SW1 is closed and the phase-locked loop begins working. Quadrature outputs are generated by CML dividers which are shown in Fig. 1 as dividers 1 and 2.

3. Circuit design

3.1. VCO

VCO is the most important block in the frequency synthesizer system because its performance directly determines system out-of-band phase noise, the frequency tuning range, and affects the output spectrum spurs. A wideband low-phase-noise VCO is designed as presented in Fig. 2. It consists of two pairs of cross-coupled MOSFETs, which could save more power compared with its all-NMOS or all-PMOS counterparts. The tail current source is removed to compensate its shortage in voltage headroom. Inductors L_1 and L_3 are designed to resonate at the second harmonic frequency ($2\omega_0$) in parallel with the parasitic capacitors of MOSFETs to raise the tail impedance, based on the fact that only even harmonics, primarily second harmonics, flow in the common-mode path[1]. To satisfy the requirements of the multi-mode system, VCO has to cover a wide frequency range. If only using a pair of MOS varactors to tune the tank, K_{VCO} would be unacceptably large, which increases the varactor's proclivity to convert AM noise into FM noise and thus deteriorate phase-noise performance[2]. To keep K_{VCO} low, a 7-bit DCCA is added for coarse tuning.

Figure 3(a) shows the most commonly used DCCA structure, which is composed of MOS switches and fixed capacitors.

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Table 1. Multi-mode frequency synthesizer frequency plan.

Standards	Band designator (MHz)	Division ratio	Uplink (MHz)	Downlink (MHz)	Channel Spacing
GSM 800	800	4	3296–3396	3476–3576	200 × 4 kHz
GSM 900	900	4	3560–3660	3740–3840	200 × 4 kHz
DCS	1800	2	3420–3570	3610–3760	200 × 2 kHz
PCS	1900	2	3700–3820	3860–3980	200 × 2 kHz
WCDMA (US)	1900	2	3700–3820	3860–3980	5 × 2 MHz
WCDMA (EU)	2100	2	3840–3960	4220–4340	5 × 2 MHz

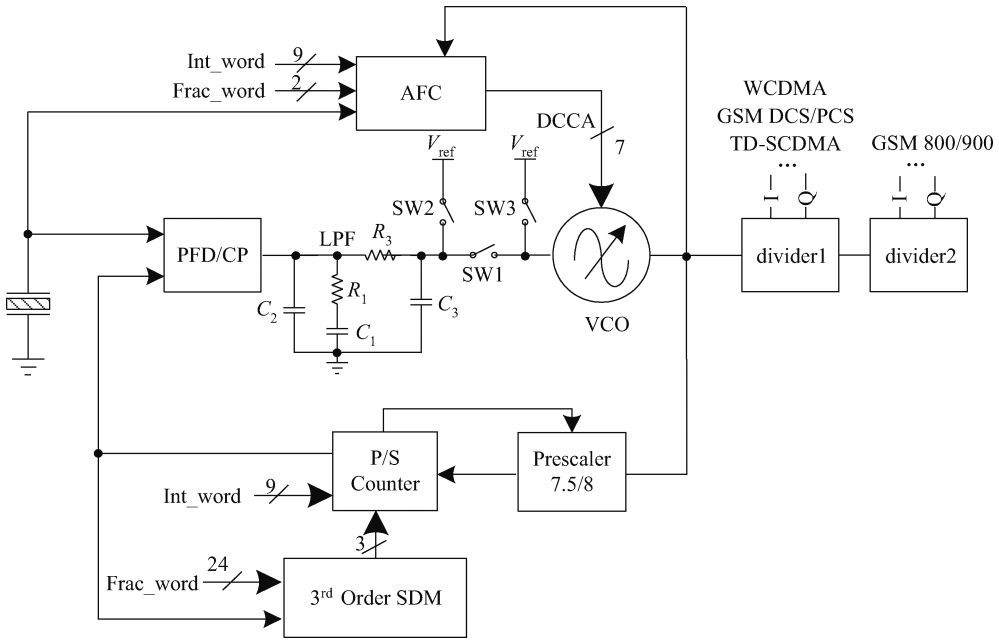


Fig. 1. Block diagram of the proposed frequency synthesizer.

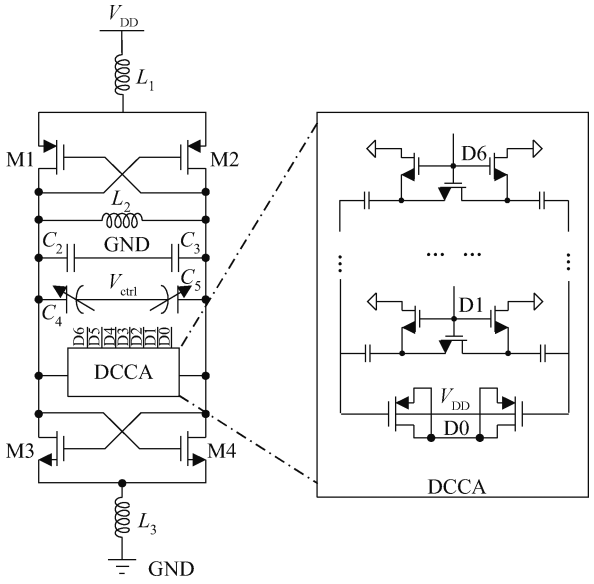


Fig. 2. Schematic of the proposed VCO.

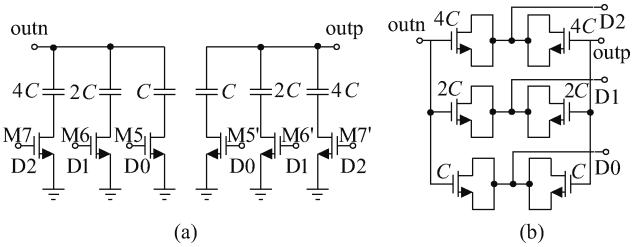


Fig. 3. Diagram of traditional DCCAs.

Taking one switched capacitor into consideration, such as M5 and its connected capacitor C, the ratio of equivalent on-state capacitance C_{ON} and off-state capacitance C_{OFF} is:

$$\frac{C_{ON}}{C_{OFF}} \cong \frac{C}{C||C_p} = 1 + \frac{C}{C_p}, \tag{1}$$

where C_p is the parasitic capacitance of MOS switch M5. From Eq. (1), it is clearly found that C_P should be much smaller than C, namely $C_P \ll C$, to minimize its impact on tuning range. However, the small size of M5 would increase its on-resistance R_{on} and thus reduce the quality factor as demonstrated in the following equation.

$$Q_{DCCA} = \frac{1}{\omega_0 R_{on} C}. \tag{2}$$

Therefore, the unit capacitor C, which directly affects K_{VCO}, cannot be made small; otherwise the specification for

tuning range and phase noise cannot be satisfied simultaneously.

To resolve this problem, varactors instead of switched capacitors are used for DCCA as shown in Fig. 3(b). However, the capacitance of the varactor varies with the voltage across it and affects phase noise by AM–FM conversion. In other words the DCCA in Fig. 3(b) is much more sensitive to power noise compared to that in Fig. 3(a) because any voltage noise in the DCCA words D_{3-0} would contribute to phase noise. The phase noise due to AM–FM conversion is expressed as follows[2]. To simplify the analysis, all varactors are treated as one big varactor.

$$L\{\Delta\omega\} \simeq \left(\frac{K_{\text{AM-FM}}}{2\Delta\omega}\right)^2 \overline{V_{\text{n}}^2} = \left[\frac{V_{\text{eff}}\omega_0}{2\Delta\omega\pi A^2 C_{\text{T}}}(C_{\max}-C_{\min})\sqrt{1-\left(\frac{V_{\text{eff}}}{A}\right)^2}\right]^2 \overline{V_{\text{n}}^2}. \quad (3)$$

In the above equations, $K_{\text{AM-FM}}$ is conversion gain, $V_{\text{eff}} = V_{\text{G}} - V_{\text{DS}} - V_{\text{T}}$, where V_{G} and V_{DS} are the gate and source/drain voltage, respectively. C_{T} is the total capacitance including varactors C_{V} and fixed capacitors C_{Fix} expressed as $C_{\text{T}} = C_{\text{V}} + C_{\text{Fix}}$. $C_{\max}$ and $C_{\min}$ are the maximum and minimum capacitances of the varactor. A is the amplitude of VCO output and $\overline{V_{\text{n}}^2}$ is the root-mean-squared (RMS) AM noise voltage spectral density on the oscillation envelope. Equation (3) shows that reducing the varactor's portion of the total capacitance ($C_{\text{V}}/C_{\text{T}}$) would improve phase noise for $C_{\max} - C_{\min}$ decreases in varactor size.

The proposed 7-bit DCCA is illustrated in Fig. 2. Bit 6 to 1 are composed of switched capacitors which are modified for a better quality factor, while bit 0 uses a PMOS varactor in I-MOS fashion. In this way, the disadvantage of switched capacitors is overcome, and varactors would not notably deteriorate phase noise as in Fig. 3(b) since $C_{\text{V}}/C_{\text{T}}$ is kept small.

3.2. AFC

The AFC technique extends the VCO tuning range together with the DCCA unit and guarantees the robustness and linearity of PLL for VCO always operating at the center of its tuning curve due to the AFC algorithm.

The proposed AFC circuit and its timing diagram are shown in Fig. 4 which is based on the open-loop calibration method[3]. The idea of the designed AFC is to obtain the information about current frequency by evaluating the difference between counted and target periods, and chooses proper DCCA words accordingly. The VCO output is first divided by M ($M \geqslant 1$). And then feeds to a counter after a switch which is controlled by a strobe signal coming from the clock generator. The strobe length is T_{meas} and it is obtained by dividing the reference clock. A buffer is inserted between the counter and the AFC core for correct reading. The AFC core unit is designed to implement AFC algorithm, including comparing target and actual frequencies and deciding the DCCA control words.

Calibration resolution f_{res} and time are the two most important characteristics for AFC. As for f_{res}, one criterion should be met first, otherwise the AFC would choose the wrong

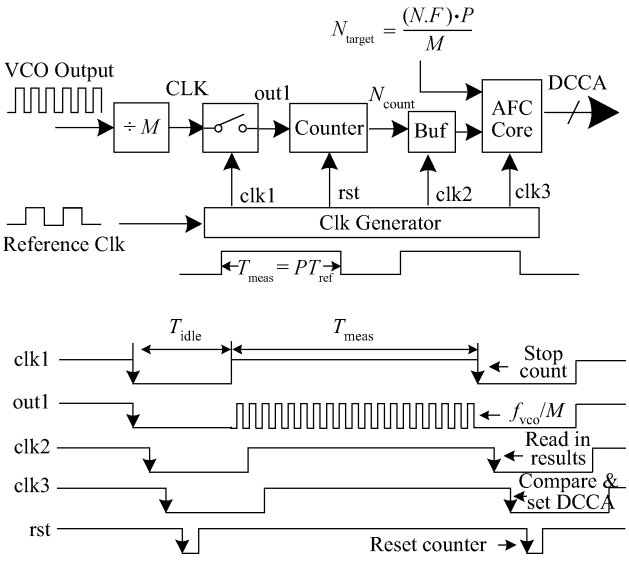


Fig. 4. The designed AFC and its timing diagram.

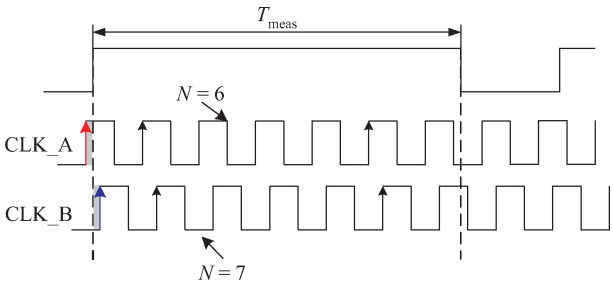


Fig. 5. Illustration of AFC random error.

band as demonstrated below:

$$f_{\text{res}} < \alpha K_{\text{VCO}} V_{\text{CP}}, \quad \alpha = 1 - \Delta f / (K_{\text{VCO}} V_{\text{CP}}), \quad (4)$$

where α is the overlap rate of VCO bands, Δf is the frequency difference of two adjacent bands, and V_{CP} is the maximum charge pump output range. According to Eq. (4), high frequency-detection resolution is necessary for low K_{VCO} design.

In this design, T_{meas} is P times larger than T_{ref} (reference clock period). And thus the ideal counting result is:

$$N_{\text{target}} = \frac{(N.F)\cdot P}{M}, \quad (5)$$

where $N.F$ is the division ratio, N is the integer part and F represents the fractional part. Equation (5) shows that N_{target} would probably be a non-integer, but the actual counted number N_{count} is obtained from counters and has to be an integer. Therefore, the resolution is limited. The division ratio resolution is given as:

$$(N.F)_{\text{res}} = \frac{M}{P}. \quad (6)$$

Accordingly, the frequency resolution can be expressed as follows:

$$f_{\text{res}} = f_{\text{ref}}\frac{M}{P}. \quad (7)$$

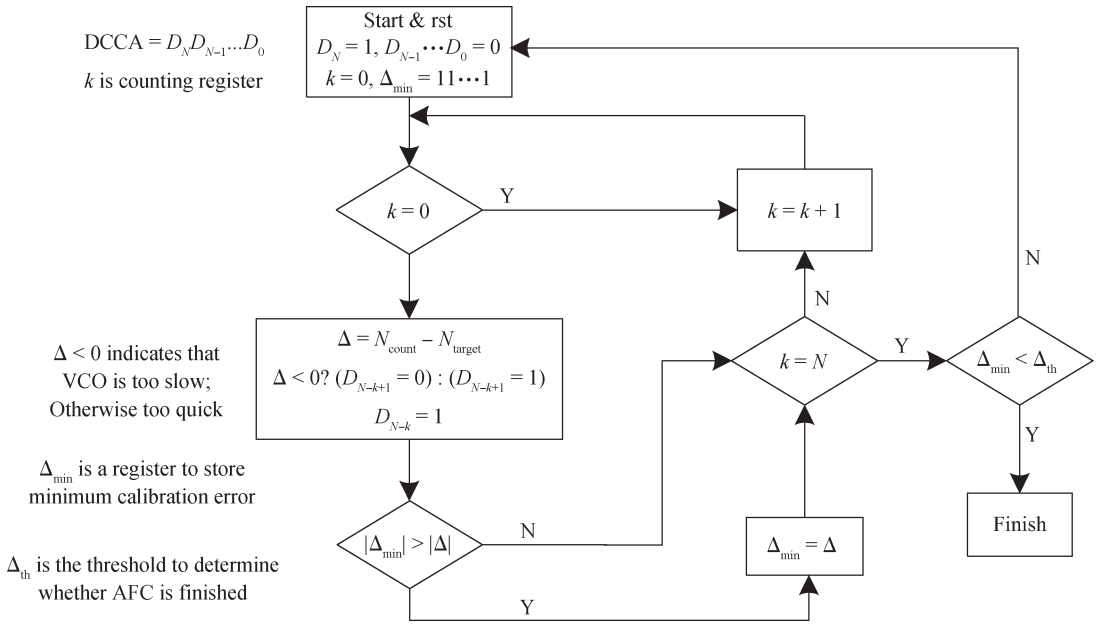


Fig. 6. Flowchart for the AFC algorithm.

This kind of error is called fractional error which is caused by fractional division. Another kind of error is the random error illustrated in Fig. 5. Because of the indetermination of initial phases, CLK_A counts one less cycle than CLK_B, as in this example. Therefore, a minimum difference between N_{count} and N_{target} of two is required to make a right decision. As a result, Equation (7) should be revised as follows.

$$f_{\text{res}} = 2 f_{\text{ref}} \frac{M}{P}. \tag{8}$$

From Eq. (8) it is clear that to improve the AFC resolution, M and $1/P$ should be kept as small as possible. Small M means a large power consumption and large P means a long calibration time. Thus it is a trade-off among resolution, power and speed.

The flowchart of the proposed AFC algorithm is illustrated in Fig. 6. Normally an N-bit DCCA only needs N steps for the algorithm to converge, unless $\Delta_{\text{min}} > \Delta_{\text{th}}$ due to unexpected factors that make the stable time for VCO longer than anticipated and the calibration process has to be restarted. At the end of the N_{th} step, the values stored in the registers meet Δ_{min} is set as the final DCCA words. The total time needed for AFC is:

$$T_{\text{AFC}} = nN\,(T_{\text{idle}} + T_{\text{meas}})\,. \tag{9}$$

n is the number of times that the AFC algorithm is repeated and T_{idle} is the idle time deliberately left for system to be stable.

3.3. Σ−Δ modulator and other building blocks

A single-loop 3-bit third-order Σ−Δ modulator is designed for its more concentrated output bit pattern and less dependence on circuit mismatch, and thus generates less high-frequency noise and makes the system less sensitive to the substrate noise coupling[4]. The accumulator in this design is 24 bits to enhance the randomness of the output bit stream within the allowance of circuit complexity. As a result, the fractional spur is reduced. To further optimize the fractional spur performance, the PFD and CP are designed to decrease mismatch and improve linearity[5]. In order to generate required division ratios, a programmable divider is adopted that is composed of a prescaler and a P/S counter block. The dual-modulus prescaler is implemented using the phase-switching technique[6]. The division ratios are designed to be 7.5 and 8 for smaller quantization noise. And the P/S counter is asynchronous to reduce power consumption.

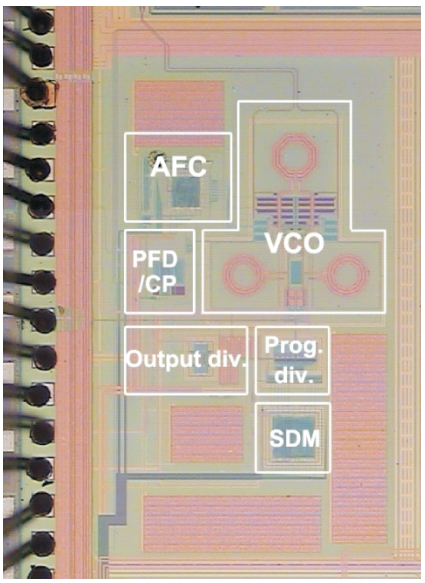
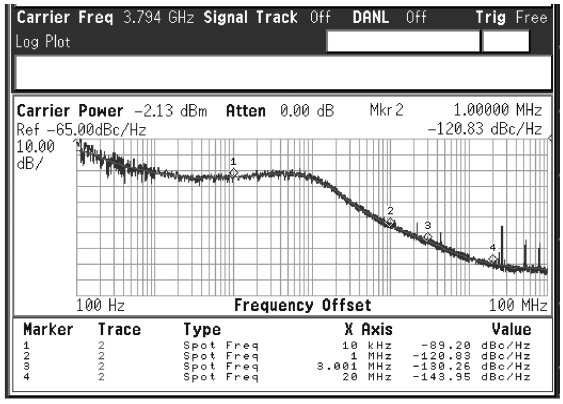


Fig. 7. Microphotograph of a manufactured synthesizer.

4. Measuremental results

The multi-mode frequency synthesizer was fabricated in 0.13 μm CMOS technology. The chip microphotograph is presented in Fig. 7. The die area is 0.8 × 1.3 mm^2 with the active core occupying about 0.57 mm^2. The measured



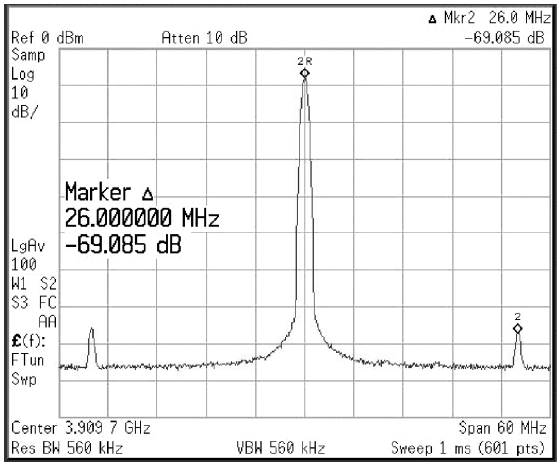


Fig. 8. Measured phase-noise and power spectrum.

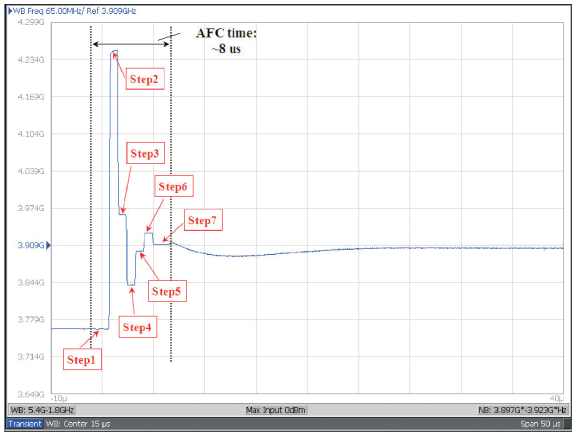


Fig. 9. Measured total lock time, including AFC and PLL phases.

VCO tuning range is 3.05–5.17 GHz which can cover all GSM/PCS/DCS/WCDMA frequency bands, and withstand temperature and process variation.

Figure 8 shows the measured closed-loop phase noise and power spectrum at VCO output. The measured in-band phase noise is less than –89 dBc/Hz with the loop bandwidth of about 100 kHz. The out-of-band noise is –121 dBc/Hz at 1 MHz offset and –130 dBc/Hz at 3 MHz offset. The reference spur level is less than –69 dBc with 26 MHz reference clock, and there is no obvious fractional spur due to proper design.

Frequency versus time is plotted in Fig. 9, which illustrates

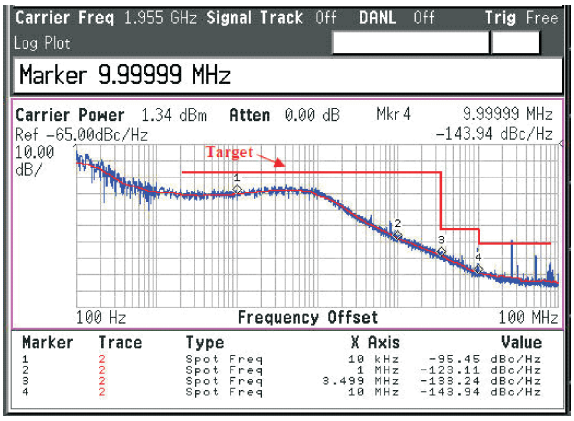


Fig. 10. Measured phase noise for WCDMA.

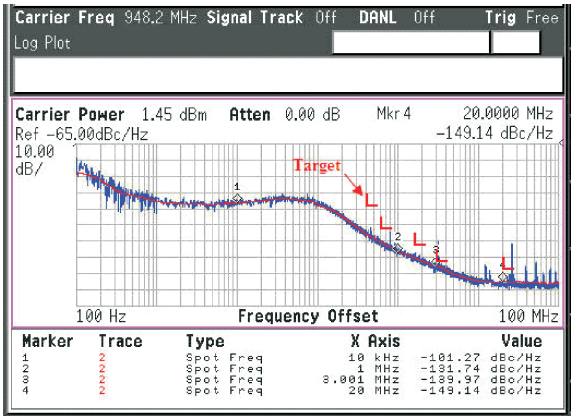


Fig. 11. Measured phase noise for GSM.

the locking process including AFC and phase locking. This is measured by an Agilent E5052B. AFC is started at -6 μs triggered by a narrow-video-band method. It is shown that the AFC runs seven steps and takes less than 8 μs to reach 6.5 MHz resolution. And the total lock time is about 30 μs to achieve 20 ppm frequency resolution.

The measured results at VCO output are summarized in Table 2 and a comparison with recently reported frequency synthesizers is made. It shows that the designed frequency synthesizer extends the frequency tuning range up to 50% without deterioration of the performance. Phase noise and reference spur level are competitive compared with similar synthesizers. Also the designed AFC runs much faster than others and helps the loop locked quickly.

The LO signals after output dividers are also measured at required frequency bands. Their phase noises are shown in Figs. 10 and 11, and the WCDMA and GSM phase noise masks[10, 11] are also plotted in the same figure shown by the solid line. Note that the GSM mask is set according to receive phase-noise requirements because our work assumes a duplex filter at the antenna. From Figs. 10 and 11, it is clearly found that the designed synthesizer can fulfill the specifications for the above-mentioned multi-mode systems.

The whole synthesizer draws about 18 mA from a 1.2 V power supply to generate a 3–5 GHz LO signal. And two-stage CML dividers at the output consume an additional 14 mA together with the output buffers.

Table 2. Performance summary and comparison.

Parameter	Ref. [7]	Ref. [8]	Ref. [9]	This work
Technology	0.25 μm BiCMOS-SiGe	0.13 μm CMOS	0.18 μm CMOS	0.13 μm CMOS
Supply voltage (V)	2.5	1.8	1.8	1.2
VCO frequency range (GHz)	3.05–4.05	3.17–4.49	1.47–2.51	3.05–5.17
Frequency resolution (Hz)	NA	1.5	100	1.5
Reference spur (dBc)	NA	–75 @ 26 MHz	–62 @ 26 MHz	–69 @ 26MHz
Phase noise (dBc/Hz)*	–73 @ 10 kHz –122 @ 1 MHz (Carrier freq. = 3.778 GHz)	–94 @ 10 kHz –145 @ 3 MHz (Carrier freq. = 900 MHz)	–92 @ 10 kHz –126 @ 3 MHz (Carrier freq. = 1.965 GHz)	–89 @ 10 kHz –121 @1 MHz (Carrier freq. = 3.794 GHz)
AFC time (μs)	No AFC	< 20	No AFC	< 8
Total lock time (μs)	$\sim$ 80	NA	NA	$\sim$ 30

* Theoretically, phase noise improves 6 dBc/Hz as carrier frequency halves.

5. Conclusion

A 1.2 V Σ–Δ fractional-N frequency synthesizer using wideband on-chip VCO and a fast AFC technique for GSM/PCS/DCS/WCDMA RF transceivers has been developed in 0.13 μm CMOS technology. The experimental results show –89 dBc/Hz in-band phase noise with 100 kHz loop bandwidth and –121 dBc/Hz out-of-band phase noise at 1 MHz offset frequency away from a 3.79 GHz carrier. The lock time is about 30 μs (20 ppm) including 8 μs AFC time and the reference spur is less than –69 dBc.

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