A 1500 mA, 10 MHz on-time controlled buck converter with ripple compensation and efficiency optimization

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Abstract: A 1500 mA,10 MHz self-adaptive on-time (SOT) controlled buck DC–DC converter is presented. Both a low-cost ripple compensation scheme (RCS) and a self-adaptive on-time generator (SAOTG) are proposed to solve the system stability and frequency variation problem. Meanwhile a self-adaptive power transistor sizing (SAPTS) technique is used to optimize the efficiency especially with a heavy load. The circuit is implemented in a 2P4M 0.35 μm CMOS process. A small external inductor of 0.47 μH and a capacitor of 4.7 μF are used to lower the cost of the converter and keep the output ripple to less than 10 mV. The measurement results show that the overshoot of the load transient response is 8 mV @ 200 mA step and the dynamic voltage scaling (DVS) performance is a rise of 16 μs/V and a fall of 20 μs/V. With a SAPTS technique and PFM control, the efficiency is maintained at more than 81% for a load range of 20 to 1500 mA and the peak efficiency reaches 88.43%.

Key words: buck converter; high frequency; large current load; efficiency; on-time control

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1. Introduction

In today's consumer market, portable battery-operated devices, such as smart-phones, tablet PCs, and personal digital assistants, are playing a more important role in people's life. As a result, a high-efficiency buck converter as a power management unit has already become an indispensable block for a whole system to extend its run time. Driven by miniaturization and low cost, the switching power converters are advancing into high frequency to further shrink the volumes of external passive devices such as inductors and capacitors. On the other hand, the increasing complexity and integration of the systems require a larger current capability of the converter to support more modules at the same time. So, high frequency, large current and high efficiency are the current trends for buck converters.

However, increasing frequency and current bring new challenges for power management IC designers. First, it imposes stricter constrains on the controller for less delay, wider bandwidth and a faster response. Hysteresis control is replacing the conventional voltage or current PWM mode in high-frequency design for its congenital simple structure, excellent dynamic characteristics and being free of complex compensation components[1]. However, its switching frequency is seriously affected by I/O voltage and propagation delay[2]. In addition, the stability is dependent on the ESR of the output capacitor. Second, the efficiency of the converter deteriorates with increasing frequency and current for more switching loss and conduction loss. Some research has been carried out in these areas. Reference [1] is an intensive study on high-frequency control and efficiency optimization, but the control mode is very complicated and needs inductor current sensing. Reference [3] tries to broaden the bandwidth of the error amplifier and reduce the delay of the comparator in Bi-CMOS technology, but the transient response is still poor with a large overshoot due to the voltage control mode. Reference [4] designs a 10 MHz open-loop converter with a high current, but the efficiency is low.

In this paper, a 1500 mA, 10 MHz self-adaptive on-time (SOT) controlled buck converter is presented, with an intensive study of system stability, frequency variation and the efficiency deterioration problem.

2. System design consideration

2.1. System architecture

The system architecture is shown in Fig. 1, which adopts the SOT control mode. The trigger signal of on-time is generated by comparing the feedback voltage (V_{FB}) and the reference voltage (V_{REF}), and the on-time of each period is controlled

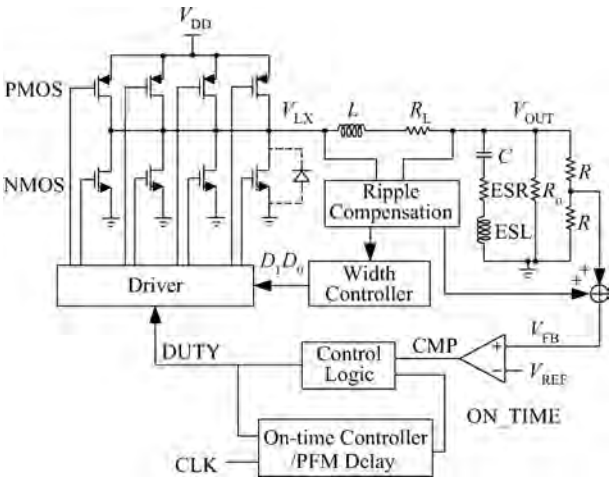

Fig. 1. System architecture of the proposed buck converter.

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Table 1. Stability analysis for different z_p ranges.

z_p range	$-1 < z_p < 0$	$0 < z_p < 1$
s-domain pole	$p_1 = \frac{\ln\lvert z_p\rvert}{T} + j\frac{\pi}{T}$, $p_2 = \frac{\ln\lvert z_p\rvert}{T} - j\frac{\pi}{T}$	$p_0 = \frac{\ln\lvert z_p\rvert}{T}$
System property parameters	$\omega_n = -\frac{\ln\lvert z_p\rvert}{T}\sqrt{1+(\pi/\ln\lvert z_p\rvert)^2}$, $\zeta = 1/\sqrt{1+(\pi/\ln\lvert z_p\rvert)^2}$	—
GBW f_g	$f_g \approx \frac{\omega_n\sqrt{1-\zeta^2}}{2\pi} = \frac{1}{2T}$	$f_g \approx -\frac{\ln\lvert z_p\rvert}{2\pi T}$
Phase margin ϕ	$\phi \approx \arccos(1-\zeta)$	90°

by a self-adaptive on-time generator (SAOTG), which is also used to lock the switching frequency. A ripple compensation block is appended to realize the stability independent of the large ESR. A segmented power transistor size is adjustable for optimizing the overall efficiency especially under a very heavy load.

2.2. System stability analysis

A dynamic model is essential in determining stability and designing a compensation circuit. Using the basic method of a sampled-data modeling technique[5], discrete small-signal model taking for this control model is developed as follows:

$$\begin{bmatrix} i_L[k+1] \\ v_c[k+1] \end{bmatrix} = \frac{A}{\Delta}\begin{bmatrix} i_L[k] \\ v_c[k] \end{bmatrix} + \frac{B}{\Delta}t_{on}, \tag{1}$$

where $i_L[k]$ and $v_c[k]$ are the inductor current and ideal capacitor voltage (without the ESR and ESL) at the beginning of the kth switching cycle, respectively, and the capital letters represent the corresponding variables in steady state:

$$\Delta = M_2 C R_c + M_1 T_{on}/2, \tag{2}$$

$$A = \begin{bmatrix} -(M_1 T_{on}/2 + M_2 T_{on}) & -M_2 C \\ (M_1 T_{on}/2 + M_2 T_{on})R_c & M_2 C R_c \end{bmatrix}, \tag{3}$$

$$B = \begin{bmatrix} M_1(M_1+M_2)T_{on}/2 \\ M_1(M_1+M_2)T_{on}R_c/2 \end{bmatrix}, \tag{4}$$

where M_1 and M_2 are the up-slope and down-slope of the inductor current and T_{on} is the on-time. The transfer function of the system is:

$$H(z) = (zI - A)^{-1}B = \frac{K}{z - z_p}, \tag{5}$$

where z_p and K are the pole and the gain of the closed-form transfer function, respectively:

$$z_p = \frac{M_2 C R_c - (M_1 T_{on}/2 + M_2 T_{on})}{M_2 C R_c + M_1 T_{on}/2}, \tag{6}$$

$$K = \frac{M_1(M_1+M_2)T_{on}R_c}{M_2 C R_c + M_1 T_{on}/2}. \tag{7}$$

With the basic property of z-transforms, set the $s = \sigma + j\omega$, then the pole z_p is:

$$z_p = e^{Ts} = e^{T\sigma}e^{jT\omega}, \quad -\pi < T_\omega \leqslant \pi. \tag{8}$$

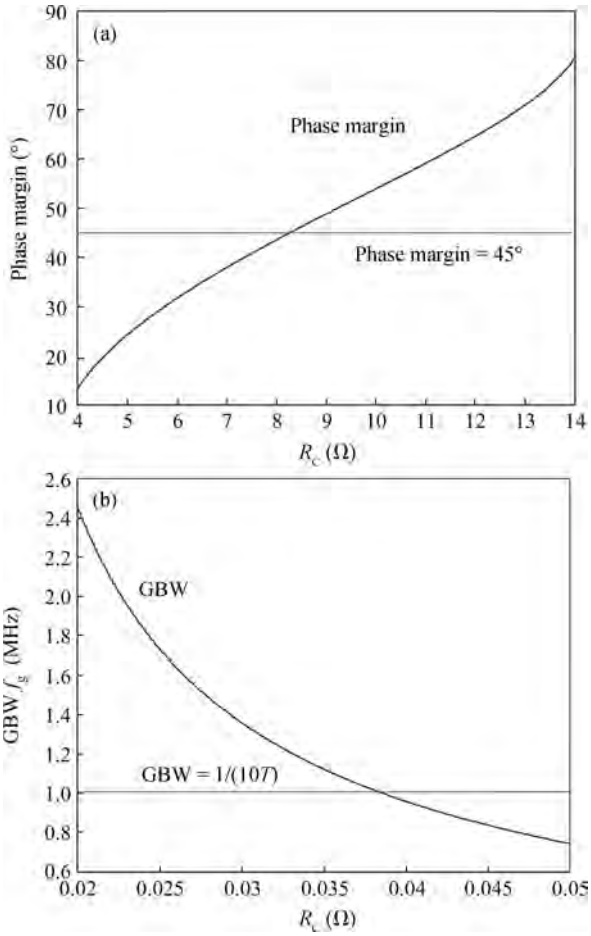


Fig. 2. (a) Relationship between phase margin and ESR when $-1 < z_p < 0$. (b) Relationship between GBW and ESR when $0 < z_p < 1$.

Since the basic stable qualification of the discrete system is $|z_p| < 1$, the stability analysis for different z_p ranges is shown in Table 1, where ω_n and ζ are the angular frequency and damping factor in quadratic pole system, respectively.

If $-1 < z_p < 0$, the GBW of the whole quadratic pole system is near to half switching frequency, so SOT control brings a very fast response speed to the converter. But the system stability is relative to ESR, as shown in Fig. 2(a). On the other hand, if $0 < z_p < 1$, the system is always stable because it is a single pole system. But the GBW is relative to ESR, as shown in Fig. 2(b). The closer $|z_p|$ to 1 is, the slower the transient response of the system. So the suitable R_c should be chosen in order to guarantee f_g larger than $1/(10T)$ to keep the relative

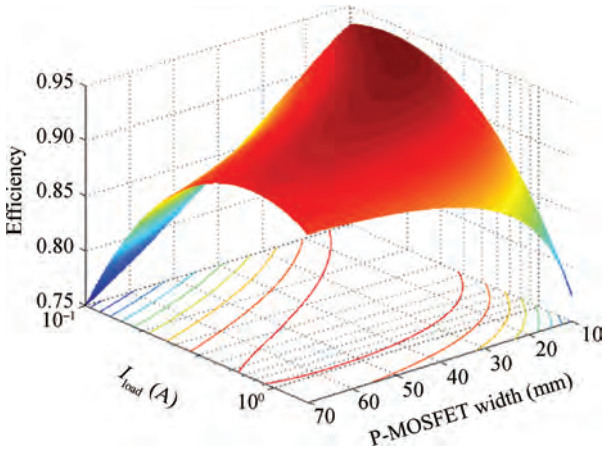


Fig. 3. 3-D plot of efficiency versus P-MOSFET width versus load current.

fast speed.

From the relationship in Fig. 2, the requirements of ESR can be derived as follows:

$$\frac{0.31M_1 + M_2}{1.38M_2C}T_{on} < R_c < \frac{0.77M_1 + M_2}{0.47M_2C}T_{on}. \quad (9)$$

So the stability and response speed of the SOT controlled buck converter are directly related to the ESR of the output capacitor. Since R_c is just a parasitic parameter, its value is variable and difficult to define or to test. On the other hand, even though enlarging the ESR can make the converter stable, it will not only slow down the response speed, but also increase the output ripple and DC error. So an RCS is proposed to ensure the system stability and response speed without the requirement of parasitic parameters.

2.3. Efficiency optimization analysis

The power consumed by a buck converter mainly consists of conduction loss, switching loss and dead-time loss, while the former two dominate the total power dissipation. According to the analysis in Ref. [6], the MOSFETs loss and total efficiency can be expressed as follows:

$$\begin{aligned} P_{pmos,total} &= P_{pmos,conduction} + P_{pmos,switching} \\ &= \frac{R_{0,pmos}}{W_{pmos}} i^2_{rms,pmos} + W_{pmos}C_{g0,pmos}V_g^2 f_s, \end{aligned} \quad (10)$$

$$\begin{aligned} P_{nmos,total} &= P_{nmos,conduction} + P_{nmos,switching} \\ &= \frac{R_{0,nmos}}{W_{nmos}} i^2_{rms,nmos} + W_{nmos}C_{g0,nmos}V_g^2 f_s, \end{aligned} \quad (11)$$

$$i_{rms,pmos} = \sqrt{D\left(I^2 + \frac{\Delta i^2}{3}\right)} \approx \sqrt{D}I, \quad (12)$$

$$i_{rms,pmos} = \sqrt{(1-D)\left(I^2 + \frac{\Delta i^2}{3}\right)} \approx \sqrt{1-D}I, \quad (13)$$

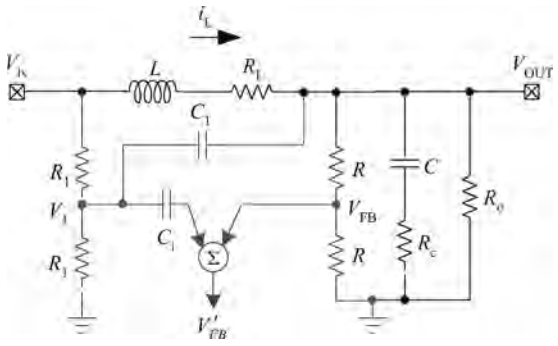


Fig. 4. Schematic of a ripple compensation scheme.

$$\eta = \frac{P_{out}}{P_{out} + P_{pmos,total} + P_{pmos,total}}, \quad (14)$$

where $R_{0,nmos}$, $R_{0,pmos}$ and $C_{g0,nmos}$, $C_{g0,pmos}$ are the conduction resistances and gate capacitances of NMOS and PMOS of unit width, respectively. D is the duty ratio of output to input voltage. The switching loss dominates with light loads while the conduction loss deteriorates the efficiency with heavy loads. In our converter the higher switching frequency and the larger load current capability make the situation worse. Fortunately the transistor size is proportional to the switching loss and inversely proportional to the conduction loss, so there is a pair of optimum sizes to make the total MOSFET loss minimum at a fixed load. In order to improve the efficiency over a full load range, we make the transistors' sizes self-adaptive to the load condition to optimize multi-load-points, according to the relationship between the efficiency and MOSFET sizes in different loads shown in Fig. 3.

3. Implementation of key blocks

3.1. Ripple compensation scheme

A ripple compensation scheme (RCS) is proposed to make the stability independent of parasitic parameters such as ESR, meanwhile maintain the low output ripple and no extra power loss, as shown in Fig. 4. By ignoring the conduct resistance of inductor L, the feedback voltage in classical buck converter without R_1, C_1 and C_i is expressed as:

$$V_{FB} = \frac{0.5V_{lx}(1 + sCR_c)}{s^2LC(1 + \frac{R_c}{R}) + s(\frac{L}{R} + CR_cR) + 1}. \quad (15)$$

At high frequency when $s << 2\pi R_oC$, $2\pi R_o/L$ and $R_c << R_o$, Equation (15) can be simplified into:

$$V_{FB} \approx \frac{0.5V_{lx}sCR_c}{s^2LC} = \frac{V_{lx}R_c}{2sL}. \quad (16)$$

For $R_1 >> 2\pi f_s L$, R_1 and C_1 parallel connected with L will not affect the power level. By omitting the low-frequency element, the feedback voltage V'_{FB} in Fig. 4 can be expressed as:

$$V'_{FB} \approx V_{lx}\frac{sLCR_oC_2/R_1}{s^2R_oC_1C_PLC} = \frac{V_{lx}}{sR_1C_1}. \quad (17)$$

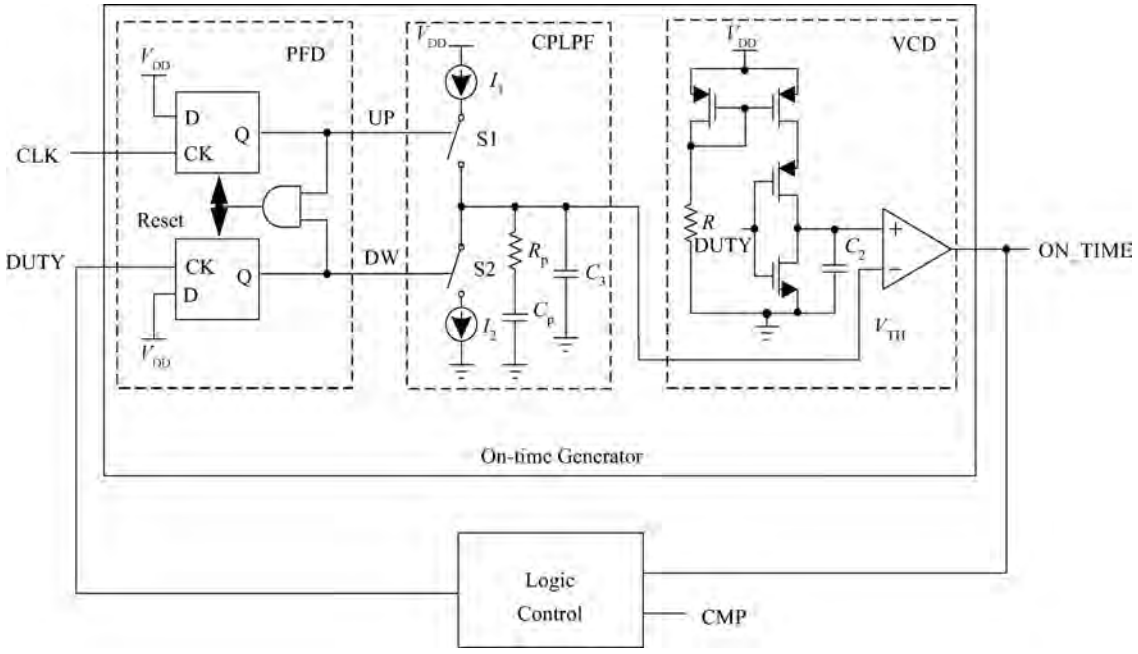


Fig. 5. Schematic of a self-adaptive on-time generator.

Comparing Eq. (17) and Eq. (16), the equivalent ESR $R_{\text{c-eq}}$ of V'_{FB} in Fig. 4 is given by:

$$R_{\text{c-eq}} \approx \frac{2L}{R_1 C_1}. \tag{18}$$

C_{i} is used to isolate the DC voltage of V_1 with that of V'_{FB}. With this method, the equivalent resistance of the feedback ripple will increase from R_{c} to $R_{\text{c}} + R_{\text{c-eq}}$, which enhances the stability, meanwhile keeps the output ripple and efficiency unchanged as the real ESR of the output capacitor. Since R_{c} is quite small, $R_{\text{c-eq}}$ can be set to cover the suitable range described in Eq. (9) to keep the system stability and a reasonable response speed.

3.2. Self-adaptive on-time generator

Figure 5 shows a proposed charge-pump-based SAOTG to control the on-time and eliminate the frequency disturbance, which consists of a phase frequency detector (PFD), a charge pump low pass filter (CPLPF) and a voltage controlled delay (VCD).

As shown in Fig. 5, the DUTY signal and the CLK constitute a negative feedback control system through the on-time generator and logic control unit to keep the frequency consistent with the CLK and not influenced by other factors. PFD responses according to the rise edges of CLK and DUTY to control CPLPF via switching S1 or S2. So the output of CPLPF V_{TH} is changed correspondingly. Then DUTY is adjusted toward CLK through the charging of C_2 to V_{TH} in VCD. The series R_{p} and C_{p} in CPLPF introduce a zero to compensate poles for loop stability, and C_3 parallels with it to reduce the voltage hopping on V_{TH} caused by the mismatch of current sources I_1 and I_2. Its bandwidth should be much lower than the switching frequency. With the consideration of the power stage, the loop transfer function is as follows:

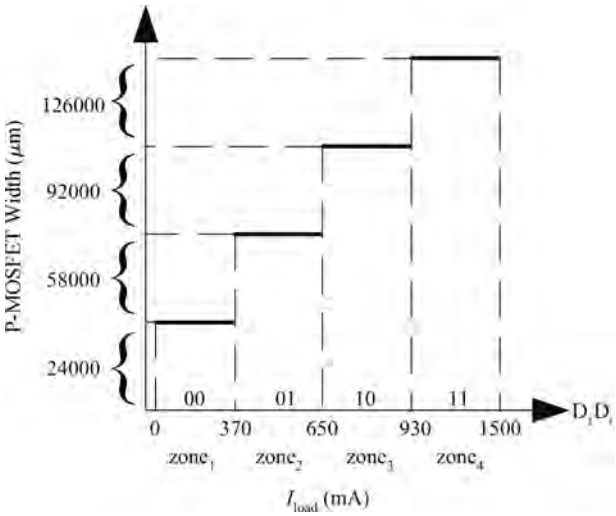


Fig. 6. Optimum size of PMOS verse load currents.

$$G(s) = \frac{C_2 R I_1}{V_{\text{out}} T_{\text{s}}^2} \frac{1 + sC_{\text{p}}R_{\text{p}}}{s^2[sR_{\text{p}}C_{\text{p}}C_3 + (C_{\text{p}} + C_3)]}. \tag{19}$$

The on-time of SAOTG is:

$$T_{\text{on}} \approx \frac{V_{\text{TH}} R C_2}{V_{\text{DD}}}. \tag{20}$$

The proposed charge pump based SAOTG has the advantage of a wide adjusting range, which is only relative to the range of the VCD. In addition, the rise edge of DUTY will be synchronized with CLK, which is favorable when using a more complicated PMU to unify timing.

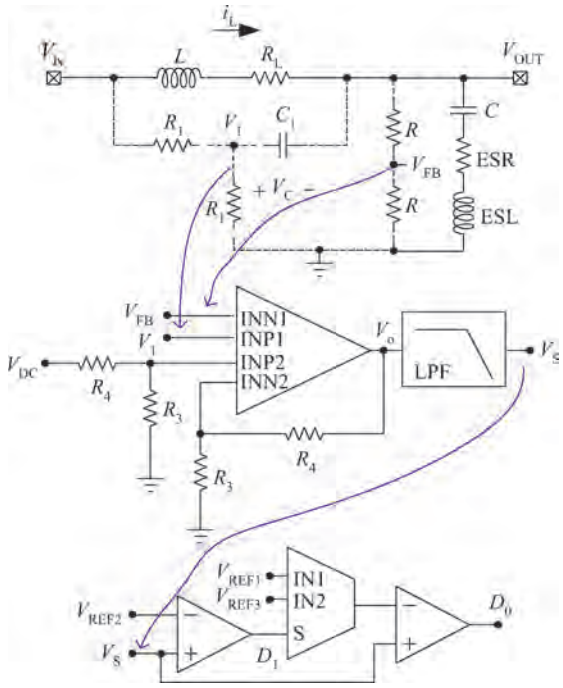


Fig. 7. Schematic of a self-adaptive power transistor sizing circuit.

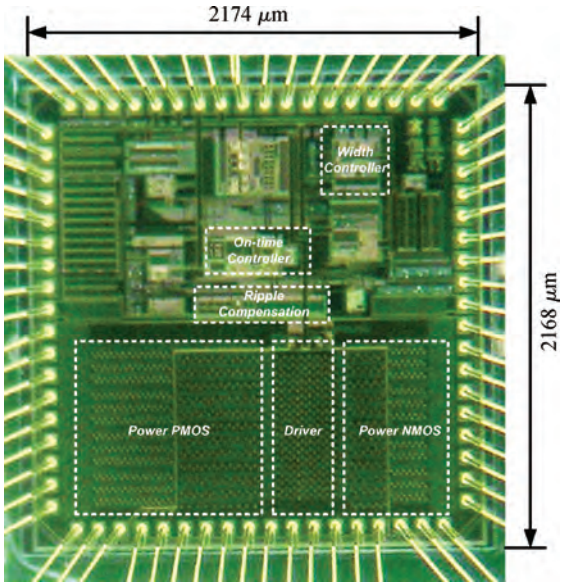


Fig. 8. Chip micrograph.

3.3. Self-adaptive power transistor sizing circuit

From the efficiency analysis, the power loss on MOSFET reaches a minimum when its conduction loss is equal to its switching loss. We can calculate the optimum transistor widths for NMOS and PMOS as Eqs. (21) and (22), which are directly proportional to the load current owing to the inductor current ripple being smaller than the load current.

$$W_{\text{pmos,opt}} \approx \sqrt{\frac{R_{\text{o,pmos}} D}{C_{\text{go,pmos}} V_{\text{g}}^2 f_{\text{s}}}} I, \tag{21}$$

$$W_{\text{nmos,opt}} \approx \sqrt{\frac{R_{\text{o,nmos}} (1-D)}{C_{\text{go,nmos}} V_{\text{g}}^2 f_{\text{s}}}} I. \tag{22}$$

Figure 6 shows the optimum power MOSFET sizes over the whole load range, which correspond to the four chosen load points, 200, 500, 800 and 1200 mA, respectively. The power transistor sizes can be adapted automatically according to the load currents. Scaling down the power MOSFETs width can save some power dissipation in switching loss when the load condition is light, and scaling up the power transistors can reduce the power dissipation in conduction loss when the load condition is heavy.

The load current can be detected by the resistance R_1 and capacitor C_1 paralleled with inductor L, in Eq. (23), which can share with the RCS, as shown in Fig. 7.

$$V_1 - V_{\text{FB}} \approx \frac{1}{2} i_{\text{L}} \frac{R_{\text{L}} + sL}{1 + sR_1 C_1} \approx \frac{1}{2} i_{\text{L}} R_{\text{L}}. \tag{23}$$

The voltage on the right terminal of the inductor can be seen as a DC value, so we choose reasonable values of R_1 and C_1 to make sure the signal $(V_1 - V_{\text{FB}})$ is approximately directly proportional to the current load. The sensing accuracy can be guaranteed because the DCR tolerance can be controlled at 5% with the current process[7].

$$V_{\text{o}} = (V_1 - V_{\text{FB}}) \frac{R_3 + R_4}{R_3} + V_{\text{DC}} = \frac{R_{\text{L}}}{2} \frac{R_3 + R_4}{R_3} i_{\text{L}} + V_{\text{DC}}. \tag{24}$$

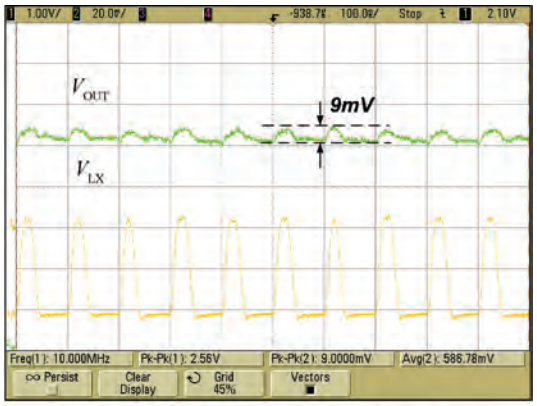
An amplifier with four inputs is used to get the AC voltage signal on C and amplify it by $(R_3 + R_4)/R_3$, in Eq. (24). Then a low pass filter is used to get the DC value V_{S} to correspond to each load condition, which is compared with reference voltages ($V_{\text{REF1}} > V_{\text{REF2}} > V_{\text{REF3}}$) via two comparators and one 2-1 MUX to judge the load zone. $V_{\text{REF1}} - V_{\text{REF3}}$ correspond to the load conditions of 370, 650 and 930 mA, respectively. Considering the input range, the voltage is divided in half before sending it to the amplifier. So the power transistor size is self-adaptive when the load condition changes, but it is locked at zone$_2$ during the process of soft-start.

4. Measurement results

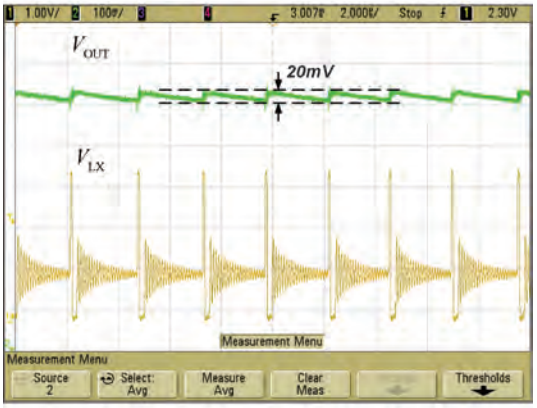
The buck DC–DC converter was manufactured in a chartered 2P4M 0.35 μm CMOS process and occupies an active chip area of 4.7 mm^2. The die micrograph is shown in Fig. 8.

The converter can work normally at different load conditions in the range 0–1500 mA. Figure 9(a) is the steady-state situation when the load current is 500 mA ($V_{\text{in}} = 2.3$ V and $V_{\text{out}} = 1$ V). We can see the ripple is less than 10 mV and the switching frequency is locked at 10 MHz precisely. The situation is similar to Fig. 9(b) when the load is as light as 50 mA ($V_{\text{in}} = 2.6$ V and $V_{\text{out}} = 1.8$ V), where the converter works at PFM mode with the help of DCM control, the ripple is about 20 mV.

The transient response when load current is switching between 150 and 350 mA ($V_{\text{in}} = 2.3$ V and $V_{\text{out}} = 1$ V) is shown in Fig. 10. From the measurement result we know the overshot and undershot are 8 mV @ 200 mA step, and the load regulation is as low as about 2 mV, which proves the outstanding transient response of the control mode.



(a) $V_{in} = 2.3$ V, $V_{out} = 1$ V, $I_{load} = 200$ mA



(b) $V_{in} = 2.6$ V, $V_{out} = 1.8$ V, $I_{load} = 50$ mA

Fig. 9. Measured waveform of the steady-state.

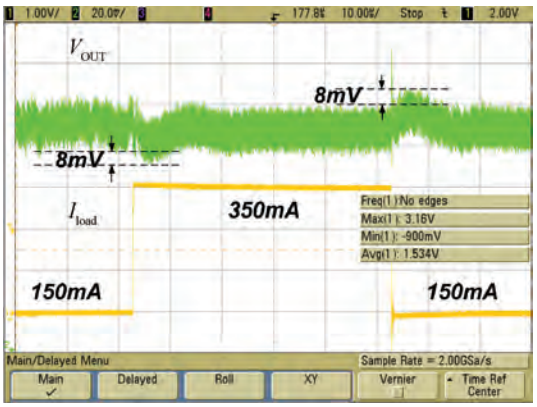


Fig. 10. Measured load transient of 200 mA step.

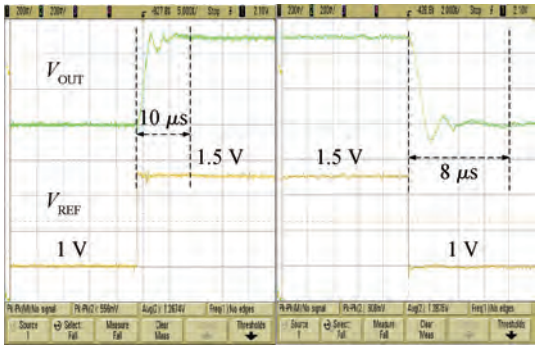


Fig. 11. Measured reference tracking in DVS of 0.5 V step.

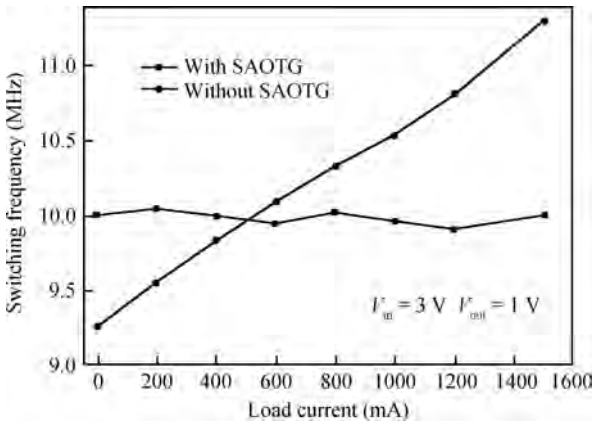


Fig. 12. Simulated frequency with and without SAOTG.

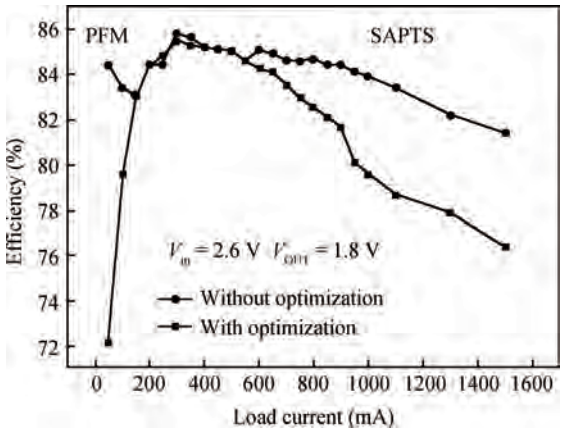


Fig. 13. Measured efficiency with and without optimization.

The DVS is measured as shown in Fig. 11. The rise response time is less than 10 μs and the fall response time is less than 8 μs @ 500 mV step between 1 and 1.5 V, which shows that the output voltage has a very fast and stable scaling following the reference voltage.

The switching frequency variation at different load currents simulated is shown in Fig. 12. With SAOTG, the variation is about 1% around the target frequency of 10 MHz in a load range of 1500 mA, compared with a 10% variation without it.

The measurement result shows that the peak efficiency 88.43% appears at 200 mA when $V_{in} = 2.3$ V and $V_{out} = 1.8$ V. Thanks to the SAPTS technique, the efficiency is optimized as shown in Fig. 13. Optimization is more obvious in the heavy load condition, and the most improved ratio reaches more than 5% @ 1500 mA. With the contribution of PFM in a light load condition, the overall efficiency can remain over 81% for the load range between 20 and 1500 mA.

Table 2 summarizes the performances of this work and compares them with state-of-the-art designs.

5. Conclusion

Conforming with high-frequency large current trends, a 1500 mA, 10 MHz self-adaptive on-time controlled buck

Table 2. Performance summary and comparison with state-of-the-art designs.

Specification	This work	VLSI'11 Ref. [3]	ISSCC'10 Ref. [1]	Micrel Inc. Ref. [8]
Year	2011	2011	2010	2008
Topology	Buck	Buck	Buck-Boost	Buck
Process	0.35 μm CMOS	0.5 μm Bi-CMOS	0.13 μm CMOS	–
Control complexity	Easy	Medium	Complicate	Easy
Input voltage (V)	2.3–4.8	2.7–5.5	1.5	2.7–5.5
Output voltage (V)	0.6–1.8	1.2	1.2, 1.8	1.2–2.5
Current capability (mA)	1500	600	400	400
Switching frequency (MHz)	10	20	10	8
External inductor (μH)	0.47	0.27	–	0.47
External capacitor (μF)	4.7	1.6	–	4.7
Output ripple (mV)	10	12	–	10
Load transient (mV@ mA)	8 @ 200	50 @ 600	–	20 @ 300
Load regulation (mV/A)	10	1.6	–	67
Up tracking speed (μs/V)	16	–	93.3	–
Fall tracking speed (μs/V)	20	–	26.7	–
Efficiency @ V_{in}/V_{out} (%)	88.4 @ 2.3–1.8 V	84 @ 2.7–1.2 V	92.1 @ 1.5–1.2 V	87 @ 2.7–1.8 V

DC–DC converter is designed and implemented on a chartered 2P4M 0.35 μm CMOS process. The simple fixed-frequency self-adaptive on-time control mode with ripple compensation is proposed to ensure that the converter works well at a frequency of as high as 10 MHz. A small external inductor of 0.47 μH and capacitor of 4.7 μF are used to lower the cost of the converter and keep the small output ripple to 10 mV. Thanks to the control mode, the converter exhibits a best-in-class load transient response of 8 mV @ 200 mA step and an excellent reference tracking DVS performance of a rising of 16 μs/V and a falling of 20 μs/V. In addition, with the self-adaptive power transistor sizing scheme and PFM control, the efficiency remains over 81% for the load range of 20 to 1500 mA. The peak efficiency reaches 88.43%. This converter is suitable for various portable applications.

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