A 18-mW, 20-MHz bandwidth, 12-bit continuous-time ΣΔ modulator using a power-efficient multi-stage amplifier*

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Abstract: A fourth-order continuous-time sigma delta modulator with 20-MHz bandwidth, implemented in 130-nm CMOS technology is presented. The modulator is comprised of an active-RC operational-amplifier based loop filter, a 4-bit internal quantizer and three current steering feedback DACs. A three-stage amplifier with low power is designed to satisfy the requirement of high dc gain and high gain-bandwidth product of the loop filter. Non-return-to-zero DAC pulse shaping is utilized to reduce clock jitter sensitivity. A special layout technique guarantees that the main feedback DAC reaches 12-bit match accuracy, avoiding the use of a dynamic element matching algorithm to induce excess loop delay. The experimental results demonstrate a 64.6-dB peak signal-to-noise ratio, and 66-dB dynamic range over a 20-MHz signal bandwidth when clocked at 480 MHz with 18-mW power consumption from a 1.2-V supply.

Key words: continuous-time; sigma delta modulation; low power design; multistage operational amplifier
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1. Introduction

Nowadays the rapid development of wireless communication evokes new standards of larger bandwidth, such as a long-term evolution (LTE) protocol of up to 20 MHz for 4G applications. In recent years, several published works[1−4] have focus on larger bandwidth sigma delta modulators due to their attractions of low power dissipation. Most of them employ a continuous-time (CT) structure, targeting at 10–12 bit resolution and covering 10–25 MHz signal bandwidth. The CT ΣΔ structure is widely used because it is much more suitable for lower power consumption compared to discrete-time (DT) structures, since the required GBW of the amplifiers for a fixed sampling frequency f_s is approximately a factor of three times lower compared to its DT counterparts[5]. This results in power saving and allows CT ΣΔ ADC to operate at higher frequencies. Moreover, the CT structure offers inherent implicit anti-aliasing, hence eliminating the use of extra power-hungry anti-aliasing filters, which also help to reduce the system complexity. However, many unique design challenges appear when designing such ADCs. They are more sensitive to clock jitter, excessive-loop-delay (ELD) and loop coefficients variation than those in a DT design approach. Special design considerations have been taken in recent published works, such as full clock period the switched-capacitor-resistor (FSCR) feedback DAC used in Ref. [3] to reduce the clock jitter sensitivity and the RC trimming method implemented in Ref. [2] to tune the loop coefficients.

Although the required GBW of the amplifiers is reduced in the CT structure, the operational amplifiers (opamp) still contribute the main power consumption to the modulator for broadband applications. So it is crucial to explore power-optimized amplifiers. For example, the sigma delta ADC reported in Ref. [1] optimized a two-stage miller compensated opamp to save power, and Ref. [2] achieves 76 dB signal-to-noise-and-distortion ratio (SNDR) over a 20 MHz bandwidth with the help of a special four-stage operational amplifier.

This paper presents a 4th-order CT low-pass sigma delta modulator with 12 bit resolution and 20 MHz bandwidth aiming at LTE mobile system application. It is implemented in 130 nm CMOS technology with 1.2 V supply voltage. Power optimization is considered at both system and circuit level. A multi-stage amplifier is designed to maintain high DC gain and large bandwidth with small power consumption.

2. System architecture

2.1. Modulator topology

The proposed CT modulator architecture is shown in Fig. 1(b), operating at 480 MHz with 20 MHz bandwidth. It consists of a fourth-order active-RC loop filter, a 4-bit quantizer and three NRZ feedback DACs. For the given signal bandwidth, low over-sampling-rate (OSR) is restrained by the technology. The modulator combines with the merits of feed forward and feedback structures, acquiring both low-power realization and flat response within the signal band. Meanwhile, multi-bit quantizer is used to improve the in-band SNR.

The modulator employs four active-RC integrators to constitute the loop filter. This implementation has advantages of high linearity and high output signal swing compared to G_m–C structure and provides a good virtual ground for the modulator feedback DACs. These advantages will be more significant under low supply voltages. The 4-bit quantizer, including the feedback DACs, is connected to the output of the loop filter. The quantizer delay is set to half of the sampling period,

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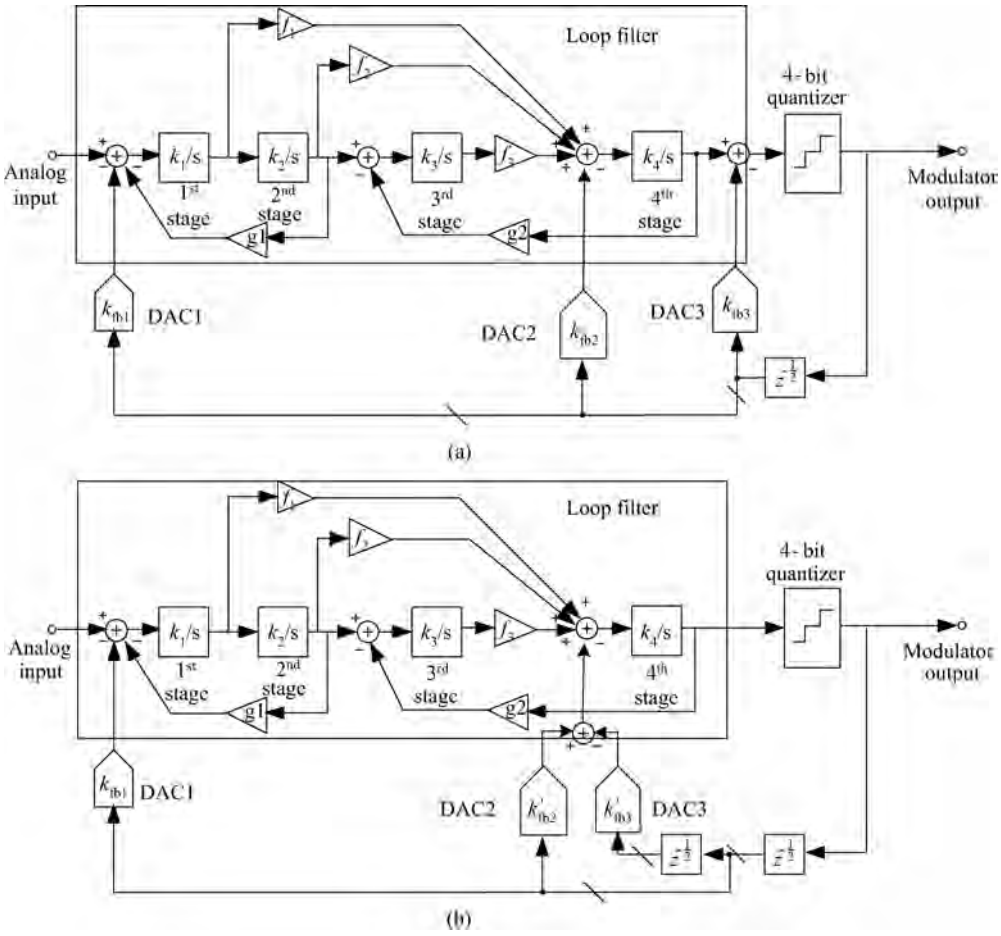

Fig. 1. (a) A 4th-order single-loop, multi-bit CT ΣΔ modulator with summing stage. (b) The proposed ΣΔ modulator without summing stage.

compensated exactly by an additional feedback path k'_{fb3} at the system level. Therefore the placement of noise-transfer function (NTF) poles is not limited by the effect of quantizer delay on loop stability.

2.2. System level consideration for lower power

In the feed-forward structure, a signal summing block before the quantizer is needed, as shown in Fig. 1(a). This summing stage is power-hungry because it has to handle high frequency signals. With low power consideration, the signal summing node is repositioned and located right before the fourth stage, removing the signal summing circuit with the help of DAC2 and DAC3[2], as illustrated in Fig. 1(b). Also DAC2 and DAC3 perform ELD compensation to ensure the stability of the continuous-time modulator.The coefficients k'_{fb2} and k'_{fb3} in Fig. 1(b) can be expressed as

$$k'_{\mathrm{fb3}} = k_{\mathrm{fb3}}/k_4, \tag{1}$$

$$k'_{\mathrm{fb2}} = k_{\mathrm{fb2}} + k'_{\mathrm{fb3}}, \tag{2}$$

where k_4 is the gain of the fourth integrator, k_{fb2} and k_{fb3} are the coefficients of DAC2 and DAC3 in Fig. 1(a).

System level simulation shows that larger GBW of amplifiers will have better stability performance, but it will consume more power. So a tradeoff must be made between stability and power consumption. Figure 2 shows the relationship between the GBW of the operational amplifiers and the signal-to-quantization noise ratio (SQNR) of the modulator, where F_{s} is the sampling frequency. To get SQNR over 74 dB, the GBW of the opamp in first stage is chosen to be 1.5 times of sampling rate F_{s}, because it deals with the feedback signal from DAC1. The GBW of the fourth one is 2.5 times of sampling rate F_{s} for the high frequency signals are added at this stage.

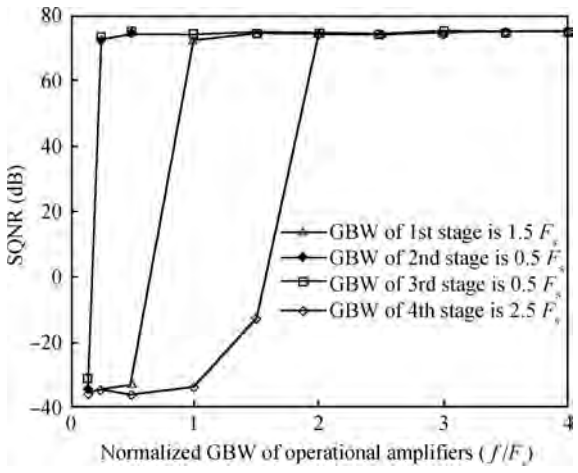

Fig. 2. SQNR performance under different GBW of operational amplifiers.

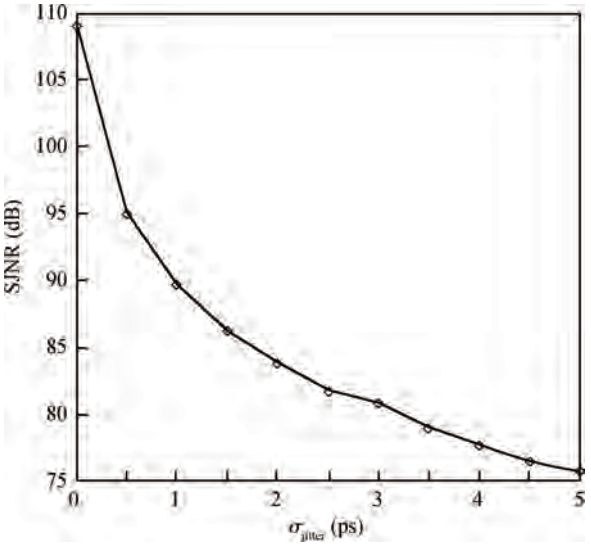

Fig. 3. Jitter simulation in MATLAB under –3.1 dB input amplitude.

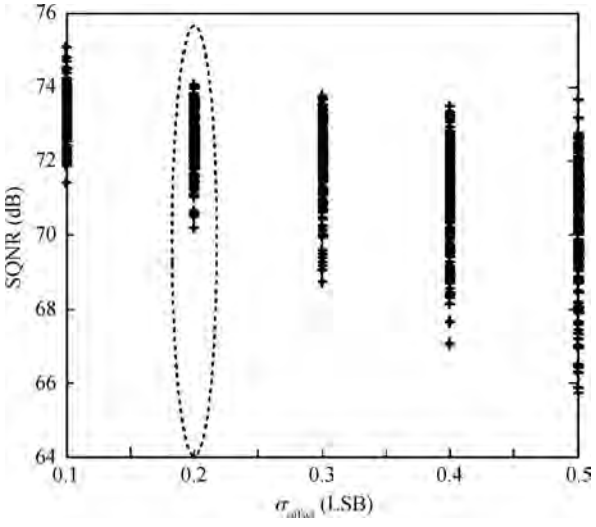

Fig. 4. Quantizer offset simulation in MATLAB.

2.3. Clock jitter consideration

As is pointed out in Refs. [3, 6], clock jitter affects both the sampling of the quantizer and the feedback DAC pulse. For broadband sigma delta ADC, the jitter effect on feedback DAC cannot be noise-shaped and thus greatly degrades the SNR. The effect of the clock jitter to SNR can be expressed as

$$\mathrm{SNR}_{\mathrm{jitter}} = 10\lg \frac{\mathrm{OSR}\cdot V_{\mathrm{in}}^2/2}{\sigma_{\Delta y,\mathrm{NRZ}}\left(\dfrac{\sigma_\beta}{T_{\mathrm{s}}}\right)^2}, \tag{3}$$

where OSR is the oversampling ratio, V_{in} is the input signal amplitude, $\sigma_{\Delta y,\mathrm{NRZ}}$ is the standard deviation of the adjacent modulator output difference, σ_β is the standard deviation of the clock jitter and T_{s} is the sampling period.

Several techniques are introduced to reduce this effect[6]. Multi-bit NRZ DAC is used here to reduce the jitter sensitivity. System-level simulation demonstrates that for a signal-to-jitter noise ratio (SJNR) larger than 74 dB, the RMS value of clock jitter needs to be less than 5 ps, as shown in Fig. 3.

2.4. Quantizer offset consideration

The 4-bit quantizer in Fig. 1 is implemented in flash structure and the minimized channel length of the comparators is used for high conversion speed, but it brings in a large offset voltage, especially when the supply voltage gets lower. Although the non-idealities of the quantizer can be largely shaped by using a loop filter, the large offset may cause logic error and degrade SNDR. To achieve more than 11.5 bit performance, the random offset in comparator requires less than 0.2 least significant bit (LSB) according to the results of 400 trials in MATLAB for each level offset, as shown in Fig. 4.

2.5. DAC linearity consideration

Resolution in feedback current steering DAC is another obstacle for sigma delta modulator performance, the resolution of current steering DAC is limited mainly by I-mismatching. There are many attempts to suppress the mismatch[3, 7], such as calibration and DEM. However, both methods have their own problems. Calibration may introduce new tone and increase design complexity while DEM will increase noise floor and bring in more loop delay. In this design, the linearity of 4-bit NRZ DAC is warranted by a special DAC layout technique[8].

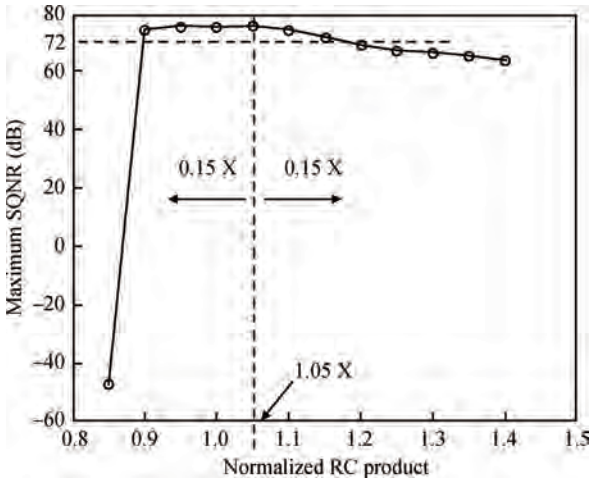

Fig. 5. Effect of RC product variation on the system performance under –3.1 dB input amplitude.

2.6. Loop coefficient variation

In continuous-time modulator, the loop coefficients are determined by the absolute value of the product of resistance and capacitance, so they are sensitive to process and temperature variation[7, 9]. In modern CMOS processes, the absolute value of R or C can vary $\pm 25\%$ which may decrease the achievable SNDR or even make the system unstable. Careful system-level simulation is performed to estimate the impact on the SQNR of the modulator. Figure 5 demonstrates that the modulator can endure $\pm 15\%$ time constant variation under –3.1 dB input amplitude. In this design, 3-bit digital codes are externally fed into the chip to tune the time constant to make the system stable.

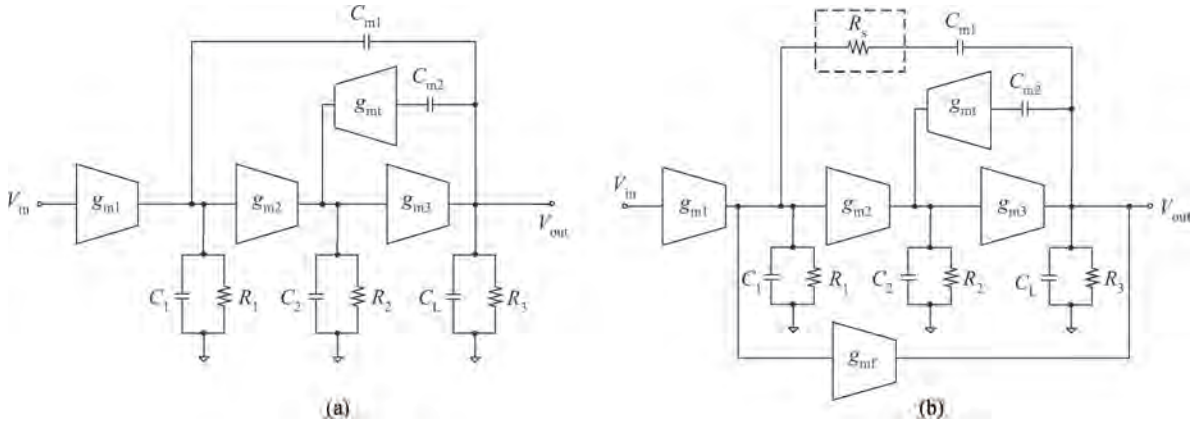

Fig. 6. Block diagram of (a) TCFC structure and (b) the proposed structure

2.7. Noise consideration

By appropriately selecting NTF, topology, etc, the quantization noise can be controlled under very low level. Thus the whole noise level is mainly determined by the device noise especially in high resolution and broadband design. Therefore, the noise budget is needed to fix before the circuits design. In this modulator, the frond-end noise mainly comes from the two input resistors, the opamp in the first integrator and DAC1 in Fig. 1. To achieve a SNR larger than 74 dB, SNR contributed by each part should be larger than 80 dB. The tradeoff between power and noise must be considered. The input resistor $R_{\rm in}$ is chosen to be 3.4 kΩ which makes SNR = 85 dB for a full scale input signal[7]. The noise coming from DAC1 can be expressed as

$$n_{\rm DAC} = \frac{8kT\gamma I_{\rm DAC}R_{\rm in}^2}{V_{\rm GS}-V_{\rm TH}}\Delta f, \tag{4}$$

where $n_{\rm DAC}$ is the noise coming from DAC1, $I_{\rm DAC}$ is the total current of DAC1, $V_{\rm GS}-V_{\rm TH}$ is the overdrive voltage of the current source, k is the Boltzmann constant, T is the absolute temperature, γ is the MOS transistor noise factor and Δf is the signal bandwidth. The adjustable parameters are $I_{\rm DAC}$ and $V_{\rm GS}-V_{\rm TH}$. The noise from the opamp contains both thermal and flicker noise which should also be kept low.

3. Circuit design

3.1. Multi-stage amplifier

As has been mentioned in Section 2, the GBW of the opamp in the fourth integrator requires 1.2 GHz with 2 pF load. This requires at least 9 mA power consumption for two-stage Miller CMOS opamp[10]. In the mean time, high in-band DC gain can lower the opamp bandwidth requirement for ΣΔ modulator because it can reduce excess phase shift of the integrator stages[2]. With supply voltage becoming lower, the high in-band gain cannot be obtained by simply cascoding transistors. Multistage operational amplifiers are then adopted in this design since they meet the requirements of both large bandwidth and high in-band gain. Some multistage amplifiers are discussed in Ref. [11], however, most of them are suitable for large capacitive loads. The opamp used in Fig. 1 has a lighter capacitive load and a larger bandwidth, also it has to drive the resistive load of the following stages.

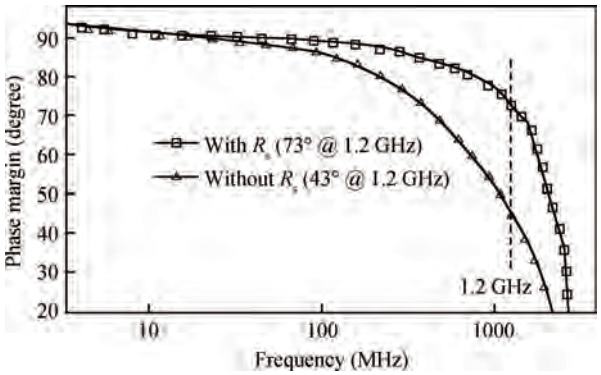

Fig. 7. Improvement on PM with $R_{\rm s}$.

The opamp with four stages and $G_{\rm m}$–C compensation used in Ref. [2] hasa larger bandwidth and a high DC gain, but it suffers conditional stability. In Ref. [11], a multi-stage amplifier structure called transconductance with capacitances feedback compensation (TCFC) is introduced, as shown in Fig. 6(a). A transconductor with capacitive feedback method is adopted to improve the high frequency phase margin, and high frequency shorting effect on the output stage $g_{\rm m3}$ is avoided, also stability can be well ensured with a small transconductance $g_{\rm mt}$ in the output stage. However, in high frequency up to more than 500 MHz, the first miller capacitor $C_{\rm m1}$ connecting the first stage and the output also suffers the high frequency shorting effect, and a right plane zero makes the phase margin worse, so additional resistor $R_{\rm s}$ is proposed here to push this zero away, as shown in Fig. 6(b). The small signal transfer function of the open-loop gain of this amplifier can be given by

$$A_{\rm v}(s) = \frac{A_{\rm dc}\left(1+\dfrac{s}{\omega_4}+\dfrac{s^2}{\omega_4\omega_5}+\dfrac{s^3}{\omega_4\omega_5\omega_6}\right)}{\left(1+\dfrac{s}{\omega_{\rm d}}\right)\left(1+\dfrac{s}{\omega_1}+\dfrac{s^2}{\omega_1\omega_2}+\dfrac{s^3}{\omega_1\omega_2\omega_3}\right)}, \tag{5}$$

where $A_{\rm dc}$ is the low-frequency gain. $\omega_{\rm d}$ is the dominant pole, ω_{1-3} and ω_{4-6} represent frequency factor in denominator and numerator of Eq. (5), respectively. The transfer function of opamp in Ref. [11] is similar as Eq. (5), but there is a right

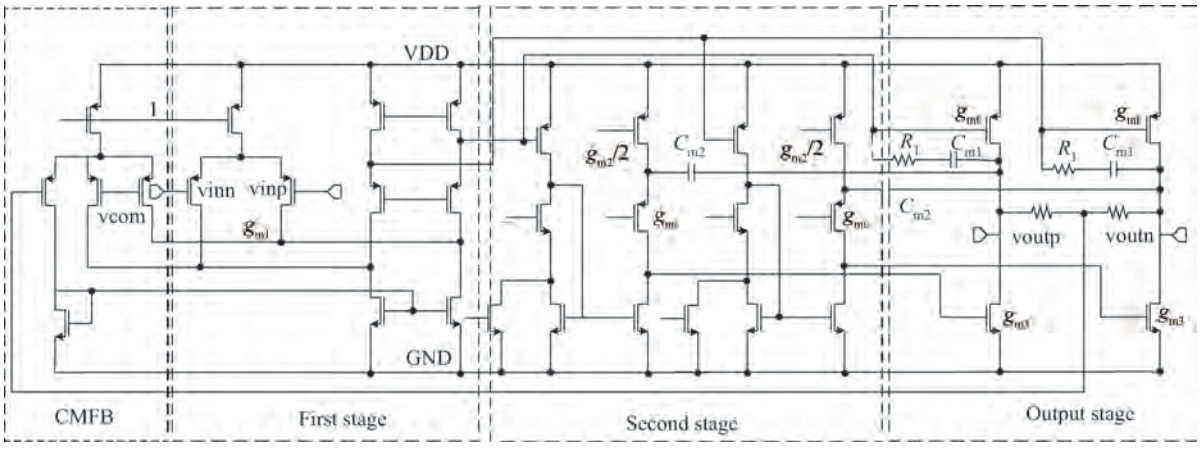

Fig. 8. Multi-stage amplifier used in integrator.

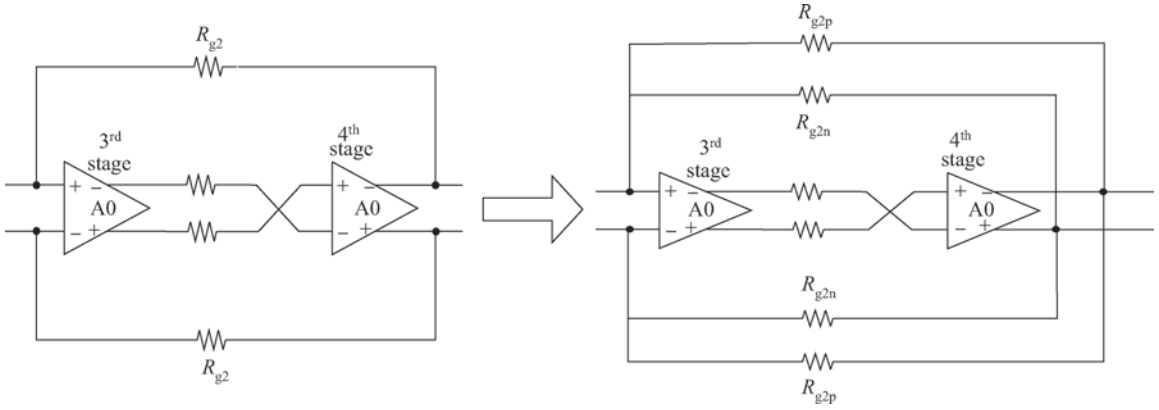

Fig. 9. Split large feedback resistor.

plane zero ω_5 which can only be neglected when the demanded bandwidth is narrow. This zero ω_5 can be expressed as

$$\omega_5 = \frac{-C_{m2}g_{mt}g_{m3}}{C_2C_{m1}g_{m2}}. \quad (6)$$

This high frequency zero will degrade the phase margin in a large bandwidth design. After inserting resistor R_s, it can be expressed as

$$\omega_5' = \frac{-C_{m2}g_{m2}g_{m3}}{C_2C_{m1}\left(g_{mt} - g_{m2}g_{m3}R_s\right)}. \quad (7)$$

It can be seen from Eq. (7) that the effect of right plane zero will be cancelled by appropriately choosing R_s, which can significantly improve phase margin (PM) by 30°, as shown in Fig. 7. This resistance of R_s is about 3 kΩ, and it can endure 20% variation, also parallel connection of several larger resistors in layout design will further guarantee the performance of the multi-stage amplifier.

To improve the large-signal performance such as slew rate, a feed-forward stage g_{mf} is included to constitute a push-pull output stage, as illustrated in Fig. 6(b). The schematic of the multi-stage amplifier is shown in Fig. 8. In sigma–delta modulator, the bandwidth of the common mode feedback stage (CMFB) is not as important as differential GBW. Through simulation, the CMFB bandwidth of each amplifier is only required to be half of the differential counter-part. As shown in Fig. 8, the common mode feedback stage is on the left part, and most of the differential parts from OTA can be reused, so the CMFB bandwidth requirement can be satisfied by small additional power. The multi-stage amplifier in the fourth integrator achieves 80 dB DC gain and 1.2 GHz GBW with 5.5 mA power consumption.

The first integrator contains a three-stage operational amplifier which dissipates 0.6 mA current in the input differential pair to satisfy the thermal noise requirement; also the channel length of the input pair should be large enough to minimize the offset. Minimal channel length is used in the following three integrator stages because of relaxed requirements on noise and offset, making lower power consumption and large bandwidth possible.

3.2. Multibit DAC

Current steering DAC is used for its potential for high speed operation and easy to interface with continuous-time loop filter. To reduce glitch error at the output, which would degrade the performance of the whole modulator, the 4 bit DAC is thermometer coded. The swing of the digital controlling switch signals is limited to 0.4 V with low crossing point instead of full logic swing[7]. The required precision of the DAC is achieved by using a proper layout technique[8] instead of a DEM algorithm to reduce the loop delay.

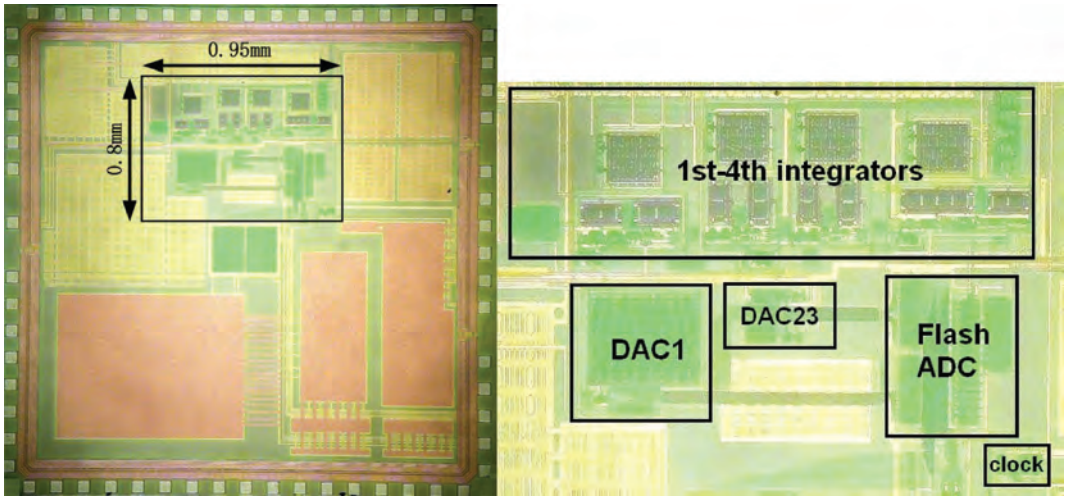

Fig. 10. Chip microphotograph.

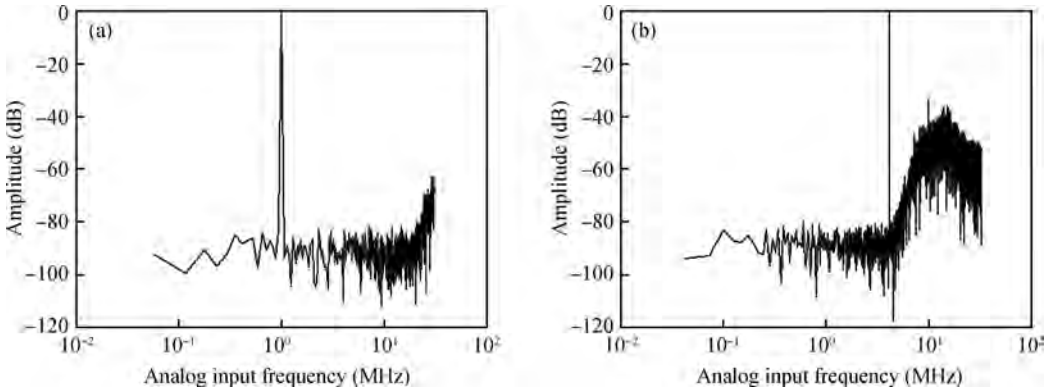

Fig. 11. Spectra of the modulator for a −4.2 dBFS, 1 MHz and 19 MHz input tone. (a) 1 MHz. (b) 19 MHz.

3.3. Capacitor tuning and loop filter coefficient

To stabilize the modulator and maintain the performance over the different output data rates, a capacitor tuning logic is used to cover the RC variation which can vary the capacitor from 40% to 180%.

The loop filter coefficients in Fig. 1 are realized with resistors. According to the system implementation, the feedback resistors from the fourth stage to the second stage are large, about mega ohm, which leads to large parasitic capacitance and even changes the transfer function. A technique in Ref. [12] is carried out in this design, which splits R_{g2} into two small ones R_{g2p} and R_{g2n}, reducing feedback resistance by 10×, so to the parasitic capacitance, as indicated in Fig. 9.

4. Experimental results and comparison

The chip was implemented in SMIC 0.13 μm 1P8M (one-poly-eight-metal) CMOS process. The active area is 0.76 mm^2 as shown in Fig. 10. The total power consumption is 18 mW with 1.2 V power supply.

An Agilent 8257D signal source and an Agilent 8267D clock source were used to characterize the modulator. The output data of the chip was captured by a logic analyzer Agilent 16822A and processed by MATLAB on the PC. The experimental output spectrums with 1 MHz and 19 MHz, –4.2 dBFS (0.74VP-P) input signal under 480 MHz clock frequency are plotted in Figs. 11(a) and 11(b), respectively. The achieved peak SNR over the 20 MHz bandwidth is 64.6 dB. Figure 12 shows the measured SNR and SNDR versus the input ampli-

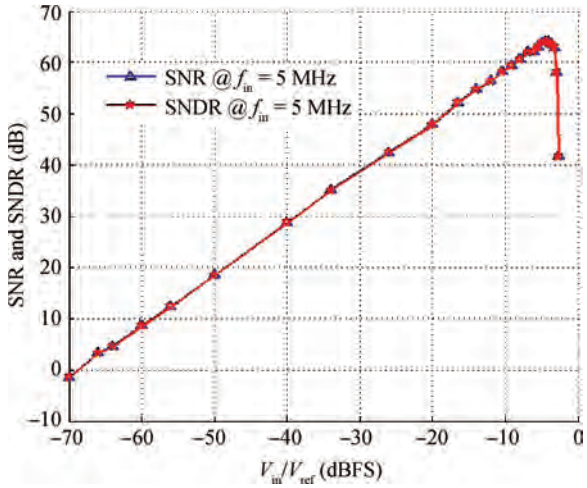

Fig. 12. Measured SNR and SNDR versus input amplitude from a 5 MHz single tone test.

Table 1. Summary of the measured performance.

Parameter	Value
Process	130 nm CMOS
Supply voltage	1.2 V
Signal bandwidth	20 MHz
Sampling rate	480 MHz
DR	66 dB
Peak SNR	64.6 dB
Peak SNDR	64.1 dB
Power	18 mW
Chip area	0.76 mm^2
FOM	333 fJ/conv

Table 2. Comparison with other works.

Parameter	Ref. [1]	Ref. [2]	Ref. [3]	Ref. [4]	This work
CMOS technology (μm)	0.18	0.13	0.13	0.18	0.13
Power supply (V)	1.8	1.2	1.2	1.8	1.2
BW (MHz)	15	20	20	10	20
SNR (dB)	67.2	76	67.9	82	64.6
DR (dB)	70	N.M	68	87	66
Power (mW)	20.7	20	58	100	18
FOM (pJ/conv)	0.37	0.12	0.715	0.486	0.33

tude with 5 MHz input signal. The measured dynamic range (DR) is 66 dB.

The performance of the proposed $\Sigma\Delta$ modulator is shown in Table 1. The figure-of-merit (FOM)[13] is expressed as

$$\mathrm{FOM} = \frac{P}{2 \cdot \mathrm{BW} \cdot 2^{(\mathrm{SNR}-1.76)/6.02}}, \tag{8}$$

where P is the power consumption, BW is the signal bandwidth and SNR is the signal power over noise power ratio.

Table 2 compares the performance of the modulator proposed in this work with other state-of-art designs. This work achieves a relatively low energy per level resolved with the help of power efficient multistage amplifier.

5. Conclusion

A fourth-order, single-stage, single-loop continuous-time sigma–delta modulator with active-RC loop filter has been presented. The loop architecture is insensitive to the excess loop delay caused by the quantizer and feedback DAC. A multistage operational amplifier is introduced to achieve high DC gain, wide bandwidth and low power. Over a bandwidth of 20 MHz, the modulator achieves 64.6 dB peak SNR and 66 dB dynamic range while dissipating 18 mW from a 1.2 V supply. The active area is 0.76 mm^2 implemented in a 0.13-μm 1P8M CMOS process.

Acknowledgment

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