S-band low noise amplifier using 1 μm InGaAs/InAlAs/InP pHEMT

Z. Hamaizia[1, †], N. Sengouga[1], M. C. E. Yagoub[2], and M. Missous[3]

[1]Laboratory of Materials Semiconductors and Metallic, University of Med Khider, Biskra, 07000 Algeria
[2]RF and Microwave Research Group, School of Electrical Engineering and Computer Science, University of Ottawa, Ottawa ON, KIN 6N5 Canada
[3]Microelectronic & Nanostructure Group, School of Electric and Electronic Engineering, University of Manchester, UK

Abstract: This paper discusses the design of a wideband low noise amplifier (LNA) in which specific architecture decisions were made in consideration of system-on-chip implementation for radio-astronomy applications. The LNA design is based on a novel ultra-low noise InGaAs/InAlAs/InP pHEMT. Linear and non-linear modelling of this pHEMT has been used to design an LNA operating from 2 to 4 GHz. A common-drain in cascade with a common source inductive degeneration, broadband LNA topology is proposed for wideband applications. The proposed configuration achieved a maximum gain of 27 dB and a noise figure of 0.3 dB with a good input and output return loss ($S_{11} < -10$ dB, $S_{22} < -11$ dB). This LNA exhibits an input 1-dB compression point of –18 dBm, a third order input intercept point of 0 dBm and consumes 85 mW of power from a 1.8 V supply.

Key words: HEMT; InGaAs; InP; SKADS; telescope; LNA
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1. Introduction

CMOS technology has become a competitive technology for radio transceiver implementation of various wireless communication systems due to its ease of scaling, higher level of integrability, lower cost, etc. On the other side, CMOS wideband low-noise amplifiers (LNAs) are in high demand in the radio-astronomy community for their lower noise performances.

LNA designers usually utilize III–V semiconductors such as gallium arsenide (GaAs) and indium phosphide (InP) because of their higher performance in terms of gain and noise. However, to further improve the LNA performance, InP/InGaAs composite devices are also a promising way of enhancing the on-state breakdown voltage[1, 2]. This has been made possible through advancements in epitaxial growth technology, which allow the growth of strained InGaAs into GaAs and InP substrates[1−7].

On the other side, significant progress has been made recently in heterojunction transistor technology because of their small size, reproducibility and low cost at high frequencies. Therefore, millimeter-wave monolithic microwave integrated CMOS circuits based on InGaAs/GaAs pseudomorphic high electron mobility transistor (pHEMT) technology are gaining popularity in communication, radar, electronic warfare and radiometry system applications.

Additionally, InAlAs/InGaAs HEMTs are used in high transconductance devices because of their large conduction band discontinuity, high electron mobility and very good carrier confinement in the channel[8].

In fact, InP-based HEMTs have been shown to be the best performing three-terminal devices, with excellent performance in the microwave and millimeter-wave range. The combination of high gain and low noise has been demonstrated by many devices and circuits having operating frequencies as great as 100 GHz and higher[7, 9, 10−14].

InGaAs/InAlAs/InP HEMTs have demonstrated the highest gain, lowest noise and highest frequency capability for any three terminal transistor[1, 3, 8, 15] and are a natural fit towards next generation satellite communication systems, wireless LAN and ultra-high frequency remote sensing applications to name a few. A further advantage, especially for array-type applications is the ultralow dc power dissipation of these transistors.

Recently reported is a very promising material system for low-noise applications: a InGaAs/InAlAs system on InP. GaAs and InP HEMTs are attractive for several applications such as radio astronomy, because of their high transconductance and linearity under low DC bias operation, their small size, and low noise figure capability at L-, S-, and C-band frequencies[16, 17]. One of the most exciting applications of this technology is the Square Kilometer Array (SKA) radio telescope. SKA design studies (SKADS) is an international effort to investigate and develop technologies which will allow the building of an enormous radio astronomy telescope with a million square meters of collecting area[18, 19].

The LNA design involves many tradeoffs between the noise figure (NF), gain, linearity, impedance matching, and power dissipation[16]. Generally, the main goal of LNA design is to achieve simultaneous noise and input matching at any given amount of power dissipation. It must also provide low noise behavior not only at one frequency but over the whole bandwidth of interest[20−22].

In this paper, we focused on the design of an S-band (2–4 GHz) LNA for SKA receivers as part of European SKADS. To achieve the desired sensitivity, the LNA should exhibit an NF of less than 0.5 dB with a flat gain of at least 10 dB. With these specifications and in order to achieve such a

† Corresponding author. Email: hamaiziaz@gmail.com
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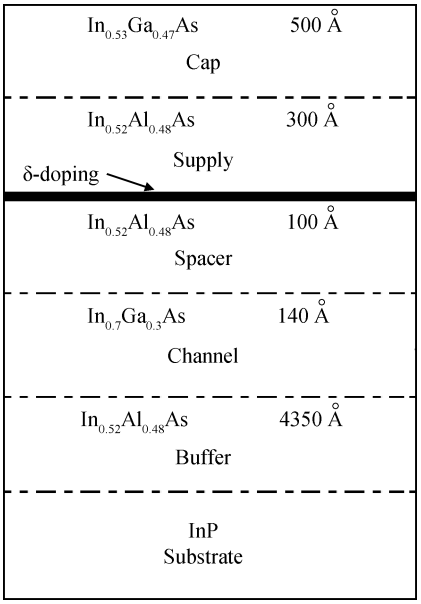

Fig. 1. Epitaxial structure of the InGaAs/InAlAs/InP pHEMT (4 × 200 μm) used in this work.

low noise figure and high linearity over the frequency band, the transistor noise resistance R_n must be substantially decreased to make the system insensitive to impedance matching. This can only be realized through the fabrication of a very large gate width InGaAs/InAlAs pHEMTs[17].

2. Description of pHEMT technology

The fabricated high breakdown of a 1 μm InGaAs-InAlAs-InP pHEMT used in this work is shown in Fig. 1. Such a transistor is suitable for radio astronomy applications. It uses an advanced MBE (molecular beam epitaxy) growth technique and is a four finger device with a 200 μm unit gate width and a 1 μm gate length. More details about this pHEMT can be found in Refs. [17, 23–25].

As mentioned, the InGaAs/InAlAs/InP system offers many advantages over GaAs structures. The high conduction band discontinuity of the structure allows a high two-dimensional electron gas concentration. The high mobility of electrons in InGaAs, coupled with the high density of electrons in the channel, leads to high conductivity in the active channel. Because of these superior material characteristics, InP based pHEMTs exhibit very high transconductance, a lower noise figure and higher gain than conventional HEMTs fabricated on GaAs material. All the noise sources that contribute to the device noise figure are lower in the GaInAs/AlInAs HEMTs than in GaAs HEMTs. The extremely high conductivity of the two-dimensional (2-D) electron gas lowers the source resistance and associated thermal noise. Due to lower intervalley electron transfer probability, the velocity of electrons in the channel is higher and leads to high f_T[26–29].

3. 2–4 GHz wide-band LNA design and analysis

A 2–4 GHz LNA was designed using the Agilent advanced design commercial simulator (ADS)[30]. In LNA design, several circuit design techniques have demonstrated their robustness, such as the capacitive peaking technique, the inductive peaking technique, the common-gate (CG) input configuration, and the common drain (CD) input configuration[31]. It has to be noted that the CG and CD input configurations relax the effect of a large input parasitic capacitance better than the conventional common-source (CS) input. The minimum noise figure of an InP pHEMT increases with frequency. When designing a broadband LNA, one would like to either minimize the noise figure over the whole bandwidth or to allow the noise figure to be higher at low frequencies, giving a wider band of operation. The proposed LNA is shown in Fig. 2. The input stage is a common-drain stage with a common-drain stage in the feedback loop for impedance matching. The output stage is a common-source amplifier inductive degeneration topology that consists of a transconductor T_1, drain and source inductors, L_{d3} and L_{s3}, respectively. The value of the drain inductor L_{d1} is adjusted to simultaneously optimize the input gain and noise matching.

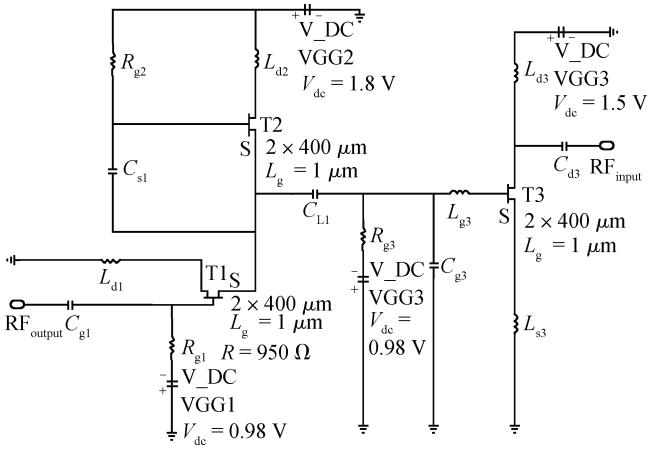

Fig. 2. LNA circuit simulation using a modelled 1 × 800 μm^2 transistor. The transistor is biased at about 20% I_{DSS} and all components are on-chip.

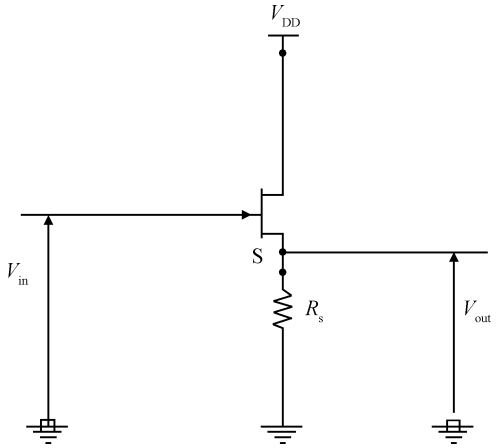

Fig. 3. The common drain configuration.

Figures 3 and 4 show the common-drain stage used in impedance matching and its simplified small signal equivalent circuit, respectively. Its voltage gain is close to unity for load resistances higher than $\frac{1}{g_m+g_d}$ and is given by:

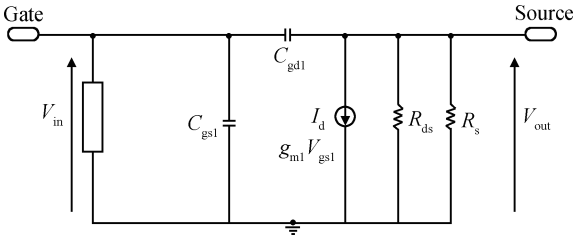

Fig. 4. A simplified small-signal equivalent circuit of the common drain amplifier.

$$G_v = \frac{g_{m1} + j\omega C_{gs1}}{g_{d1} + g_{m1} + G_s + j\omega(C_{gs1} + C_{gd1})}, \quad (1)$$

where $G_s = \frac{1}{R_s}$. The input admittance can be written as

$$Y_{in} = j\omega\left[C_{gd1} + C_{gs1}(1 - G_v)\right]. \quad (2)$$

To achieve a voltage gain close to unity, the input admittance is set equal to the gate drain capacitance C_{gd}, i.e., much lower than the gate-source capacitance C_{gs}. The noise performance of an LNA is dominated by the input stage. Thereby, and in order to simplify the analysis, only the input stage noise analysis is considered here. Thus, the condition that allows the simultaneous noise and input matching is now:

$$Z_{opt} = Z_{in}^*. \quad (3)$$

Using inductive degeneration allows a noise figure close to the minimum noise figure (F_{min}) and a reduced input voltage standing wave ratio (VSWR). The wideband input matching is achieved by a suitable choice of C_{g1}, C_{d3}, L_{d1}, and L_{d2}. L_{d2} is the serial peaking inductor to boost the gain of T_2 in the low ultra-wideband (UWB) range and ensure the bias of the second stage of the LNA circuit. The last stage uses the source degeneration inductor L_{s3} to adjust the gain flatness while the serial peaking inductor L_{g3} can boost the gain and output matching in the wideband range. The series feedback capacitance C_{s1} is used to obtain simultaneous noise and input matching without degrading the noise figure.

To analyze the behavior of an LNA noise figure at frequencies where its noise figure is close to the minimum noise figure,let us consider the general expression of the noise figure

$$NF = NF_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2. \quad (4)$$

Three of the four parameters in Eq. (4) are constants determined by the device characteristics at a given frequency, so the amplifier noise figure is completely determined by the source impedance Z_s[32−38].

The main function of this LNA is to increase the input signal level, while at the same time minimizing the increment of the SNR. These two tasks are not always easily achieved simultaneously, the main reason being the noise impedance matching and the input matching are not always obtained for the same source impedance.

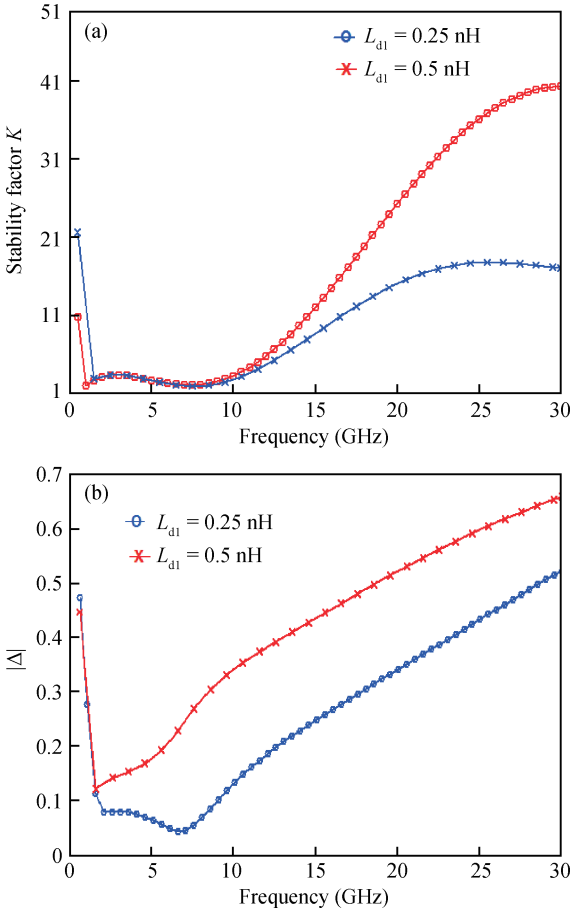

Fig. 5. Stability of the proposed LNA. (a) Rollet's factor. (b) Absolute value of delta ($|\Delta| < 1$).

4. Simulation results

The proposed wideband LNA is simulated using the ADS circuit simulation tool[30]. The bias point is fixed to $V_{DS} = 1$ V and $I_D = 0.2I_{DSS} = 37$ mA. This LNA is a three-stage circuit with all three transistors operating at the same bias condition.

The LNA gives the best results without the interstage matching network and with an L_{d1} value between 0.25 and 0.5 nH. The proposed LNA amplifier exhibits a maximum gain of 27 dB gain with an output return loss of below –11.5 dB and an input return loss lower than –10 dB, this circuit gives best input impedance matching ($S_{11} < -13$ dB) for $L_{d1} = 0.5$ nH.

The circuit also showed unconditional stability up to 30 GHz by employing the signal flow theory and S-parameters which show the Rollet's factor, given by[37]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}, \quad (5)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \quad (6)$$

The unconditionally stability requirement of the LNA is ($K > 1$) and $|\Delta| < 1$. It is shown in Fig. 5; with a total power dissipation of 85 mW.

The common-drain and common-source stages of the proposed LNA, operating from power supplies of 1.5 V and 1.8 V, respectively, were designed to include the on-chip output matching network. The obtained simulation results in-

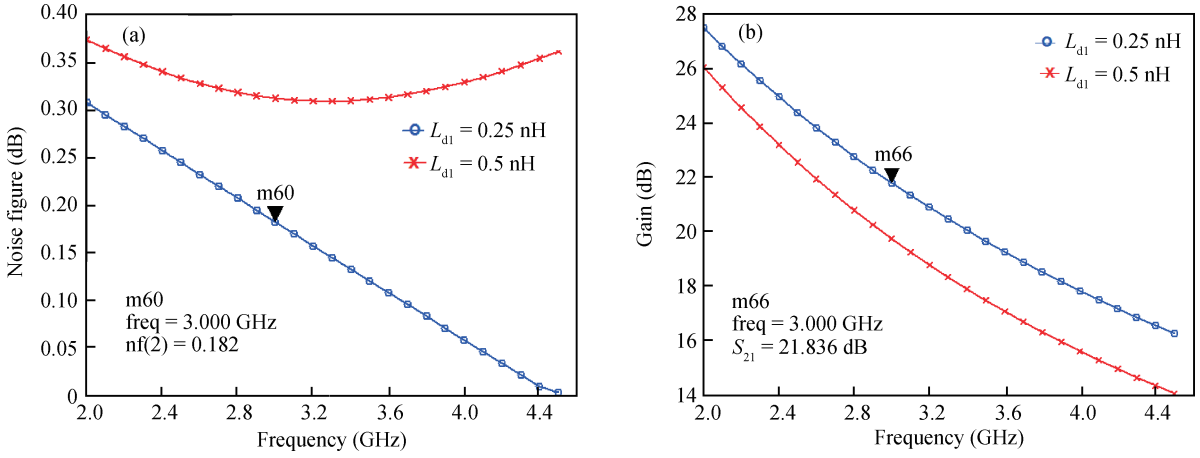

Fig. 6. (a) Noise figure and (b) power gain (S_{21}) of the simulated LNA.

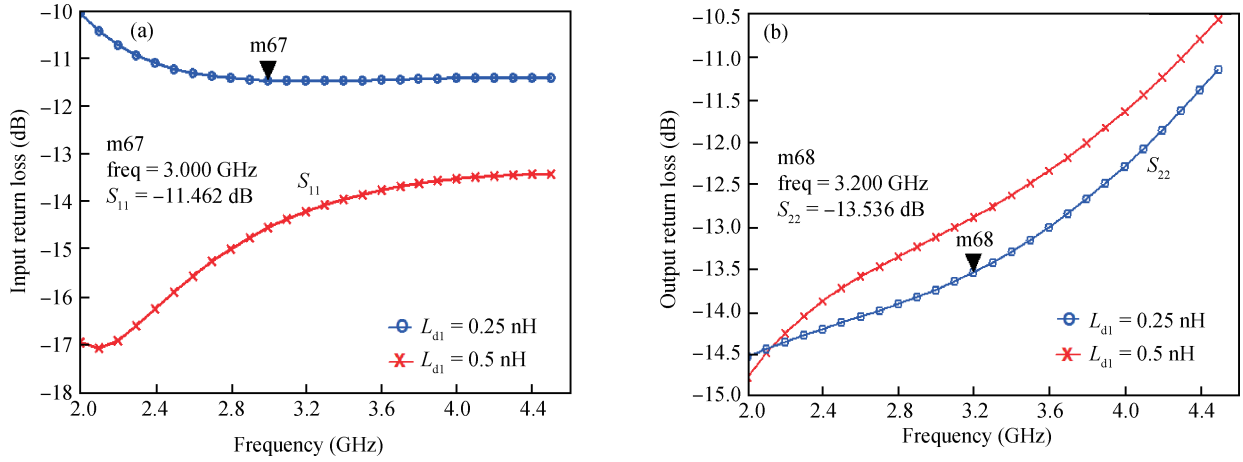

Fig. 7. (a) Input return losses (S_{11}) and (b) output return losses (S_{22}) of the simulated LNA.

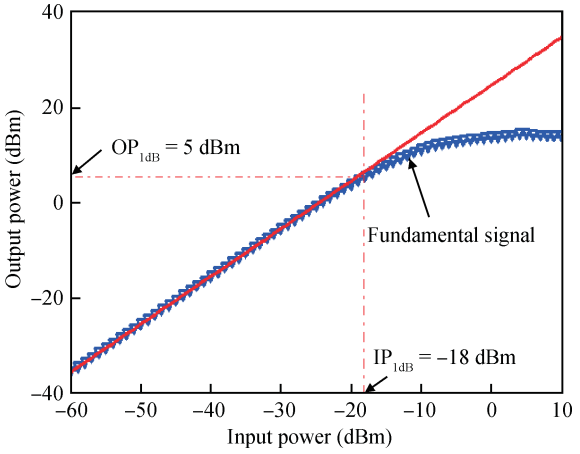

Fig. 8. Simulation of 1 dB compression point.

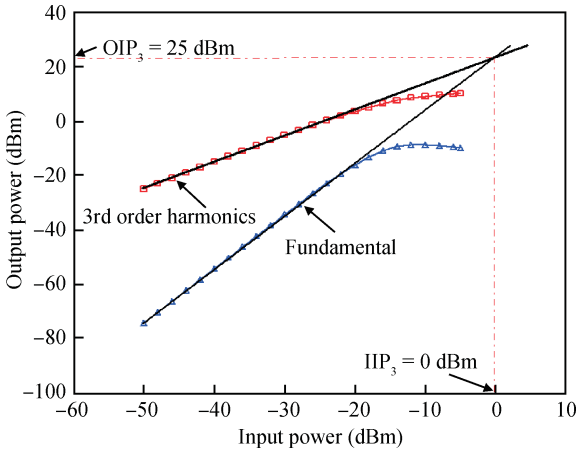

Fig. 9. Simulation of third intercept point of the proposed LNA.

clude the effects of series resistances of on-chip inductors. A minimum noise figure slightly below 0.3 dB with associated gain above 16 dB at mid-band was obtained. Figures 6 and 7 show the simulated noise figure and S-parameters, respectively, while Table 1 summarizes the performance of the designed circuit and also compares it to other designs (both simulations and measurements). Our results clearly show the competitiveness of this design for SKA receivers.

The 1-dB compression point of the LNA is also simulated. Thus, input and output 1-dB compression points are found to be –18 dBm and 5 dBm at 2.5 GHz, respectively (Fig. 8). The simulated input third order intercept point (IP3) is around 0 dBm

Table 1. Summary of simulated LNAs using a 2×400 μm transistor compared with other designs in the literature.

Parameter	Proposed topology		Ref. [17]	Ref. [32]	Ref. [18]	Ref. [39]	Ref.[40]
	$L_{d1} = 0.25$ nH	$L_{d1} = 0.5$ nH					
Freq (GHz)	2–4	2–4	0.3–2	0.4–2	0.8–1.8	4–5	0.1–1.3
NF (dB)	< 0.3	< 0.37	0.94	0.62	< 1	0.6	1.6
NF_{min} (dB)	< 0.21	< 0.28	0.52	0.5	0.8	*	*
$Gain_{max}$ (dB)	> 17.89	> 15.67	11.9	11	> 23	> 21	25
$\|S_{11}\|$ (dB)	< -10.06	< -13.52	–2.3	–10.11	*		
$\|S_{22}\|$ (dB)	< -11.64	< -12.28	–17	–36	*		*
IP_{1dB} (dBm)	–18	–18	*	–26	*		*
OP_{1dB} (dBm)	5	5	*	3.5	*		*
IIP_3 (dBm)	0	0	*	-5	*		*
OIP_3 (dBm)	25	25	*	25	15		
V_{DD} (V)	1.8	1.8	*	2	*		*
P_{DC} (mW)	84.5	84.5	110	55	90	*	*
Topology	CD[1] + CS[2]	CD + CS	C.S	Cascode	DLNF[3]	Cascade	Differential
Technology	1 μm pHEMT (InP)	1 μm pHEMT (InP)	1 μm pHEMT (InP)	1 μm pHEMT (InP)	0.18 μm CMOS	pHEMT GaAs	pHEMT
Meas/sim[4]	sim	sim	sim	Sim	meas	sim	sim

[1]CD: Common drain; [2]CS: Common source; [3]DLNF: Dual loop negative feedback, power to power; [4]Meas/sim: measured/simulated.

(Fig. 9).

Since our amplifier stages are designed for radioastronomy applications, all passive components are on chip, exhibiting a low noise figure (< 0.4 dB) over an acceptable wideband frequency range (2–4.5 GHz). It has to be noted that since submicron devices are prone to oscillations at low frequencies, the circuit can be highly unstable. Large periphery transistors are utilized for low noise resistance and wideband operation, especially at frequencies of less than 2 GHz. Therefore, a high breakdown InGaAs-InAlAs pHEMT device is used in this work[29, 34–37].

The excellent low noise characteristics of the InP-based HEMT make it a natural choice for low noise applications. However, manufacture on a large scale is difficult due to the limited size, high cost and the brittle nature of the InP substrate. Furthermore, achieving a noise figure value close to the minimum noise figure across a wide frequency band is significantly more complicated. Thus, by using an inductive degeneration in our wideband application, a noise figure very close to the minimum noise figure is obtained along with a reduced input VSWR.

5. Conclusion

A two-stage common-drain and common-source wideband low noise amplifier (LNA) suitable for the upcoming Square Kilometre Array telescope is presented in this paper. Large gate periphery pHEMTs have been fabricated using a novel InGaAs/InAlAs/InP structure to limit current leakage and to exhibit a high breakdown voltage. The advantages of this topology are discussed and wideband design techniques for input matching and low noise are proposed.

In fact, the designed LNA exhibits a lower noise figure than existing conventional configurations. The simulation results of the proposed LNA show an input/output matching of less than –10 dB, a maximum gain of 27 dB and a noise figure of less than 0.3 dB at 2 GHz with a power consumption of 85 mW. A comparison with existing designs demonstrated the high performance of our circuit for applications radio astronomy and wireless communication systems.

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