An IO block array in a radiation-hardened SOI SRAM-based FPGA

Zhao Yan(赵岩)†, Wu Lihua(吴利华), Han Xiaowei(韩小炜), Li Yan(李艳), Zhang Qianli(张倩莉), Chen Liang(陈亮), Zhang Guoquan(张国全), Li Jianzhong(李建忠), Yang Bo(杨波), Gao Jiantou(高见头), Wang Jian(王剑), Li Ming(李明), Liu Guizhai(刘贵宅), Zhang Feng(张峰), Guo Xufeng(郭旭峰), Zhao Kai(赵凯), Stanley L. Chen(陈陵都), Yu Fang(于芳), and Liu Zhongli(刘忠立)

Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China

Abstract: We present an input/output block (IOB) array used in the radiation-hardened SRAM-based field-programmable gate array (FPGA) VS1000, which is designed and fabricated with a 0.5 μm partially depleted silicon-on-insulator (SOI) logic process at the CETC 58th Institute. Corresponding with the characteristics of the FPGA, each IOB includes a local routing pool and two IO cells composed of a signal path circuit, configurable input/output buffers and an ESD protection network. A boundary-scan path circuit can be used between the programmable buffers and the input/output circuit or as a transparent circuit when the IOB is applied in different modes. Programmable IO buffers can be used at TTL/CMOS standard levels. The local routing pool enhances the flexibility and routability of the connection between the IOB array and the core logic. Radiation-hardened designs, including A-type and H-type body-tied transistors and special D-type registers, improve the anti-radiation performance. The ESD protection network, which provides a high-impulse discharge path on a pad, prevents the breakdown of the core logic caused by the immense current. These design strategies facilitate the design of FPGAs with different capacities or architectures to form a series of FPGAs. The functionality and performance of the IOB array is proved after a functional test. The radiation test indicates that the proposed VS1000 chip with an IOB array has a total dose tolerance of 100 krad(Si), a dose survivability rate of 1.5×10^{11} rad(Si)/s, and a neutron fluence immunity of 1×10^{14} n/cm^2.

Key words: partially-depleted SOI; FPGA; IOB; radiation-hardened; ESD protection
DOI: 10.1088/1674-4926/33/1/015010 **EEACC:** 1265A

1. Introduction

Field-programmable gate arrays (FPGAs) are widely used in systems design with ever increasing complexity because of their lower depreciated mask costs and fast time-to-market compared with application-specific integrated circuits (ASICs). All these advantages are based on its configurability[1, 2]. SOI SRAM based FPGA is particularly appropriate for use in aerospace and military applications because of its higher silicon density, smaller parasitic capacitance, better latch-up immunity and better radiation-hardened performance. Several factors have to be considered in choosing a particular type of FPGA for a specific application. One key consideration is whether the mapping of the application of the input/output pins to the input/output block (IOB) of FPGA can meet the requirements of functionality and performance. Another challenge facing IOBs is that the electrostatic discharge (ESD) protection network must be credible especially for use in SOI-CMOS technology. Most FPGA IOBs cannot confirm the presence of an input/output pin, the TTL/CMOS level standard and the connection with the core logic before configuration. boundary-scan path circuit is also necessary for FPGA testing and programming. All the aforementioned features show the difference between the designs of the SOI-CMOS FPGA IOB array and ASICs. Thus, when proposing an IOB array design for a FPGA family, both the potential application conditions and the different IO cell organizations in the individual FPGA family members are taken into consideration[3]. By combining the advantages and challenges of FPGA with those of SOI, an IOB array used for a FPGA chip, named VS1000, is fabricated with a 0.5 μm SOI-CMOS logic process and presented in the current paper.

2. Overall architecture of the IOB array

As shown in Fig. 1, VS1000 is a 14×14 logic block (LB) array. An IOB is fixed at the end of each column and each row. Each IOB includes two or three IOCs. As basic components of the IOB array, the IOCs can be classified into four types according to their functionalities[3] and are described in Table 1.

The power IO supplies power to the input/output buffers of the I/O pad, the internal core circuit and the ground rail.

A dedicated-function IO is only used for programming (which includes a configuration clock pin (CCLK), an initialization pin (INITN), a done pin (DONE), mode pin (MOD) and a program pin (PROGRAM)) or JTAG, (which includes a test clock pin (TCK), a test data input pin (TDI), a test mode select pin (TMS) and a test data output pin (TDO)). Thus, it has no configurable resources and cannot be configured for other functions.

† Corresponding author. Email: zhaoyan20@semi.ac.cn
Received 27 June 2011

Table 1. Class of VS1000 FPGA IOCs.

Type	Function	Description	Pin name
Power IO	vcc	5 V power supply pin	VCC
	gnd	0 V ground pin	GND
Dedicated-function IO	configio	Input/output pin used for program	CCLK
	configod	Open-drain pin used for program circuit	INITN, DONE
	configin	Input pin used for program circuit	MOD, PROG
	jtagin	Input pin of JTAG	TCK, TDI, TMS
	jtagout	Output pin of JTAG	TDO
Programmable IO	user	Programmable tri-state IO	USER
Dual-purpose IO	dualout	User pin, output of program circuit	HDC, LDC
	dualio	User pin, input of program circuit	DIN
	gclk	User pin, input of global clock signal	GCLK
	gclkdout	User, global input, program output	DOUT

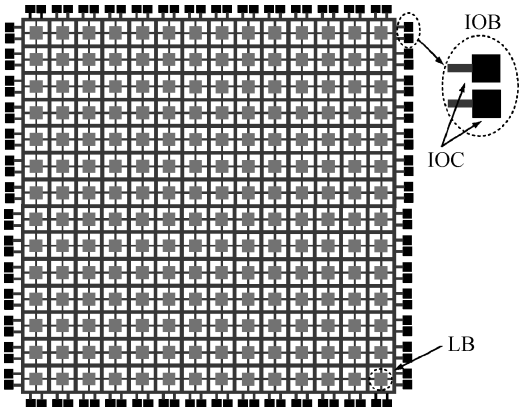


Fig. 1. Simplified diagram of the VS1000.

A programmable IO is a general-purpose user-defined input/output data interface when FPGA is in operation mode. The majority of the IOCs in the IOB array belong to this type. It provides multiple versatile modes for the user to configure in each FPGA application. Each individual user IO can be configured to comply with a special input/output standard in an application.

A dual-purpose IO can work either as a general-purpose user IO or a special-function IO. These IOs include some program circuit input/output pins and a global clock input pin. For example, in addition to being used as a user pin, the data out pin (DOUT) works either as the output pin of a program circuit or the input pin of a global clock tree which is distributed throughout the entire chip. If the pin is configured as an IO function, the other routing path will be turned off.

The number of IOCs in each bank, as well as their types and locations, are all specified in the FPGA architecture.

3. Circuit design of the IOB array

Although all four types of IOCs are different in their functionalities, their circuit structures can be divided into four segments: the signal path, the local routing pool, the IO buffer, and the ESD protection network. Furthermore, a special design is necessary to improve the anti-radiation performance.

The signal circuit of a typical IOC is composed of the data input/output path, the boundary-scan path, and the input/output buffer. The data path provides the user with the input and output path and registers. The boundary-scan path can be used to shift serial data into the register chain and load it into separate associated latches in the testing mode. The local routing pool is a programmable interconnected network between the data path and the chip routing channel. It is shared by adjacent IOCs in the same IOB. The configurable IO buffers provide dual IO standards for both the TTL and CMOS levels. Moreover, the ESD network provides the discharge path for the enormous electric charge.

3.1. Signal path circuit

Figure 2 shows the structure of the data path in the VS1000 FPGA. The signal path circuit includes three parts: the data path, the boundary-scan path, and the pad with an input/output buffer.

The data path is close to the core logic of the VS1000 FPGA and includes three configurable logic circuit paths: the input data path; the output data path; and the tri-state data path. Either the input or output data path has an individual register which latches or stores input/output data instead of using a register in the logic block so that it can shorten the data set-up time for the input data path and the clock-to-output time for the output data path. Furthermore, it provides a high data rate in data transmission applications. Each register can be configured as an edge-triggered D-typed register or a level-sensitive latch whose clock, enable signal, and set-reset polarities are also configurable.

The boundary-scan path is a point of intersection of the input/output path in an IOC and the boundary-scan chain in an IOB array. A boundary-scan chain is used in FPGAs mainly for test paths[4], which enhances the flexibility of FPGAs. As shown in Fig. 2, the boundary-scan path is composed of three registers, three latches and a configurable multiplexer. During the JTAG mode, the boundary-scan path logic can shift data on the boundary-scan chain of the entire IOB array and capture/update data from/into the pad/core logic through the different control signals and configurations. During the normal mode, the boundary-scan path can be by-passed. This structure ensures that VS1000 meets the test requirements in the JTAG mode.

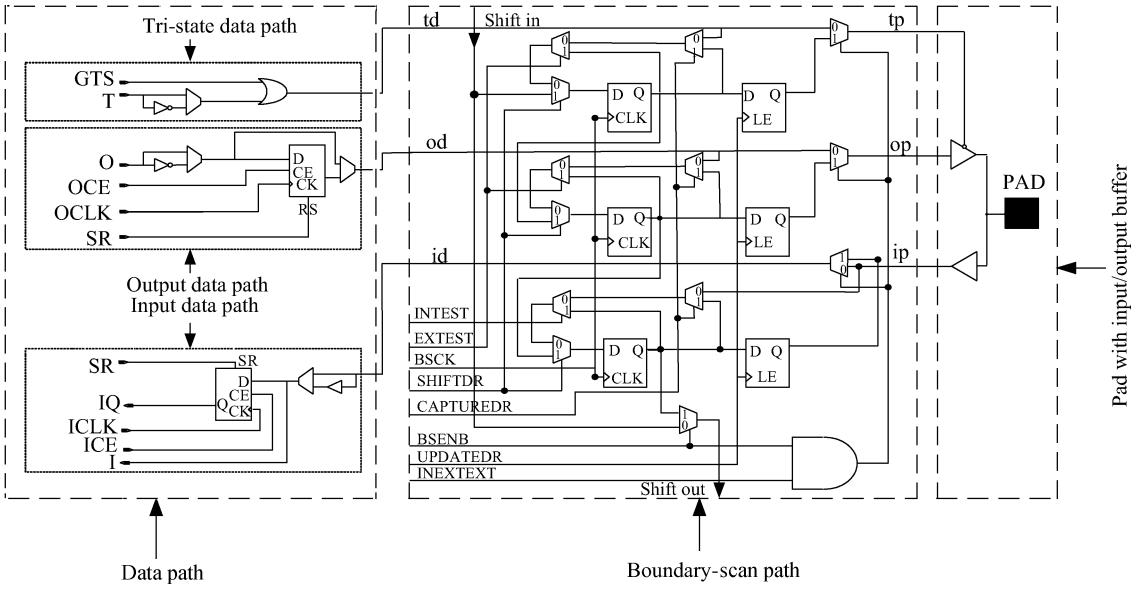


Fig. 2. Simplified signal path circuit diagram.

3.2. Programmable IO buffers

The IO pad can achieve both the 5 V TTL and 5 V CMOS standard work voltages of the VS1000 FPGA through programming. A programmable multiplexer can choose two input signals, which come from the TTL-CMOS and CMOS input drivers. Generally, a 5 V TTL output high level VOH > 2.4 V, the output low level VOL < 0.4 V, the input high level VIH > 2.0 V, and the input low level VIL < 0.8 V. Given that the threshold voltage of NMOS in the 0.5 μm SOI process is higher than 0.8 V, the 2.4 V input high level would make a conventional TTL-CMOS, which is composed of a cascaded CMOS inverter chain that produces quiescent current. Therefore, in the proposed TTL-CMOS design, an NMOS MN3 (Fig. 3) is added to ensure that when the input voltage is between 2.4 and 3.4 V, the PMOS MP3 is closed. Although MN3 would reduce the work frequency, the simulation result shows it can still meet the 100 MHz work frequency (Fig. 4).

The output drive of the VS1000 IO is realized based on the buffer introduced in Ref. [5] (Fig. 3). The output drive is composed of two couples of buffers, and each buffer has a PMOS and NMOS pull-up structure which can achieve the TTL level and CMOS level output. Table 2 shows the configuration information of the output buffer.

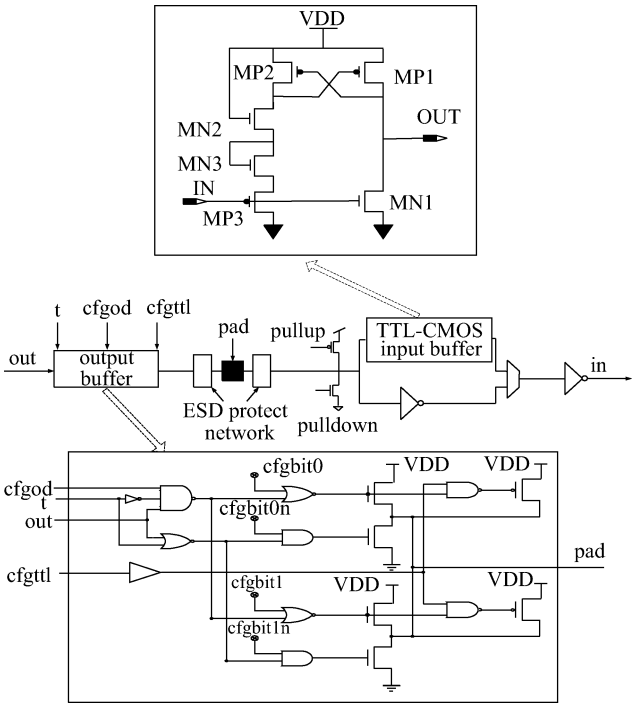


Fig. 3. Block diagram of the IO buffers.

3.3. IOB local routing pool

As shown in Fig. 5, the routable signals to and from the IOCs are connected through a shared programmable interconnected network, called the IOB local routing pool, to the external routing channel surrounding the IOB array. The IOB local routing pool is designed to increase the IO pin routing flexibility and resolve the congestion caused by pin-locking in the FPGA application. Since each IOB is composed of IOCs of different types, an automation tool, whose layout is based on the architectural specification of the target FPGA, is used to generate the routing switch pattern. In Fig. 5, the LRP is composed of four interconnections: the glrp, located between the global IOB input pin and the IOC clock input pin; the ilrp, located between the IOB and IOC input pins; the olrp, located between the IOB and IOC output pins; and the plrp, located between the power rail and the IOC input pin.

3.4. Radiation-hardened design

The SOI technologies have been regarded as contenders for long-time applications, in which electronics are exposed to radiation[6]. This is a consequence of the lower susceptibility to the transient effects produced by the reduced charge-collection volume relative to bulk technologies[7]. The VS1000 chip is

Table 2. Configuration information of output buffer.

MODE	Configurable bit				Description
	cfgod	cfgttl	cfgbit0	cfgbit1	
TTL mode	x	0	x	x	TTL voltage output
CMOS mode	x	1	x	x	CMOS voltage output
Fast slew rate	x	x	0	0	Fast slew rate output
Slow slew rate	x	x	0	1	Slow slew rate output
Open drain mode	0	x	x	x	Open drain output

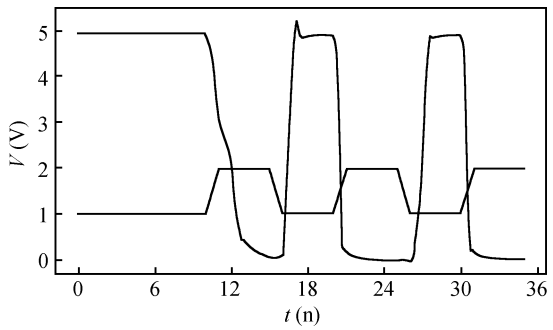


Fig. 4. Waveform of the IO input TTL-CMOS buffer operating at 100 MHz.

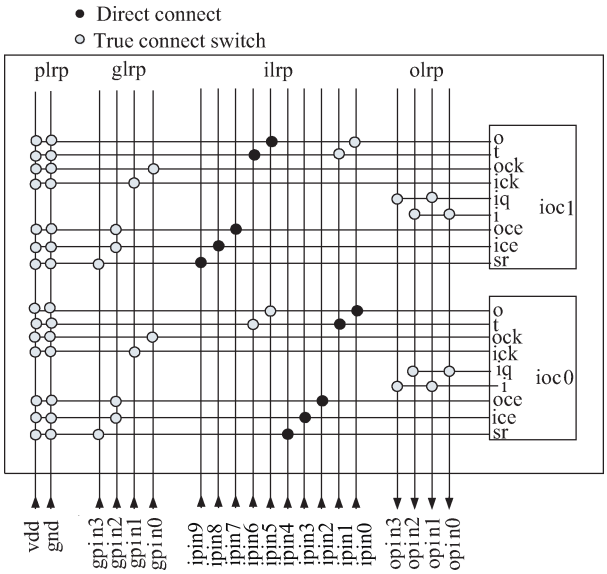


Fig. 5. Structure of the IOB local routing pool.

designed based on a 0.5 μm PD-SOI process. Contrary to the early assertion that the DC kink effect is largely responsible for PD-SOI's advantage over conventional bulk-Si technologies, the higher performance of PD-SOI is predominantly due to the dynamic effects during its switching events, especially at a high supply voltage, along with a dynamic kink effect that charges (or discharges) the floating body to its dynamic steady-state condition[8]. Every viable SOI device needs to have a good radiation-hardened design before it can be used in integrated circuit applications. When a high transient photocurrent is generated in the radiation environment, the floating-body effect in PD SOI induces the kink effect and triggers the parasitical BJT effect[9]. To avoid this, an efficient method is introduced in Ref. [9], which ties the bodies of SOI transistors to a stable voltage. As shown in Fig. 6, three types of body-tied embodiment transistors can be used in the design: the T-type, A-type, and H-type. A stable body provides the ability to transfer transient photocurrent quickly and improve the radiation-hardened performance. In addition, the smaller body-tied resistor is better in rapidly transferring transient photocurrent. Thus, the transfer transistor in the current I/O is constructed using an H-type body-tied structure instead of a T-type body-tied structure. Considering the area effect, the load and drive transistors in our I/O are constructed using an A-type body-tied structure.

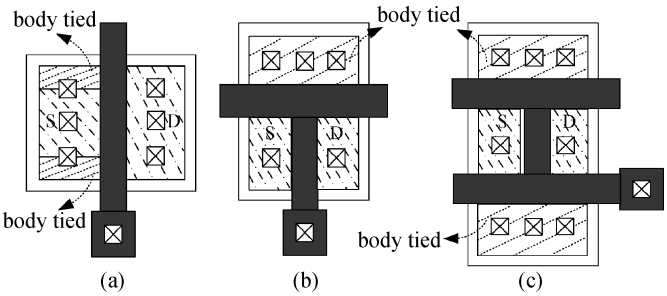
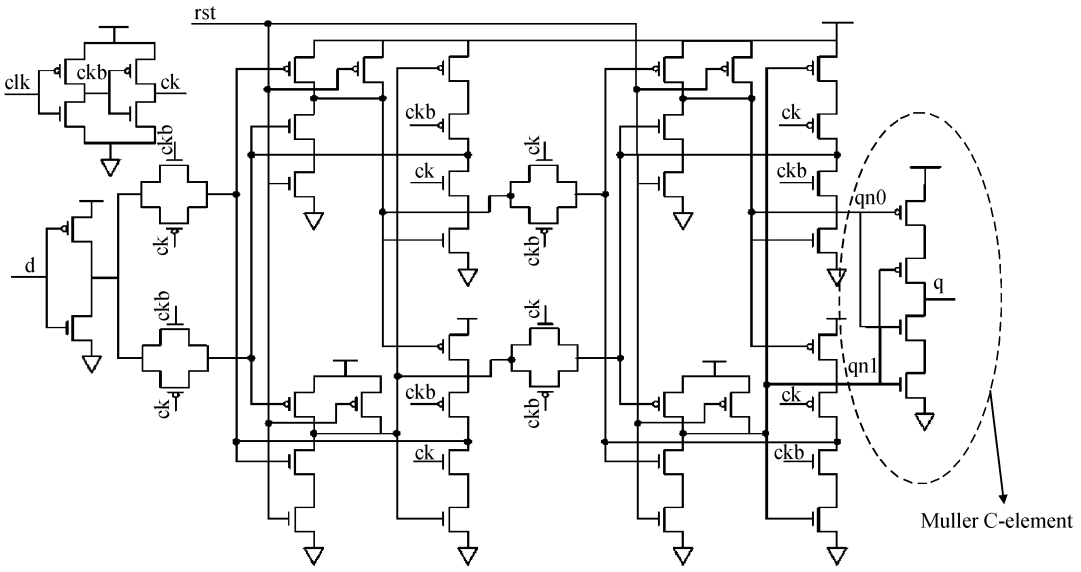


Fig. 6. (a) A-type body-tied structure. (b) T- type body-tied structure. (c) H-type body-tied structure.

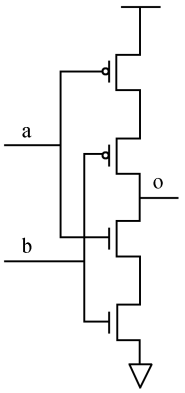
Aside from radiation hardening by technology (RHBT), radiation hardening by design (RHBD) is also used during the development of the VS1000 IOB array to enhance the radiation performance. A register design should be a free single event, not only during the static data storage phase, but also during the high frequency switching operation. We use a dual interlocked cell (DICE) structure register, which has been proven to have a high radiation-hardened performance[10], in the VS1000 chip equipped with the IOB array. A Muller C-element is added, as the last stage of the DICE register (Fig. 7) further improves the anti-SEU ability of the DICE register. For example, assuming that the out pin q of the register is 1 in some static storage cycle, i.e., both qn0 and qn1 are 0, when a high-energy particle upsets qn0 or qn1 temporarily changes to 1, q will be kept at 1. For the dual interlocked structure, qn0 or qn1 will recover after the energy of the high-energy particle has been released. Thus, the register possesses a high SEU resistance.

3.5. ESD protection scheme

Most VS1000 chips have a digital circuit. Thus, the ESD protection is designed in the IOB and power rail instead of in the core logic. The internal circuit is assumed fully isolated from the I/O pad. Except for the I/O ESD protection design itself, the focus of the ESD chip design in the VS1000 chip is to ensure a proper I/O pad ring layout design that accounts for the voltage drop in the power rail, the number of clamps, and the RC delay and to make sure that the current path for every pin-to-pin combination is addressed. In addition, a proper I/O pad ring should clamp the supply rail voltage and include the current path to safely divert the ESD discharge current[11].



(a)



a	b	o
0	0	1
1	1	0
0	1	hold
1	0	hold

(b)

Fig. 7. (a) Dual interlocked cell (DICE) register with a Muller C-element. (b) Muller C-element and the truth table.

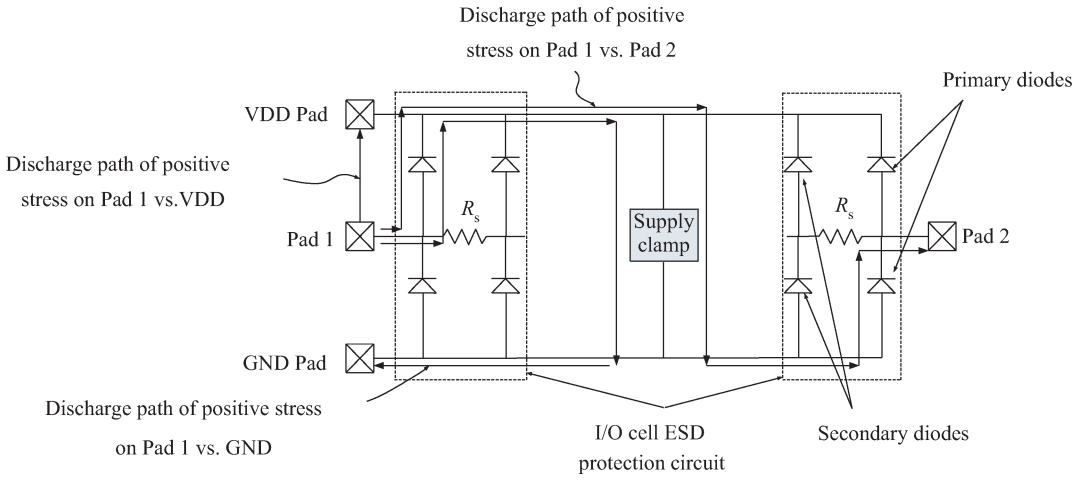


Fig. 8. Dual diode-based ESD protection structure.

ESD protection networks consisting of forward biased diodes and transient triggered active MOSFET rail clamps have been proven effective in advanced CMOS bulk[12] and SOI[13] products, which can be easily ported from bulk to SOI technologies. In VS1000, dual diodes based on the ESD protection scheme[14] are used to protect I/O pads (Fig. 8). The diodes are forward-biased and provide a low resistive discharge path for ESD stress. In addition, the discharge path of pad 1 versus

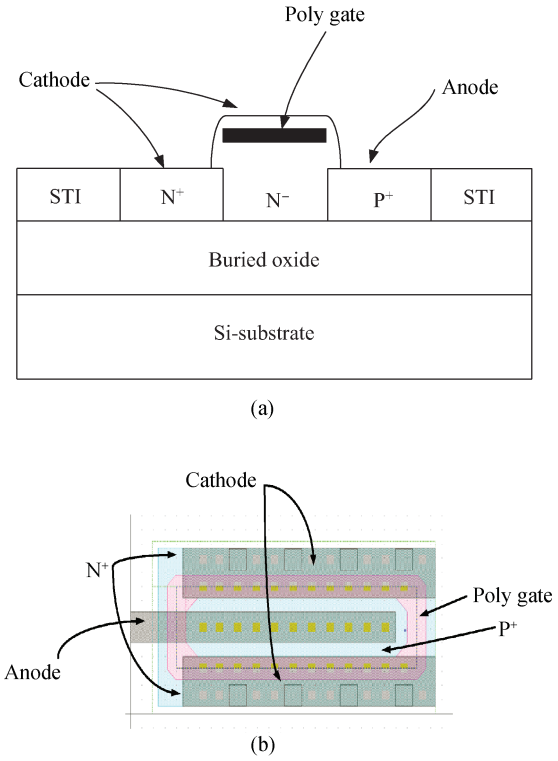


Fig. 9. (a) Cross-section of the poly-bound SOI diode. (b) Layout of the poly-bound SOI diode.

pad 2, pad 1 versus VSS, and pad 1 versus VDD is marked. A power supply rail is necessary for the dual diode-based structure. Although the I/O pad diode may break down, the diode cannot divert the whole ESD discharge current because the reverse-biased current capability is low. Thus, a series resistance and a secondary dual-diode stage are used to increase the ESD performance of the dual-diode structure.

Continuous changes in the SOI technologies and the emergence of new structure types with thinner silicon films, e.g., partially-depleted SOI (PDSOI), fully-depleted SOI (FDSOI), and double-gate SOI (DGSOI), have negative effects on the ESD performance. Thus, in the VS1000 chip, poly-bound diodes are used to protect against ESD in SOI technology, which is an improvement over the previous findings of combined bulk and SOI structures[15]. Figure 9(a) shows a cross-section of the poly-bound SOI diode, where the diode is formed as if it were a PMOS, except that the implant on one side is changed from P^+ to N^+ and both the halos and extensions are blocked on both sides of the structure. Figure 9(b) shows the layout of the poly-bound SOI diode in VS1000. In an SOI process flow, the structure is formed by first integrating a buried oxide and then forming the anode (P^+) and cathode (N^+) regions in the substrate (or handle-wafer region) using a standard source and drain implants. As a result, an N^+/P-substrate junction diode can be created. A deep N-well can also be introduced to isolate the structure by adding a high-energy implant to the process flow and create a P^+/N-well junction diode. Contacts are then added to connect the diode to the I/O circuit for protection. In this case, the gate poly defines the diode and the length of the diode base is equal to the length of the gate poly.

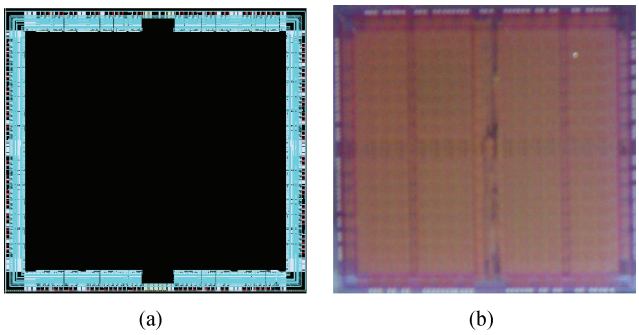


Fig. 10. (a) VS1000 IOB array layout. (b) VS1000 chip photo.

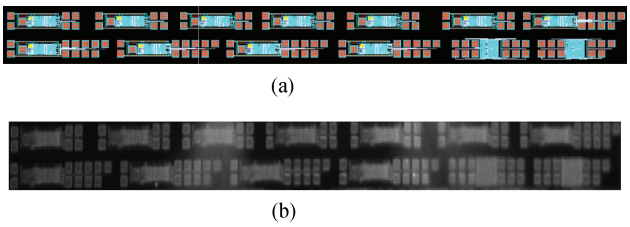


Fig. 11. (a) VS1000 IOB test layout. (b) VS1000 IOB photo.

4. Implementation and test results

4.1. Layout implementation

The current VS1000 FPGA design is implemented with a 0.5 μm partial-depletion SOI CMOS 1P3M processed at the CETC 58th Institute. The layout of the entire chip, including the IOB array, is fully custom-designed. The key constraints of the IOB array layout floor plan come from the requirements of the LB array width. Several wide power and ground rails simultaneously encompass the entire VS1000 chip, which also constrain the IOB array layout. According to the full chip floor plan, the proposed design has a metal M3 as the supply ring rails, M2 as the supply line in the horizontal direction, and metal M3 as the supply in the vertical direction, so that the supply layout in the IOB array and core logic forms a full-chip power network. The IOB array layout is shown in Fig. 10(a), whose size is about 10.2×9.5 mm^2 with a CQFP208 package. The full chip die photo is illustrated in Fig. 10(b).

4.2. Fault and function tests

We design IOC test chips (Fig. 11) before the FPGA full chip tapeout. Every IOC has a certain functional block because all programmable points are connected to a power supply or to the ground. A test on these test chips is conducted to make sure that the basic functions of the IOB work well based on the DIP14 package (Table 3).

After the FPGA tapeout, we test the VS1000 chip via a wafer test to select good dies. The final test is conducted to ensure that the selected dies are working well after packaging and to test the performance of VS1000 in a PCB board. All test experiments are performed using a Teradyne J750 test system at the CETC 58th Institute. VS1000 used a one clock-source during the wafer and final tests, resulting in a difference between the maximal work frequencies of the two tests. Table 4 provides the test results interrelated with the IOB.

Table 3. Test results of the IOB dies.

Test die name	Description	Test result
cmosio	5 V CMOS level tri-state control IO	Work well
ttlio	5 V TTL level tri-state control IO	Work well
cmossio	5 V CMOS level tri-state control IO with slow slew rate	Work well
ttlsio	5 V TTL level tri-state control IO with slow slew rate	Work well
cmosodio	CMOS open drain output	Work well
ttlodio	TTL open drain output	Work well
ioff0	IO register in synchronous clear '0' mode	Work well
ioff1	IO register in synchronous set '1' mode	Work well
ioff2	IO register in asynchronous clear '0' mode	Work well
ioff3	IO register in asynchronous set '1' mode	Work well
iolatch	IO register in latch mode	Work well

Table 4. Partial test results of the VS1000 chip.

Parameter	Wafer test	Final test	Applied test
Static current (mA)	10	10	—
Functional test	Pass	Pass	Pass
Maximal program frequency (MHz)	25	25	—
Maximal work frequency (MHz)	25	25	100
CMOS input high level (V)	4.2	4.2	4.2
TTL input high level (V)	2.0	2.0	2.0
CMOS input low level (V)	0.8	0.8	0.8
TTL input low level (V)	0.8	0.8	0.8

Table 5. Radiation test results.

Radiation test	Radiation tolerance
TID	100 krad(Si)
Dose rate	1.5×10^{11} rad(Si)/s
Neutron fluence	1×10^{14} n/cm^2

4.3. Radiation test

FPGA is the only active device placed on the radiation test board so that the radiant effects of other devices do not interfere with the test results. Radiation tests include the total ionizing dose (TID), dose rate, and neutron fluence tests. We program the VS1000 and read back through the JTAG pins during the radiation test. A user pin is also used as the input or output pin during the radiation tests. FPGA is considered a failure if we detect an error in the readback bitstream or in the output signals. The radiation test results are listed in Table 5.

5. Conclusions

In the current paper, a radiation-hardened IOB array used for FPGA VS1000 is designed and fabricated with a 0.5 μm partial-depletion SOI logic process. The organization of the array, the data path structure, the boundary-scan path structure, the local routing pool for IOB, configurable TTL-CMOS IO buffers and the ESD protection network are also presented. Two types of body-tied embodiment transistors, the A-type and H-type, are applied in the IOB array, together with a DICE structure register with a Muller C-element. The combination improved the radiation-hardened performance. A dual diode-based ESD protection scheme with a poly-bound diode is used to protect the I/O pads. The IOB array is used in the VS1000 chip but is not limited to a specific FPGA structure. The IOB dies and VS1000 full chip tests show that the IOB circuit can actualize its programmable function and meet the requirements of the input/output level and frequency. The radiation test results show that the IOB array has a total dose tolerance of 100 krad(Si), a dose rate survivability of 1.5×10^{11} rad(Si)/s, and a neutron fluence immunity of 1×10^{14} n/cm^2, which result from the RHBT and RHBD.

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