A wideband LNA employing gate-inductive-peaking and noise-canceling techniques in 0.18 μm CMOS*

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Abstract: This paper presents a wideband low noise amplifier (LNA) for multi-standard radio applications. The low noise characteristic is achieved by the noise-canceling technique while the bandwidth is enhanced by gate-inductive-peaking technique. High-frequency noise performance is consequently improved by the flattened gain over the entire operating frequency band. Fabricated in 0.18 μm CMOS process, the LNA achieves 2.5 GHz of –3 dB bandwidth and 16 dB of gain. The gain variation is within $\pm$0.8 dB from 300 MHz to 2.2 GHz. The measured noise figure (NF) and average IIP3 are 3.4 dB and –2 dBm, respectively. The proposed LNA occupies 0.39 mm^2 core chip area. Operating at 1.8 V, the LNA drains a current of 11.7 mA.

Key words: low noise amplifier; wideband LNA; gate-inductive-peaking; noise-canceling; wideband input matching

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1. Introduction

Global navigational satellite systems (GNSSs) have been drawing many countries' attention for its increasing influence on daily life and public security. Different modes like GPS, GLONASS, Galileo and Compass are emerging and progressing rapidly. To provide seamless indoor/outdoor navigation and communication capabilities, the concept of an integrated GNSS/UMTS (universal mobile telecommunications system) receiver, using GPS/Galileo and 3G/UMTS for mass market navigational applications has recently been proposed[1]. In the meantime, standards such as WLAN and Bluetooth have also been merged into multi-standard terminals for short-range communication. Based on the evolutionary software defined radio (SDR) concept[2], a reconfigurable receiver is proposed to support multiple radio standards across multiple frequency bands. The receiver, as shown in Fig. 1, is reconfigurable for agile service switching and adaptive power consumption in response to radio dynamics. In this architecture, the receiver's RF front-end is shared among different modes and a wideband low noise amplifier (LNA) is needed to amplify all the received signals before down conversion and baseband processing.

The design of wideband LNAs poses many challenges. Traditional techniques used in narrowband LNAs, such as adding an inductor at the load to create a resonance at a certain frequency, are not suitable for wideband LNAs[3]. Secondly, since the LNA is the first stage connecting to off-chip components in a receiver, wideband input impedance matching and low noise characteristic over the entire operating bandwidth have to be achieved. For a wideband LNA, a small chip area is also preferred, especially for system-on-chip applications in order to reduce the manufacturing cost.

The noise-canceling technique is efficient to design wideband LNAs[4−8] since it can break the tradeoff between input matching and noise figure[4]. However, parasitic capacitance can degrade the gain of the amplifier at high frequency, which consequently degrades the high-frequency noise performance. The decline of the gain also complicates the design of the receiver because of the varied signal amplification across the whole spectrum in the downstream receiver path.

In this paper, a wideband LNA using noise-canceling and gate-inductive-peaking techniques is presented. A gate inductor is used to extend the bandwidth of the matching amplifier stage and the voltage-sensing amplifier stage simultaneously. The proposed technique splits the poles of the two stages and pushes the complementary poles to higher frequency. As a result, the bandwidth of the gain is extended and the noise performance at high frequencies is improved.

2. Basic noise-canceling technique

Since it was originally proposed to reduce the noise figure of the feedback amplifiers at low gigahertz frequency ranges[4], the noise-canceling technique has become a popular technique for designing wideband LNAs[5−8]. Figure 2 illustrates the generalized model of the noise-canceling architecture. It simply consists of a matching amplifier stage, an auxiliary voltage-sensing amplifier stage and a network combining the output of the two amplifiers. Noise from the matching stage cancels while signal contributions add.

Figure 3 shows a simplified realization of the concept in Fig. 2. The channel thermal noise of the matching device M1, which is a dominant noise component in a submicron CMOS device, can be modeled as a noise current source I_n. A portion of this thermal noise current αI_n flows out of M1 through R_f and R_S, where $0 < \alpha < 1$, and causes two correlated noise voltages at nodes X and Y, which are in phase and can be expressed

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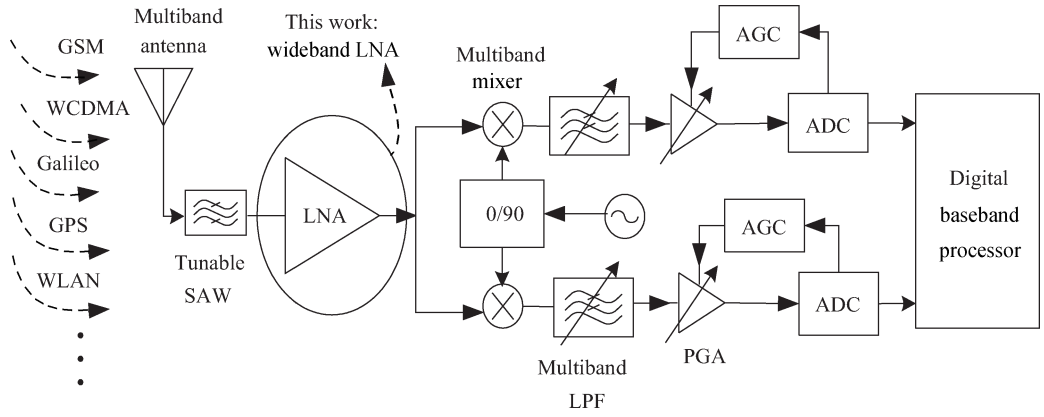

Fig. 1. Block diagram of the multi-standard receiver.

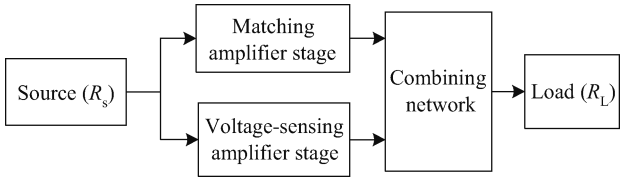

Fig. 2. Block diagram of an LNA exploiting noise cancellation.

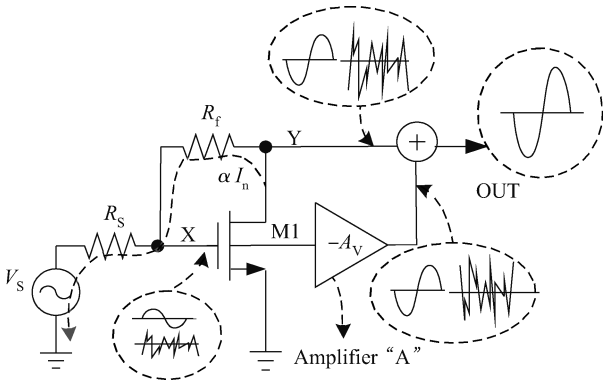

Fig. 3. Wide-band LNA exploiting noise-canceling technique.

as

$$V_{X,n} = \alpha I_n R_S, \tag{1}$$

$$V_{Y,n} = \alpha I_n (R_S + R_f). \tag{2}$$

Meanwhile, because of the negative gain of the common source amplifier, the signal voltages at nodes X and Y are in opposite phases. This difference in noise and signal makes it possible to cancel the noise of the matching device M1 while adding the signal contributions constructively. It can be done by adding a negatively scaled replica of the voltage at node X to the voltage at node Y as illustrated in Fig. 3. The output noise voltage after noise canceling operation can be derived as

$$V_{out,n} = \alpha I_n (R_S + R_f) - A_V (\alpha I_n R_S). \tag{3}$$

Output noise cancelation, $V_{out,n} = 0$, is achieved when the gain A_V equals

$$A_V = 1 + \frac{R_f}{R_S}. \tag{4}$$

In the meantime, signals along the two paths add up constructively. The overall gain can be written as

$$G_V = -2\frac{R_f}{R_S}. \tag{5}$$

Since noise-canceling LNAs sense the dominant noise of the amplifier and use a feedforward path to cancel this contribution over a wide frequency range, it is suitable to be used in multi-standard receivers. However, the noise-canceling technique has high frequency limitations, which not only limits the gain bandwidth, but also degrades noise and distortion cancelation. In the following section, the gate-inductive-peaking technique will be analyzed in depth to show how it improves the high frequency performance of the proposed LNA and how the bandwidth is extended.

3. Gate-inductive-peaking technique

In order to enhance the –3 dB bandwidth of an amplifier, the inductor shunt peaking technique, which adds an inductor in series with the load resistor, has been commonly used[9, 10]. However, the inductor, which is usually placed at the drain of the MOSFET, is very large and consumes a great deal of area.

In this paper, a gate-inductive-peaking technique with an inductor placed at the gate of the input transistor is presented. Using this topology, a much smaller inductor is needed to achieve a similar bandwidth extension while the gain flatness is improved simultaneously. In this section, the gate peaking inductor's effect on the matching amplifier stage and the voltage-sensing amplifier stage will be analyzed respectively. Afterwards, the improvement of noise performance will be summarized.

3.1. Gate-inductive-peaking for the matching amplifier stage

In noise-canceling topology, a common source amplifier with a resistive feedback, shown in Fig. 4(a), is used to provide wideband input impedance matching with its input impedance $Z_{in} = 1/g_{m1}$ and gain $v_Y/v_X = 1 - g_{m1}R_f$.

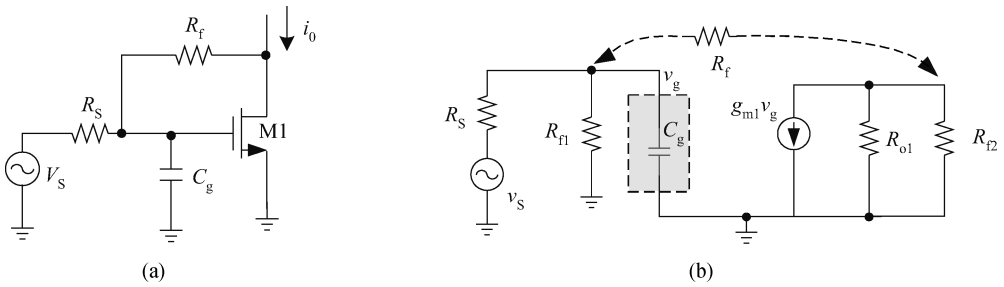

Fig. 4. (a) Common source amplifier with resistive-feedback. (b) Small signal equivalent circuit of (a).

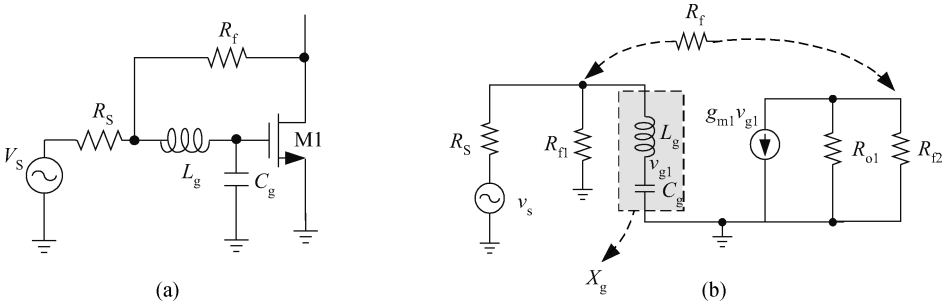

Fig. 5. (a) Cascode amplifier with gate-inductive-peaking technique. (b) Small signal equivalent circuit of (a).

The small signal equivalent circuit of the matching stage amplifier is shown in Fig. 4(b), where R_{f1} and R_{f2} are miller equivalent resistors of R_f and C_g is the sum of C_{gs1}, Miller equivalent capacitor of C_{gd1} and other possible capacitors at the input port. The signal voltage at the gate of M1 is derived as

$$v_g = v_s \frac{R_{f1}||\dfrac{1}{sC_g}}{R_S + R_{f1}||\dfrac{1}{sC_g}} = v_s \frac{R_{f1}}{R_S R_{f1} C_g s + (R_S + R_{f1})}. \quad (6)$$

Then, the voltage gain A_v of the amplifier in Fig. 4(a) can be derived as Eq. (7). The transfer function has one pole approximately at $s = -(R_S + R_{f1})/R_S R_{f1} C_g$.

$$A_v = -\frac{g_{m1} v_g (R_{f2}||r_{o1})}{v_s} = -\frac{g_{m1} R_{f1} (R_{f2}||r_{o1})}{R_S R_{f1} C_g s + (R_S + R_{f1})}. \quad (7)$$

After introducing the peaking inductor at the gate of M1, the schematic and the small signal equivalent circuit of the matching stage are shown in Fig. 5.

We assume:

$$X_g = sL_g + \frac{1}{sC_g}. \quad (8)$$

The signal voltage at the gate of M1 can be derived as:

$$v_{g1} = v_s \frac{R_{f1}||X_g}{R_S + R_{f1}||X_g} \frac{\dfrac{1}{sC_g}}{X_g}. \quad (9)$$

Naturally, the transfer function is derived as

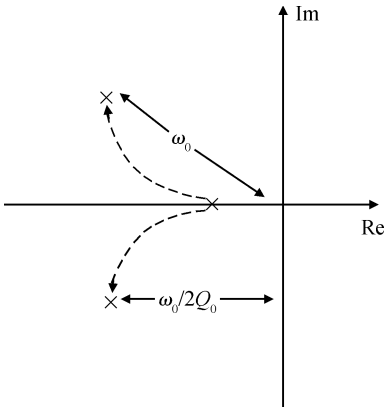

Fig. 6. Pole splitting and pushing in S-plane.

$$A_v = -\frac{g_{m1} v_{g1} (R_{f2}||r_{o1})}{v_s} = -\frac{g_{m1} R_{f1} (R_{f2}||r_{o1})}{(R_S + R_{f1}) L_g C_g} \frac{1}{s^2 + \dfrac{\omega_0}{Q_0} s + \omega_0^2}, \quad (10)$$

where

$$\omega_0 = \frac{1}{\sqrt{L_g C_g}}, \quad (11)$$

$$Q_0 = \frac{\sqrt{L_g C_g}(R_S + R_{f1})}{R_S R_{f1} C_g}. \quad (12)$$

The real parts of the complementary poles at the transfer function are both $-\omega_0/2Q_0$ and they can be placed at higher frequency by adjusting the value of L_g. Therefore, the gain rolls off at higher frequency although the roll-off is twice as

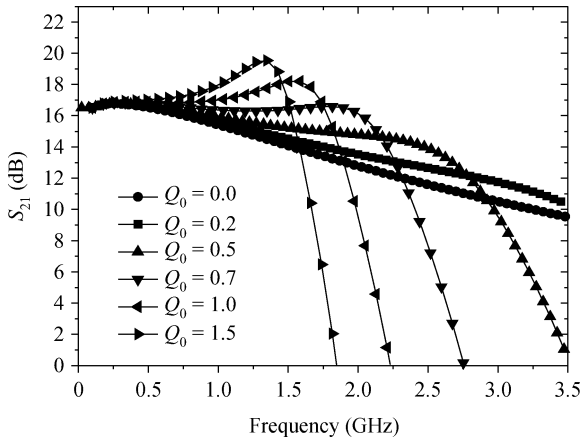

Fig. 7. Gain of the C–S amplifier with different Q_0.

fast. The mechanism of the pole splitting is illustrated in Fig. 6.

From Eqs. (11) and (12), the value of L_g defines Q_0. Q_0 is related to the frequency response of the common source amplifier. High Q_0 will result in gain peaking, as shown in Fig. 7. Good gain flatness can be obtained by setting Q_0 around 0.7.

3.2. Inductive-peaking for the voltage-sensing amplifier stage

In Bruccoleri's noise-canceling topology, a cascode amplifier provides an auxiliary path to cancel the noise from the matching amplifier stage. It is expected that the gain of the noise-canceling amplifier is stable and flat over LNA's operating frequency band, and thus the noise of the matching stage can be canceled to the utmost. Cascode amplifier features high gain and good reverse isolation, and mitigates the Miller effect. Nevertheless, gain degradation over 2 GHz is still severe.

The gate-inductive gain peaking technique is used to enhance the high frequency gain of the cascode amplifier and the gain flatness. The inductor L_g is connected to the gate of M1, as shown in Fig. 8(a), which introduces two complementary poles.

The small signal equivalent circuit of the cascode amplifier is shown in Fig. 8(b). Similar to part A, the transfer function of the cascode amplifier is derived as

$$A_V = -\frac{g_{m1}r_{o1}(1+g_{m2}r_{o2})R_D}{2(r_{o1}+r_{o2}+g_{m2}r_{o1}r_{o2})}\frac{1}{L_gC_{gs1}}\frac{1}{s^2+\dfrac{\omega_0'}{Q_0'}s+\omega_0'^2}, \tag{13}$$

where

$$\omega_0' = \frac{1}{\sqrt{L_gC_g}}, \tag{14}$$

$$Q_0' = \frac{1}{R_S}\sqrt{\frac{L_g}{C_{gs}}}. \tag{15}$$

The real parts of the complementary poles at the transfer function are both $-\omega_0'/2Q_0'$. Comparing Eq. (11) and Eq. (14), the absolute values of the complementary poles of both stages are the same, which makes it convenient to compromise the value of L_g between the two stages. In order to achieve a flat and extended gain bandwidth, the required inductor for the

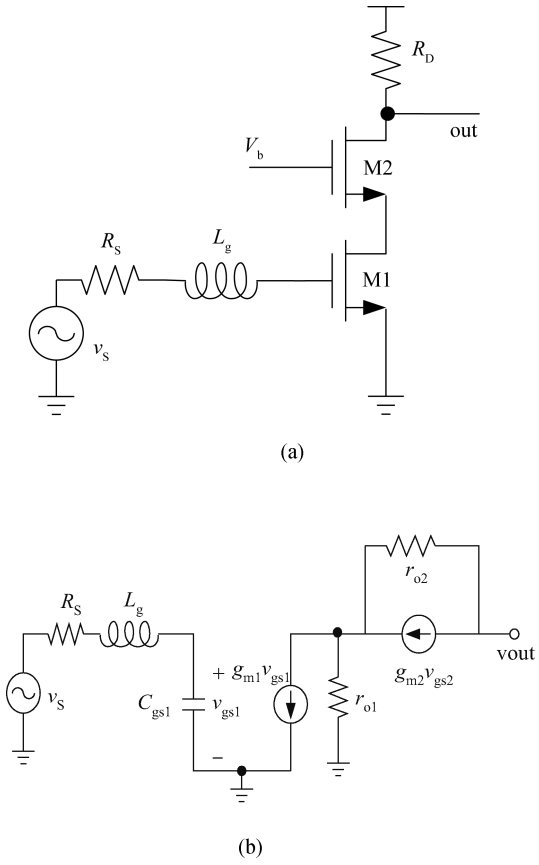

Fig. 8. (a) Cascode amplifier with gate-inductive-peaking technique. (b) Small signal equivalent circuit of (a).

voltage-sensing stage is a little smaller than that for the matching amplifier stage. The difference is caused by the mitigated Miller capacitances of the cascode structure. So one medium inductor is exploited to achieve slight overshoot for voltage-sensing amplifier stage while slight roll-down for the matching amplifier stage. The two stages compensate each other to get a flat gain.

3.3. Noise performance improvement by using the inductive peaking technique

The noise-canceling technique cancels noise which can be modeled by a current source between the drain and source of the matching device, such as $1/f$ noise, thermal noise of the distributed gate resistance and the bias noise current injected into node Y. However, noise from R_f and the voltage sensing stage is not canceled[4].

Considering Fig. 3, the noise figure of the LNA can be written as:

$$F = 1 + \underbrace{\frac{\gamma g_{d0}}{g_{m1}}\frac{(R_f+R_s-A_VR_s)^2}{R_sA_{VF}^2}}_{\text{MD}} + \underbrace{\frac{2}{A_{VF}}}_{\text{Rf}} + \underbrace{\frac{N_A}{g_{m1}}\frac{8-6A_{VF}+A_{VF}^2}{R_SA_{VF}^2}}_{\text{A}}. \tag{16}$$

Each term in Eq. (16) represents the contribution of the

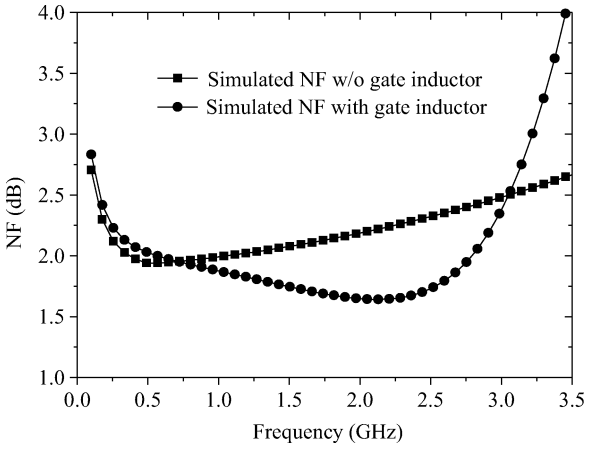

Fig. 9. Simulated noise figure with and w/o L_g.

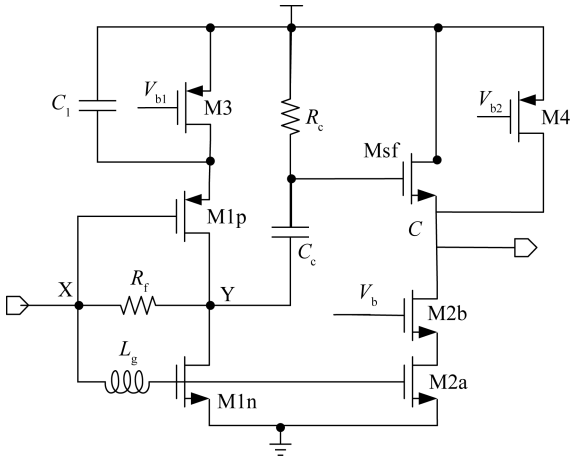

Fig. 10. Simplified schematic diagram of gate inductors.

corresponding device, where index MD refers to the matching device, R_f to the feedback resistor, A to amplifier A, A_{VF} to the overall voltage gain, N_A to the output noise power of amplifier A and A_V to the voltage gain of amplifier A.

As shown in Eq. (16), exact noise cancelation occurs only at low frequency when $A_V = 1 + R_f/R_S$. As frequency increases, the cancelation degrades because of gain degradation and parasitic capacitances. As mentioned by Bruccoleri[4], the frequency dependent noise factor $F(f)$ can be written as

$$F(f) = F_c + (F_c - 1 + \frac{\gamma g_{d0}}{g_m})\left(\frac{f}{f_0}\right)^2. \qquad (17)$$

F_c in Eq. (17) is the low frequency noise figure when the noise of matching device is canceled and $f_0 = 1/(\pi R_S C_{IN})$ is the input pole, where C_{IN} represents the input parasitic capacitances.

Equation (17) shows the importance of maximizing f_0 in order to mitigate the degradation of the noise factor. Gate-inductive-peaking technique employed in this paper can achieve frequency compensation by using an inductor to partly cancel the effect of the parasitic capacitances. Consequently, noise canceling deviation is reduced due to higher f_0.

However, the noise figure is not only contributed by the matching stage, the feedback resistor R_f and the voltage-sensing amplifier also produce noise that cannot be ignored. As shown in Eq. (16), their noise contribution is tightly relative to the overall gain of the whole LNA. In this paper, the signal is pre-amplified by the series RLC network by introducing the peaking inductor at the gate of the amplifier[11]. The resonant frequency of the RLC series network can be set at about 2.2 GHz. The input signal to noise ratio is consequently improved, resulting in better noise performance at high frequency, as shown in Fig. 9. An inductive-peaking technique would cause a quick roll-off gain above the resonant frequency. Hence, the noise figure will grow quickly above the resonant frequency. So the tradeoff between noise figure and noise figure bandwidth is inevitably taken into account.

4. Circuit design

The circuit diagram of the gate-inductive-peaking wideband CMOS LNA is shown in Fig. 10. The matching amplifier stage consists of transistors M1n and M1p with a large capacitor $C_1 = 12$ pF grounding the source of M1p. The matching stage is ac coupled to Msf via the high-pass filter formed by R_c and C_c. The cascode transistor M2b improves the isolation and reduces the input capacitance by decreasing the Miller effect from M2a. The bandwidth and flatness of the matching amplifier stage and voltage-sensing amplifier stage are simultaneously enhanced by the gate inductor L_g. The combining network is realized by the source follower Msf, which also acts as the output buffer to maintain output matching with its transconductance $g_{m,sf} \approx 20$ mS. The current bleeding technique is used to provide additional bias current for the cascode amplifier. So it can be tuned for high gain without increasing the DC current of the source follower Msf. Since both the matching amplifier stage and voltage-sensing amplifier stage have good gain flatness and extended bandwidth, excellent overall gain flatness and noise cancellation can be achieved.

Considering that the LNA's maximum operating frequency is higher than 2 GHz, large-area devices should be avoided for less parasitic capacitances. Increasing the current of M3 is an effective way to increase the gain of M1n and M1p while their width is relatively small. The tradeoff among power, input matching and gain is a key issue during choosing the width of the MOSFETs. In this work, the widths of M1n and M1p are chosen as 92 μm and 125 μm, respectively, to compromise the input matching and gain while consuming less than 4 mA current in the matching stage.

R_f determines the voltage gain of the matching amplifier stage and the noise voltage ratio V_Y/V_X. V_Y/V_X consequently determines the gain of voltage-sensing amplifier. In this work, an R_f of 700 Ω is exploited, expecting a noise voltage ratio $V_Y/V_X = 14$. To achieve theoretically noise cancellation, g_m of the voltage-sensing amplifier stage needs to be 280 mS, which means that the dc current consumption of M2a will be larger than 20 mA and the gate width of M2a is extremely big. To compromise power consumption, input matching and noise performance, the gate width of M2a is chosen as 210 μm, by which the noise of the matching amplifier stage is partly canceled while the expected S_{11} is below –10 dB at 2.4 GHz.

Because only one inductor is exploited in the circuit to extend the bandwidth of both stages, the inductor value should be

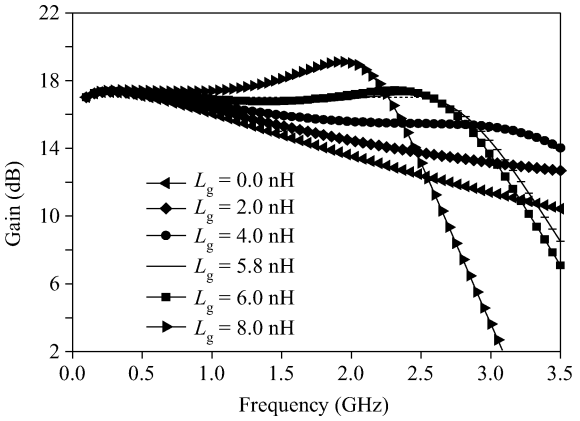

Fig. 11. Gain of the whole LNA versus different gate inductor peaked wideband LNA.

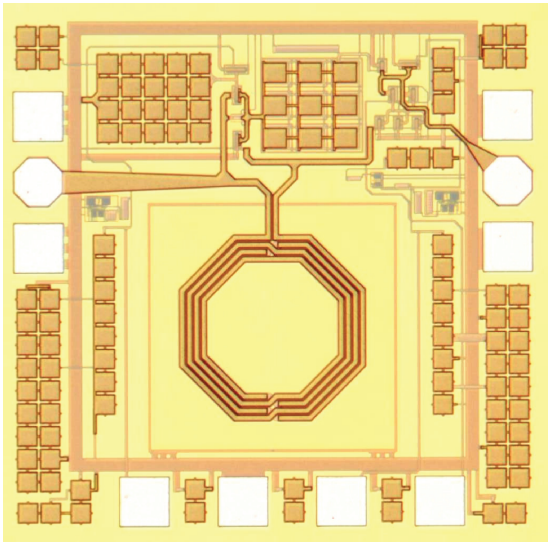

Fig. 12. Chip photograph of the fully-integrated wideband LNA.

carefully selected to guarantee that the gain of whole LNA is flat and stable. In addition, a passive spiral inductor inherently has parasitic resistance which may increase the noise factor of the LNA. The inductor value affects both the bandwidth and the stability of the LNA, as shown in Fig. 11. In this work, considering the tradeoff between bandwidth and stability, an inductor of 5.8 nH is applied in the proposed circuit.

5. Measurement results

The wideband LNA with gate-inductive-peaking and noise-canceling techniques is fabricated in TSMC 0.18 μm RF CMOS technology. The chip photograph of the fully-integrated wideband LNA is shown in Fig. 12. The core chip size is 600 $\times$ 650 μm^2. On-wafer measurement is carried out by mounting the wafer on a Cascade Summit 11000 probe station. The S-parameters are measured by using an Agilent E5071B network analyzer. The noise figure is measured by using an Agilent N8975A NF analyzer. The measured dc current is 11.7 mA from a 1.8 V supply voltage.

Figure 13 shows the measured S_{11} and the post-simulated S_{11} of the proposed LNA. The measured S_{11} is below –10 dB

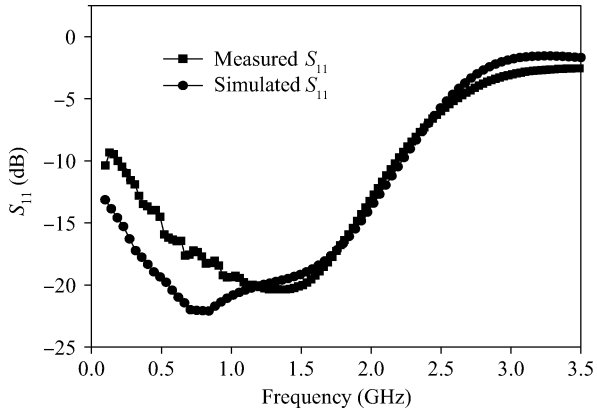

Fig. 13. Measured and post-simulated S_{11} of the proposed LNA.

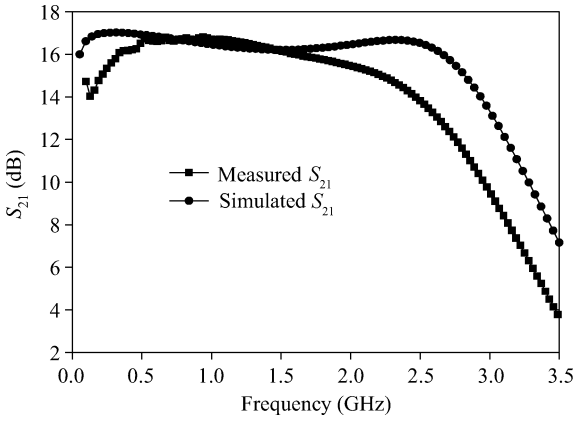

Fig. 14. Measured and post-simulated S_{21} of the proposed LNA.

from 200 MHz to 2.2 GHz and it is –7 dB at 2.4 GHz. The measured maximum power gain is 16.8 dB and the –3 dB bandwidth is 2.5 GHz as shown in Fig. 14. The effect of the gate-inductive-peaking technique is verified by the extended flat gain bandwidth of the LNA. The measurement data corresponds to the post-simulation result quite well. Nevertheless, parasitic capacitance still degrade the power gain at high frequency to some extent.

The output match and reverse isolation characteristics are presented in Fig. 15. The measured S_{22} is less than -8.5 dB above 500 MHz. The measured S_{12} is below -28 dB above 700 MHz, which also satisfies the system requirements.

Figure 16 presents both the post-simulated and the measured NF. The measured NF has a minimum value of 3.4 dB. The difference between the two curves is caused by the inaccuracy of the noise modeling, the drops in gain and the parasitic resistors of the inductor. Moreover, it is believed that the non-ideal experimental environment also introduces extra noise which can degrade noise performance. The ripples in the measured NF curve at low frequency could be caused by the interference from the non-ideal experimental environment.

The two-tone measurement is performed to characterize the input 3rd order intercept point (IIP3). The space of the two tones is 1 MHz. As shown in Fig. 17, the measured IIP3 ranges from -2.8 to -1.3 dBm within 0.5–2.5 GHz. And the average IIP3 is about –2 dBm.

The measured performance of the proposed LNA and other

Table 1. Summary and performance comparison.

Reference	Technology	Frequency (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	VD (V)	PD (mW)	Chip area[a] (mm^2)
Ref. [4]	0.25 μm CMOS	0.002–1.6	13.7[b]	2.0–2.4	0	2.5	35	0.075
Ref. [5]	0.18 μm CMOS	0.05–0.86	13.5–16[c]	< 4.5	–0.4	1.8	10.8	0.04
Ref. [12]	0.18 μm CMOS	0.2–1.46	12.1[c]	3.0–4.9	0	1.8	18	0.034
Ref. [13]	0.18 μm CMOS	0.47–0.87	–17 to 16[b]	4.3	–1.5	1.8	22	0.32
Ref. [14]	0.18 μm CMOS	0.05–0.86	–16 to 15[b]	4.2	2.6	1.8	10	0.29
This work	0.18 μm CMOS	0.2–2.5	16[c]	3.4	–2	1.8	21	0.39

[a] The pads are not included. [b] Voltage gain. [c] Power gain.

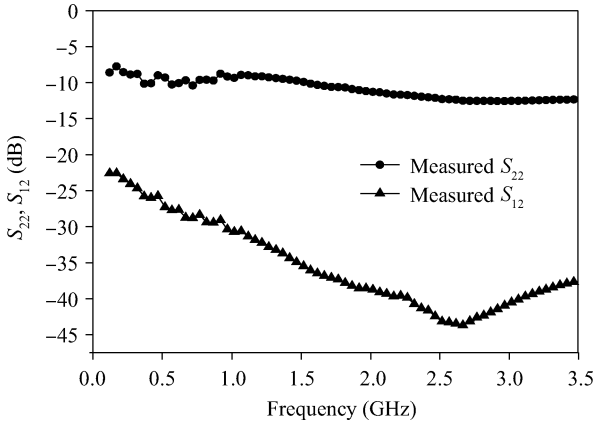

Fig. 15. Measured S_{22} and S_{12} of the proposed LNA.

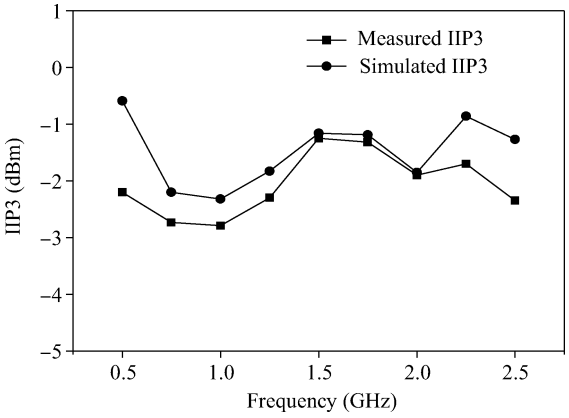

Fig. 17. Measured and post-simulated IIP3 of the proposed LNA.

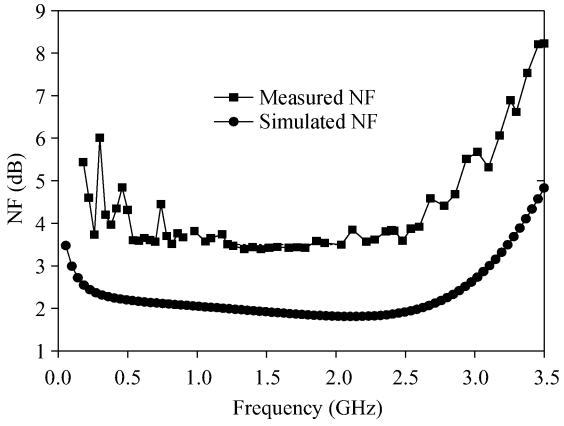

Fig. 16. Measured and post-simulated noise figure of the proposed LNA.

recently published wideband CMOS LNAs are summarized in Table 1. By adding an inductor at the gate of the input transistor, the –3 dB bandwidth of the LNA is extended to 2.5 GHz at the cost of a slightly increased area. Meanwhile, the LNA maintains a moderate power consumption and a low noise figure across the operating frequency band. The width and flatness of gain bandwidth has a great significance for wideband receiver design, especially for SDR receivers.

6. Conclusions

This paper presents a wideband LNA for multi-standard applications including GSM, WCDMA, GPS, Galileo, WLAN, etc. Gate-inductive-peaking and noise-canceling techniques are analyzed in depth. To verify the analysis, a 0.18 μm CMOS wideband LNA is designed and fabricated. The designed LNA's measured –3 dB bandwidth is 2.5 GHz and the gain variation is $\pm$0.8 dB from 300 MHz to 2.2 GHz. It achieves 3.4 dB of noise figure, 16 dB of gain and –2 dBm of average IIP3. Operating at 1.8 V, the LNA drains a current of 11.7 mA. The characteristics of wide bandwidth, low noise, moderate power consumption and moderate area consumption make this implementation a suitable alternative for multi-band, multi-standard radio applications.

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