A wide-band low phase noise LC-tuned VCO with constant K_{VCO}/ω_{osc} for LTE PLL

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Abstract: A wideband LC-tuned voltage-controlled oscillator (LC-VCO) applied in LTE PLL frequency synthesizers with constant K_{VCO}/ω_{osc} is described. In order to minimize the loop bandwidth variations of PLL, a varactor array is proposed, which consists of a series of differential variable capacitor pairs and a series of single-pole double-throw (SPDT) switches to connect V_{tune} or V_{DD}. The switches are controlled by switching bits. With this scheme, the ratio of $K_V = \partial C_{var}/\partial V_{tune}$ and the capacitance value of the capacitor array maintains relatively constant; furthermore, the loop bandwidth of the PLL fluctuation is suppressed. The 3.2–4.6-GHz VCO for multi-band LTE PLL is fabricated in a 0.13-μm RF-CMOS process. The VCO exhibits a maximum variation of K_{VCO}/ω_{osc} of only ±4%. The VCO also exhibits a low phase-noise of –124 dBc/Hz at a 1-MHz offset frequency and a low current consumption of 18.0 mA with a 1.2-V power supply.

Key words: voltage-controlled oscillator; loop bandwidth; LTE; K_{VCO}; low phase noise
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1. Introduction

The growing demand on high data rates in wireless communication systems has arisen in order to support broadband services. The long-term evolution (LTE) of UMTSs (Universal Mobile Telecommunications Systems) toward high-speed mobile broadband while preserving voice services is an evolution to existing 3rd-generation technologies in order to meet customer needs over the next decades. For a cost-effective LTE RFIC that supports broadband and multi-band applications, a single voltage-controlled oscillator (VCO) generating a local oscillator (LO) signal, which has a wide tuning range and a low phase noise at a low power, is an essential component.

Owing to their superior phase noise performance, LC-VCOs are employed in almost all phase locked loop (PLL) frequency synthesizers. The PLL bandwidth is an important design parameter, because it affects most of the PLL parameters including phase noise, settling time, etc. However, the PLL bandwidth varies significantly with the operating frequency due to the variation in the VCO gain, K_{VCO}, which fluctuates widely in the oscillation frequency range of the VCOs. Thus, a low tuning sensitivity along with a wide frequency range is important when designing VCOs. There are several ways to achieve a wide tuning range and a low tuning sensitivity at the same time[1−6].

In this paper, a technique is proposed that can make tuning sensitivity relatively low and maintain a wide frequency range. The LC-VCO PLL dynamics is discussed. A new VCO realization is reported.

2. Analysis of LC-VCO PLL dynamics

Figure 1 shows a simplified 3rd-order LC-VCO based charge-pump PLL.

According to Ref. [7], $\omega_{-3dB}/\omega_{ref}$ can be written as

$$\frac{\omega_{-3dB}}{\omega_{ref}} \approx \frac{I_{CP}}{2\pi} R_2 \frac{K_{VCO}}{\omega_{osc}}, \tag{1}$$

where I_{CP} is the charge-pump (CP) current, R_2 is the loop filter resistor, ω_{-3dB}, ω_{osc} and ω_{ref} are the closed-loop bandwidth, the operating frequency, and the reference frequency, respectively. To compensate for the variation of K_{VCO}/ω_{osc}, a servo loop[8] can be used to set the charge pump current I_{CP} to be inversely proportional to the square of the oscillation frequency. But this paper focuses on suppressing the K_{VCO} variations with frequency.

In a varactor tuned LC-VCO, the VCO gain K_{VCO} can be written as

$$K_{VCO} = \frac{\partial \omega_{osc}}{\partial V_{tune}} = \frac{\partial \omega_{osc}}{\partial C_{var}} \frac{\partial C_{var}}{\partial V_{tune}}, \tag{2}$$

where V_{tune} and C_{var} are the VCO control voltage and the effective capacitance of the controlled varactors, respectively. The

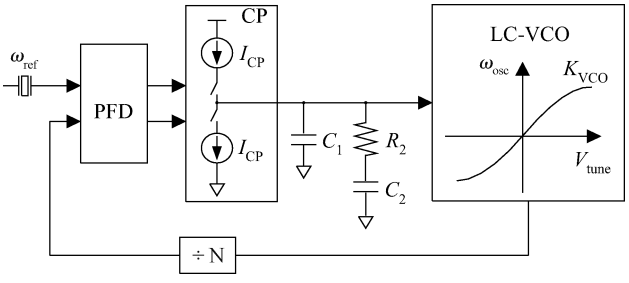

Fig. 1. Simplified schematic of a third-order LC-VCO based charge-pump PLL.

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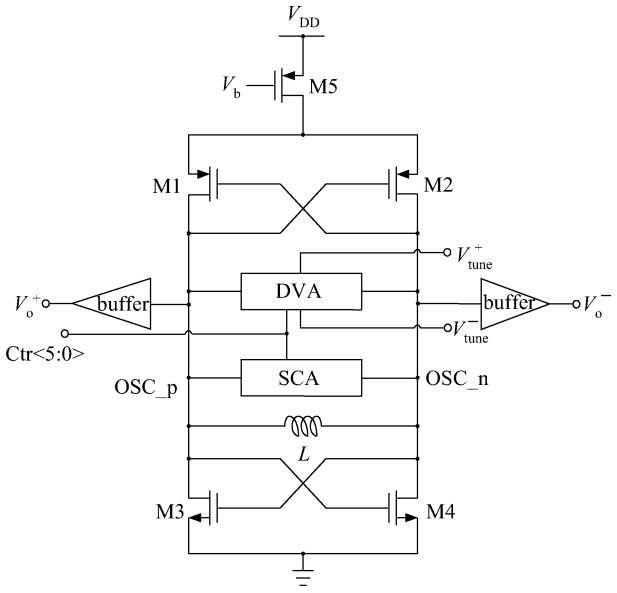

Fig. 2. Simplified VCO circuit schematic with a discrete switched tuning.

VCO operating frequency $\omega_{\rm osc}$ is given by

$$\omega_{\rm osc} = \frac{1}{\sqrt{L\left(C_{\rm fix} + C_{\rm var}\right)}} = \frac{1}{\sqrt{LC}}, \tag{3}$$

where L is the tank inductance, and $C_{\rm fix}$ is the tank capacitance excluding the varactors capacitance $C_{\rm var}$, and $C = C_{\rm fix} + C_{\rm var}$. From this relation, $\partial\omega_{\rm osc}/\partial C = -\omega_{\rm osc}/2C$ is obtained. Hence, from Eq. (2), the VCO gain $K_{\rm VCO}$ can be found to be

$$K_{\rm VCO} = -\frac{1}{2}\frac{\omega_{\rm osc}}{C}K_{\rm V}, \tag{4}$$

$$\frac{K_{\rm VCO}}{\omega_{\rm osc}} = -\frac{1}{2}\frac{K_{\rm V}}{C}, \tag{5}$$

where $K_{\rm V} = \partial C_{\rm var}/\partial V_{\rm tune}$ is the voltage sensitivity of the varactor which is related to the varactor's linearity. Combining Eq. (1) and Eq. (5) yields

$$\left|\frac{\omega_{-3\rm dB}}{\omega_{\rm ref}}\right| \approx \frac{I_{\rm CP}}{4\pi}R_2\frac{K_{\rm V}}{C}. \tag{6}$$

This equation illustrates that, in an LC-VCO PLL, the bandwidth is a function of $K_{\rm V}$. Equation (6) indicates that making $K_{\rm V}/C$ constant would maintain a constant loop width over the entire PLL tuning range.

3. VCO circuit realization

The proposed schematic diagram of the differential tuned wide-band VCO is depicted in Fig. 2. The cross-coupled NMOS and PMOS transistor pairs M1–M4 in positive feedback generate a negative resistance which compensate for the tank's resistive loss. Transistor M5 provides bias current. The LC tank consists of a 6-bit digitally controlled switched metal-insulator-metal (MIM) capacitor array (SCA), a differential varactor array (DVA), and a spiral inductor.

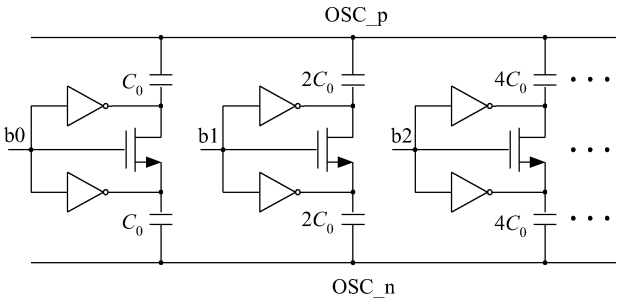

Fig. 3. Circuit schematic of the differential SCA.

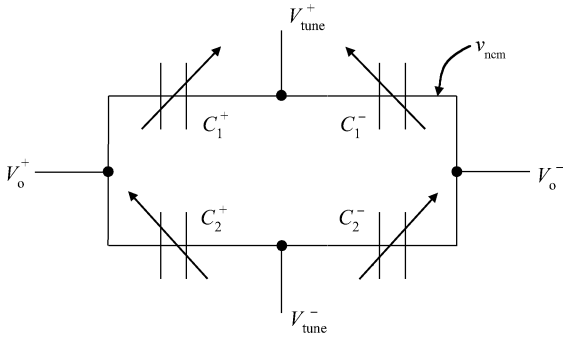

Fig. 4. Differentially tuning varactor circuits.

3.1. Differential SCA and differential varactor

In order to achieve a wide tuning range for the VCO, both discrete and continuous tuning is employed. This approach increases the tuning range, while ensuring a low sensitivity to noise on the tuning path. As for a discrete tuning configuration, the differential switched capacitor array[9, 10], depicted in Fig. 3, is implemented for coarse tuning. The targeted frequency range is spitted into 64 sub-bands by means of a 6-bit binary-weighted array of switched MIM capacitors. The capacitors are switched in and out of the tank by digitally controlled switches. In order to minimize the phase noise due to the switched capacitor array, two minimal dimension inverters are added to the source and drain, respectively, of the switching NMOS transistor to provide a dc reference point without adding significant parasitic capacitance to those nodes. Each switch contributes additional loss to the tank due to its finite resistance. Thus, NMOS devices of minimum gate-length are utilized and made as wide as can be tolerated with regards to the resulting parasitic drain-to-bulk capacitance, which ultimately limits the achievable tuning range.

Fine tuning capacitance is realized by an accumulation-mode MOS (AMOS) varactor configuration[11, 12], as shown in Fig. 4.

The differential structure is employed to minimize low frequency common-mode noise on either the control line or $V_{\rm DD}$ that affects the capacitance of the varactors and is evident as phase noise on the VCO output. For differentially tuned varactors, the capacitance between $V^+_{\rm tune}$ and $V^+_{\rm o}$ can be written as

$$C_1^+ = C_0 + k_{\rm v1}\left(V^+_{\rm tune} + v_{\rm ncm}\right). \tag{7}$$

And the capacitance between $V^-_{\rm tune}$ and $V^+_{\rm o}$ can be written as

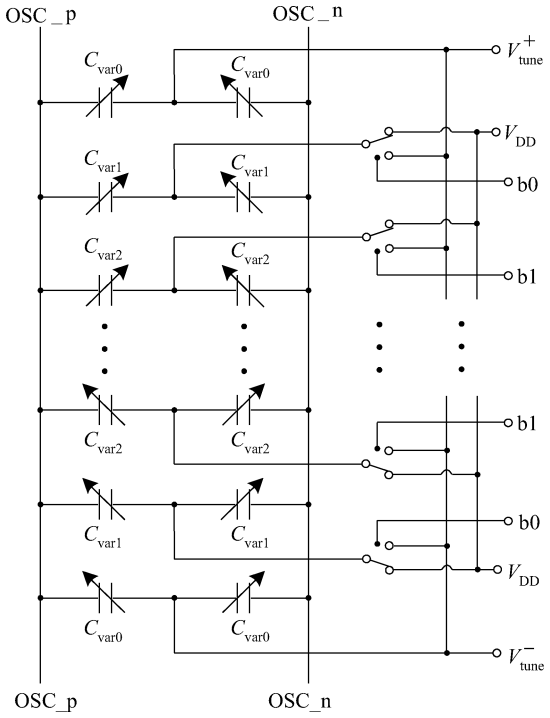

Fig. 5. The proposed varactor array.

$$C_2^+ = C_0 - k_{v2}\left(V_{tune}^- + v_{ncm}\right), \tag{8}$$

where C_0 is the zero bias capacitance, k_{v1} and k_{v2} is the varactor sensitivity, V_{tune} is the varactor control voltage, and v_{ncm} is the common mode noise voltage injected. The total capacitance between the middle node of this structure and V_o^+ is $C_{var} = C_1^+ + C_2^+$; if the varactor is perfectly symmetrical ($k_{v1} = -k_{v2}$) the expression for the capacitance is

$$C_{var} = 2C_0 + 2k_v V_{tune}, \tag{9}$$

where $V_{tune} = V_{tune}^+ - V_{tune}^-$ and the common mode noise on controlled line and power supply is rejected. If $|k_{v1}| \neq |k_{v2}|$ the gain of the common mode noise is $|k_{v1}| - |k_{v2}|$. Even in this case, common mode noise will be effectively reduced because $|k_{v1}| - |k_{v2}|$ is smaller than $|k_{v1}|$ and $|k_{v2}|$.

3.2. Suppression technique of the variation of the closed-loop bandwidth

As above discussed, the closed-loop bandwidth of a PLL-based frequency synthesizer is proportional to K_V/C. For a wideband VCO design based on a switched capacitor array, the lower the operating frequency, the more C varies and the wider the closed-loop bandwidth will vary because the K_v ($\partial C_{var}/\partial V_{tune}$) of the conventional fine tuning structure varies little. To suppress the variation of the closed-loop bandwidth, the differential tuning MOS varactor array shown in Fig. 5 is proposed. It consists of MOS varactor pairs with differential connection ways and single pole double throw (SPDT) switches connecting V_{tune} or V_{DD}. The switches are controlled by controlled bits (Ctr<5:1>). When bit voltage is high, the varactor is connected to V_{tune}, and when bit voltage is low, the varactor is connected to V_{DD} and sets the minimum capacitance. In other words, controlled bits not only connect the switched capacitor array, but also connect a series of varactors, excluding the lowest controlled bit (Ctrl<0>).

When the capacitance in a switched capacitor array varies with controlled bits (Ctr<5:0>), C_{var} must be changed correspondingly.

Ctr<5:0> is adjusted →

$$\left\{\begin{array}{l} \xrightarrow{\text{when Ctr<5:1>}\uparrow} C\uparrow \text{ and } K_V = \partial C_{var}/\partial V_{tune}\uparrow \\ \xrightarrow{\text{when Ctr<5:1>}\downarrow} C\downarrow \text{ and } K_V = \partial C_{var}/\partial V_{tune}\downarrow \end{array}\right\}$$

$$\rightarrow K_V/C \text{ maintain constant} \tag{10}$$

where C_{var} is an NMOS varactor. Therefore, careful selection of the C_{var} array makes K_V/C ($C = C_{fix} + C_{var}$) remain constant when C varies with controlled bits. As a result, the closed-loop bandwidth of this frequency synthesizer based on PLL, which adopts this VCO design, remains relatively constant over the entire frequency synthesizer tuning range.

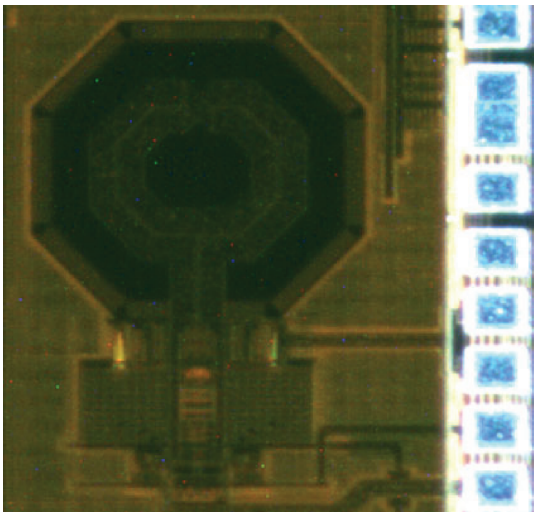

Fig. 6. Chip photo of proposed VCO.

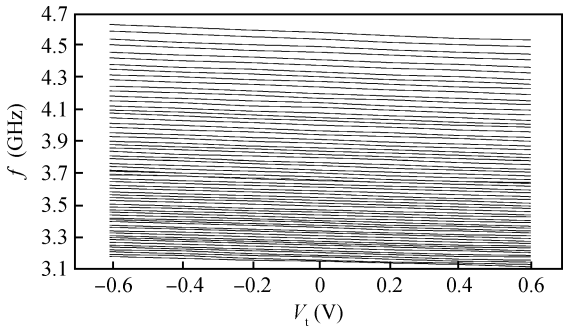

Fig. 7. Measured tuning characteristics of VCO.

4. VCO measurement results

The VCO has been designed based on a TSMC 130-nm RF CMOS process. Figure 6 shows a chip photograph of the proposed VCO. The chip occupies an area of 500 × 600 μm^2. The layout has been arranged as symmetrically as possible. All

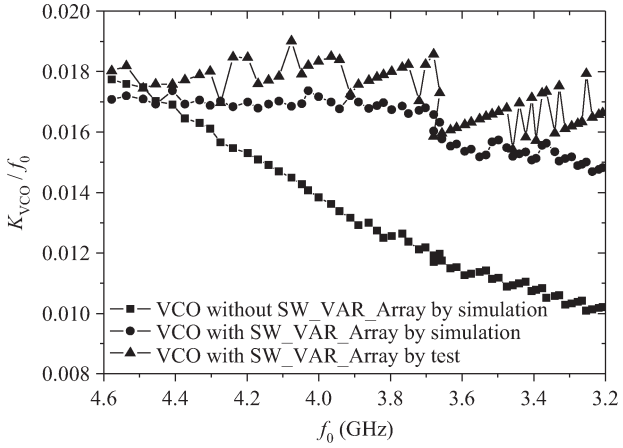

Fig. 8. Measured VCO K_{VCO}/f_0 against operating frequency.

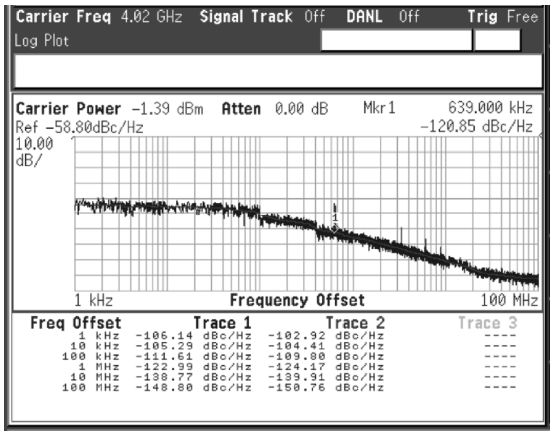

Fig. 9. Measured phase noise of the VCO.

Table 1. Wide-band VCO comparison.

Reference	Frequency (GHz)	Power (mW)	K_{VCO} variation(MHz/V)	Phase noise (dBc/Hz)	Technology
Ref. [1]	3.1–4.15	36.75	29 ± 2.5%	–115 @ 400 kHz –156 @ 20 MHz	0.13 μm CMOS
Ref. [2]	3.21–4.02	44	±14%	–165.1 @ 20 MHz	0.13 μm CMOS
Ref. [3]	4.2–5.03	6	±11 (8–10)	–120 @ 1 MHz	0.18 μm CMOS
This work	3.2–4.6	21.6	±14% (58–78)*	–124 @ 1 MHz	0.13 μm CMOS

*K_{VCO}/ω_{osc} variation is ±4%.

capacitors and transistors are placed nearby, so energy loss due to connection wires is reduced.

The VCO chip was packaged, and the characteristics of the proposed VCO are obtained by on-board measurements. Figure 7 shows the measured f_{osc} dependence on differential control voltage (V_{tune}). A wide tuning range is achieved with differential control voltage adjusted from –0.6 to 0.6 V. The fabricated VCO exhibited 64 overlapping frequency sub bands by setting the capacitance of the switched capacitor arrays. The measured frequency range is 3.2–4.6 GHz and covers most of the frequency ranges of the LTE transceiver. Figure 8 shows the curve of the K_{VCO}/f_0 of the VCO against operating frequency. The measurement results and the simulation results of the VCO with a switched VCA , and the simulation results of the VCO without a switched VCA are shown in the figure, respectively. From these curves, the great improvement of K_{VCO}/f_0 instability is exhibited. The proposed VCO exhibits a maximum variation of K_{VCO}/ω_{osc} of only ±4%.

Figure 9 shows the measured phase noise versus the offset from the oscillation frequency. It exhibits a pretty low phase noise at the operating frequency.

The single supply voltage is 1.2 V. The maximum tail current is 18.0 mA. The performance of the proposed VCO is listed in Table 1 with those of recently reported wide-band VCOs.

5. Conclusions

The developed 3.2–4.6 GHz VCO demonstrated K_{VCO}/ω_{osc} fluctuation of ±4% with a wide tuning range of 1400 MHz and low phase noise of –124 dBc/Hz at a1-MHz offset frequency. Since the proposed VCO can suppress the loop bandwidth fluctuation while maintaining a wide tuning range and low phase noise, and without additional bias current, it is well suited for multi-band and multi-mode wireless communication systems such as LTE or WiMAX.

References

[1] Lin T Y, Yu T Y, Ke LW, et al. A low-noise VCO with a constant K_{vco} for GSM/GPRS/EDGE applications. IEEE Radio Frequency Integrated Circuits Symposium, 2008: 387

[2] Samadian S. A low phase noise quad-band CMOS VCO with minimized gain variation for GSM/GPRS/EDGE. International Symposium on Circuits and Systems, 2007: 3287

[3] Xu Conghui, Xi Jingtian, Lu Lei, et al. A 4.2–5 GHz, low phase noise LC-VCO with constant bandwidth and small tuning gain. Journal of Semiconductors, 2009, 30(9): 095002

[4] Broussev S S, Lehtonen T A, Tchamov N T. A wideband low phase-noise LC-VCO with programmable KVCO. Microwave and Wireless Components Letters, 2007, 17(4): 274

[5] Nakamura T, Masuda T, Shiramizu N, et al. A wide-tuning-range VCO with small VCO-gain fluctuation for multi-band W-CDMA RFIC. Proceedings of the 32nd European Solid-State Circuits Conference, ESSCIRC, Montreux, 2006: 448

[6] Kim J, Shin J, Kim S, et al. A wide-band CMOS LC VCO with linearized coarse tuning characteristics. IEEE Trans Circuits Syst II: Express Briefs, 2008, 55(5): 399

[7] Loke A, Barnes R, Wee T, et al. A versatile 90-nm CMOS charge-pump PLL for SerDes transmitter clocking. IEEE J Solid-State Circuits, 2006, 41(8): 1894

[8] Wu T, Hanumolu P K, Mayaram K, et al. Method for a constant loop bandwidth in LC-VCO PLL frequency synthesizers. IEEE J Solid-State Circuits. 2009, 44(2): 427

[9] Fard A. Phase noise and amplitude issues of a wide-band VCO utilizing a switched tuning resonator. IEEE International Sympo-

sium on Circuits and Systems, 2005, (3): 2691
[10] Kral A, Behbahani F, Abidi A A. RF-CMOS oscillators with switched tuning. Proceedings of the IEEE Custom Integrated Circuits Conference, Santa Clara, 1998: 555
[11] Moon H, Kang S, Kim Y T, et al. A fully differential LC-VCO using a new varactor control structure. IEEE Microwave Wireless Compon Lett, 2004, 14(9): 410
[12] Carr J P, Frank B M. A 38 GHz accumulation MOS differentially tuned VCO design in 0.18 μm CMOS. Silicon Monolithic Integrated Circuits in RF Systems, San Diego, CA, 2006: 170