Capacitance–voltage analysis of a high-k dielectric on silicon

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Abstract: Device characteristics of TiO_2 gate dielectrics deposited by a sol–gel method and DC sputtering method on a P-type silicon wafer are reported. Metal–oxide–semiconductor capacitors with Al as the top electrode were fabricated to study the electrical properties of TiO_2 films. The films were physically characterized by using X-ray diffraction, a capacitor voltage measurement, scanning electron microscopy, and by spectroscopy ellipsometry. The XRD and DST-TG indicate the presence of an anatase TiO_2 phase in the film. Films deposited at higher temperatures showed better crystallinity. The dielectric constant calculated using the capacitance voltage measurement was found to be 18 and 73 for sputtering and sol–gel samples respectively. The refractive indices of the films were found to be 2.16 for sputtering and 2.42 for sol–gel samples.

Key words: sol–gel method; DC reactive sputtering; C–V analysis; flat band voltage
DOI: 10.1088/1674-4926/33/2/022001 **EEACC:** 2520

1. Introduction

Progress in the complexity of CMOS circuits has been achieved in the last decade by scaling the geometric dimensions of the metal–oxide–semiconductor field-effect transistor (MOSFET)[1−3]. Rapid scaling down of the transistor forced the decrease of the gate dielectric thickness and the channel length, which resulted in a drastic increase in leakage current due to direct tunneling[3]. Another problem with the ultra thin SiO_2 dielectric layer is when p^+ polysilicon is used as the gate contact in P-MOSFET, which changes the threshold voltage due to a low barrier against boron diffusion[4,5]. The SiO_2 gate dielectric may be replaced with a high-k material to remove that problem. In the search for a high-k material, extensive studies have been carried out on several metal oxides, such as such as Al_2O_3[6], ZrO_2[7], HfO_2[8], Ta_2O_5[9], TiO_2[2, 10−12], La_2O_2[13], Gd_2O_2[14]. In this paper, titanium dioxide (TiO_2) is chosen as an alternative to a silicon dioxide (SiO_2) gate dielectric. TiO_2 is a very well known and well researched material due to its chemical stability in hostile environments and its optical and electrical properties[15]. It is a wide band gap semiconductor and has potential applications in catalysis[16, 17], sensors[18], the photodecomposition of water[19, 20], photo catalysis and in antireflection coatings[21, 22]. TiO_2 thin films have been successfully used in sustainable energy sources because of its high incident photon to electron conversion efficiencies[2, 23, 24]. So in this experiment, MOS capacitors were fabricated using TiO_2 as the dielectric material on P-type silicon wafers and characterized for microelectronics applications.

The band gap of this material was calculated as 3.6 eV, its dielectric constant can be varied from 18 to 110 depending upon the growth process[25]. Many techniques have been employed to deposit TiO_2 thin films by MOCVD[26], ion assisted deposition[27] and sputtering[28]. In this work we have opted for the sol–gel spin coating method and the DC reactive magnetron sputtering method to deposit the thin TiO_2 films. The deposited samples were characterized using X-ray diffraction, scanning electron microscopy (SEM), and capacitance voltage measurements.

2. Experimental procedure

Two sets of PMOS capacitors were fabricated on p-type (100) oriented silicon wafers with resistivity in the 1–10 Ω·cm range. The silicon substrates were chemically cleaned by a standard RCA procedure and subsequent etching in a diluted HF solution to remove insoluble metallic and organic contaminants.

2.1. Film preparation

Titanium isopropoxide (TIP) was used as the titian precursor. The solution was prepared by the hydrolysis and condensation of $Ti(OC_3H_7O_2)_4$ in C_2H_5OH in the presence of HCl in a molar ratio of 1 : 8 : 0.1. In order to control the reaction kinetics, acetic acid was used as the chemical additive to moderate the reaction rate. The water used for hydrolysis in solution was added gradually under magnetic stirring. The molar ratio of the reactants was 1 mol of TIP $Ti(i\text{-}C_3H_7O_2)_4$ of 99.9% purity is mixed with 8 mol of ethanol absolute grade. TIP was hydrolyzed by a slow addition of cold water and 0.1 mol of acetic acid was added to catalyze the hydrolysis. The final mixture was maintained under magnetic agitation at 85 ℃ for 45 min. To obtain the film, the substrate was placed on a spinner (home-made) and drops of the above mentioned solution were placed on the substrate. The substrate was then allowed to spin for 1 min at a spinning rate of 2000 rpm. The sample was removed from the spinner and baked for 20 min at 95 ℃. Successive spin coating cycles (sol–gel deposition plus heat treatment) of the substrate were carried out in the sol-mixture.

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Received 7 July 2011, revised manuscript received 22 August 2011

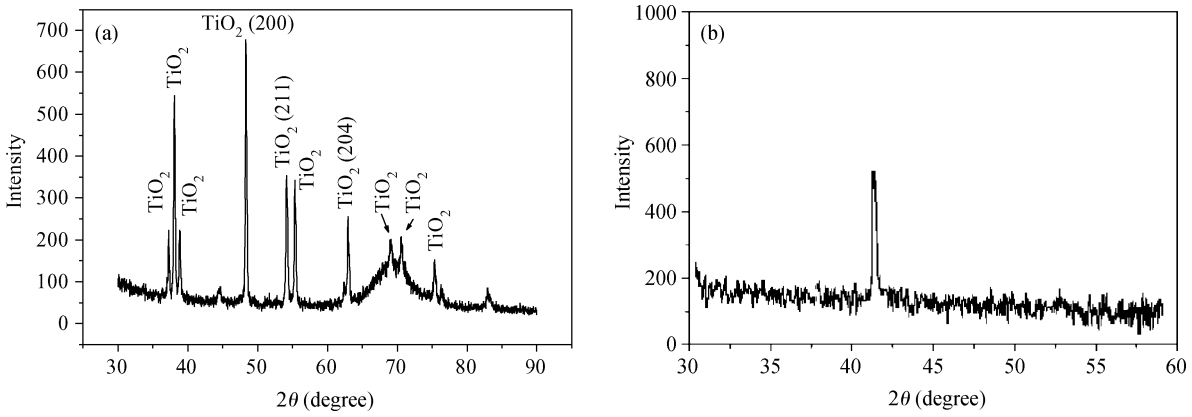
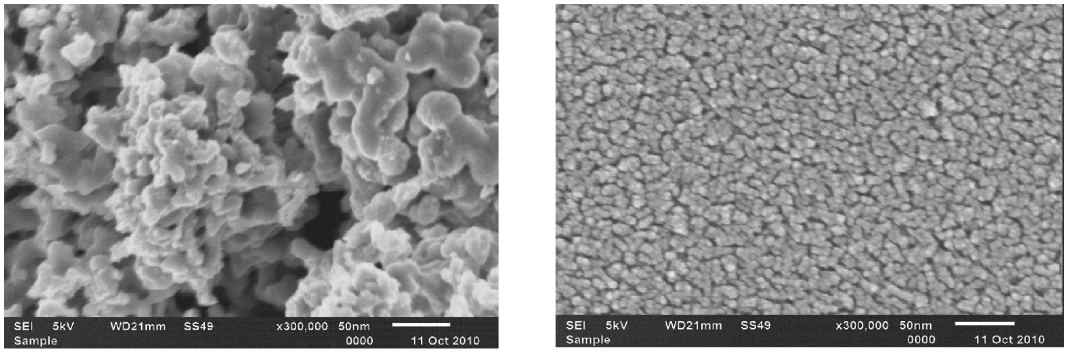


Fig. 1. XRD pattern of a TiO_2 film deposited on silicon wafer. (a) Annealed at 550 ℃ in air (sol–gel method). (b) 100 W target power (DC sputtering method).



(a) (b)

Fig. 2. SEM images of TiO_2 samples annealed at 550 ℃. (a) Deposited TiO_2 sol–gel. (b) Deposition rate: 2.0 nm/min (sputtering).

After each spin coating cycle, the film was annealed in dynamic air at 550 ℃ for 30 min. While in the DC reactive magnetron sputtering, Ar (60%) and O_2 (40%) with 99.9 purity were used as sputtering and reactive gas respectively. A rotary and diffusion pump combination was used to get the desired vacuum. After attaining the base pressure, the oxygen partial pressure was set at 10^{-3} mbar. Later on, the argon was let in and the sputtering pressure was maintained. Before each run the target was pre-sputtered in an Ar atmosphere for 5–10 min in order to remove the surface oxide layers of the target. All the samples were deposited at a pressure of 1×10^{-3} mbar.

2.2. Measurement

The thickness of the deposited film was measured by a stylus profilometer. The refractive index of the films was found to be 2.16 and 2.42 by ellipsometry. The grain size as well as crystalline phase of TiO_2 has been determined using an X-ray diffractometer. The target consisted of copper metal where ac nickel metal is used as a β-filter. To determine various peaks obtained in the XRD spectrum, Joint Committee powder Diffraction Standards (JCDPS) files were used. The $C-V$ (capacitance–voltage) curve was obtained using $C-V$ analyzer (Keithley 590). Capacitance curves were measured from -5 to $+5$ V. SEM micrographs were obtained using a JEM-1200 Ex (JEOL) model. The accelerating voltage was kept at 5 kV and tube current was 10 mA. The aluminum (Al) metal was deposited by the thermal evaporation system on the back side of the sample for the ohmic contact. A physical mask was used to make dots on the front side of the TiO_2 film. Before the deposition of dots, samples were annealed in vacuum at 300 ℃ for good ohmic contact.

3. Results

3.1. Thickness, composition and structure

The thickness of the film was found to be 39 nm and 43 nm by the stylus profilometer for sol–gel and sputtering method respectively. Figure 1(a) shows the XRD pattern of TiO_2 thin films deposited by the sol–gel method on silicon wafers and annealed at 550 ℃. XRD exhibits the different crystalline phases of the TiO_2 thin film and the grain size was calculated by Scherer's formula $D = 0.89\lambda/\beta_{1/2}\cos\theta$, where λ is the X-ray wavelength, $\beta_{1/2}$ is full width at half maximum (FWHM) of the diffraction lines and θ is the diffraction angle. XRD exhibits the different crystalline phases of the TiO_2 thin film and the calculated grain size of TiO_2 (004), (200) and (211) phases are 38, 47, and 65 nm respectively. Better crystallinity was determined at higher deposition rates of the sputtering method shown in Fig. 1(b). The two dimensional SEM images of the TiO_2 film of thickness 39 nm and 43 nm were shown in Fig. 2. The surface morphology of the TiO_2 films was investigated by FESEM (using JEOL-JM-6510). Its porous nature is clearly

Table 1. Calculated parameters with the help of C–V curves.

Deposition method	Flat band voltage (V)	Threshold voltage (V)	Dielectric constant (K)	Interface trap charge density D_{it} ($cm^{-2}{\cdot}eV^{-1}$)	Oxide charge density Q_{it} (cm^{-2})
Sol–gel spin coating	−1.34	−2.28	73	4.32×10^{13}	7.48×10^{12}
DC reactive sputtering	−0.53	−1.8	18	7.4×10^{12}	1×10^{12}

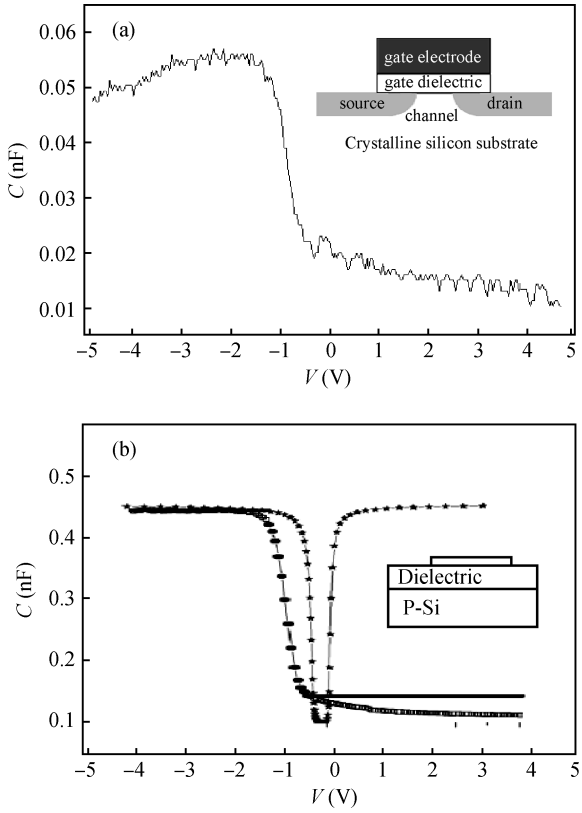


Fig. 3. C–V characteristics of MOS capacitors of structure Si/TiO_2/Al at room temperature. (a) Sol–gel (39 nm). (b) DC reactive sputtering (43 nm).

visible. The refractive index of the TiO_2 film as measured by spectroscopic ellipsometry was found to be 2.43 for the Sol-Gel sample and 2.31 for the sputtered samples.

3.2. Electrical analysis

MOS capacitors were fabricated for the electrical evaluation of the TiO_2 films. Al top contacts were deposited using a shadow mask by vacuum evaporation with a contact area of 3.14×10^{-4} cm^2 for capacitance–voltage measurement and leakage current–voltage measurement.

3.3. Capacitance–voltage analysis

The variation of the capacitance (C) with gate voltage (V_G) ranging from −5.0 to +5.0 V with frequency of 10 kHz was obtained using a Keithley 590CV analyzer as shown in Figs. 3(a) and 3(b). The oxide capacitance (C_{ox}) is the high frequency capacitance when the device is biased for strong accumulation as shown in Fig. 3(a) with the sol–gel method and found to be 55 μF, while it was 440 pF for the DC reactive sputtering method as shown in Fig. 3(b).

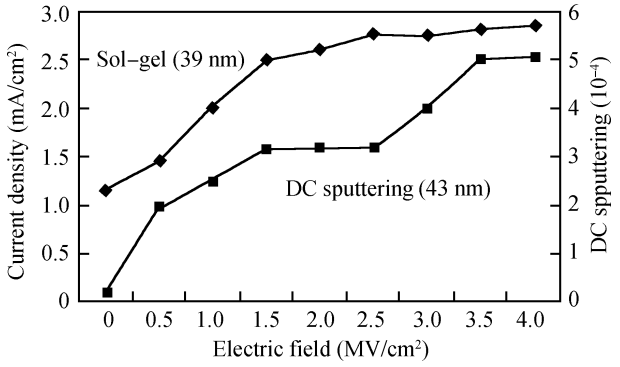


Fig. 4. Gate leakage current versus electric field for sol–gel (39 nm) and DC sputtering sample (43 nm).

By comparing the C–V characteristics of the capacitor with the ideal simulated C–V curves, the flat band voltage of the capacitors is calculated by $C_{FB} = \frac{C_{ox}\varepsilon_s A/(1\times10^{-4}\lambda)}{(1\times10^{-12}C_{ox})+\varepsilon_s A}/(1 \times 10^{-4}\lambda)$, where λ is the extrinsic Debye length, as calculated by $\lambda = \sqrt{\frac{\varepsilon_s kT}{q^2 N_x}}$. Here kT is the thermal energy at room temperature. The calculated values are shown in Table 1. The dielectric constant (K) 73 was observed for the sol–gel sample by calculation using capacitance (C_{ox}), film thickness (d), the free space charge permittivity (C_o) and the area of the capacitor (A) using the relationship $K = C_d/C_o A$.

The oxide charge density (shown in Table 1) of the capacitor was calculated by $Q_i = C_{ox}(W_{MS} - V_{FB})/A$ where C_{ox}, W_{MS}, and V_{FB} are oxide capacitance, metal semiconductor work function difference, and flat band voltage. The value of the oxide charge density for structure Si/TiO_2/Al (sol–gel sample) was calculated as (Q_{it}) 7.48×10^{12} and interface trap density (D_{it}) 4.32×10^{13} $eV^{-1}{\cdot}cm^{-2}$. The values of Q_{it} and D_{it} were slightly higher than the values reported in Ref. [19]. The gate leakage current density of the fabricated MOS capacitor (Si/TiO_2/Al) shown in Fig. 4 shows that the leakage current is higher than the value reported in the literature. A MOS capacitor was fabricated and it presented a leakage current density of 10 mA/cm^2, which is acceptable for high performance logic circuit (maximum of 100 A/cm^2) and low power circuit (10 mA/cm^2) devices[20].

4. Conclusion

In this work we have successfully fabricated MOS capacitors with a top Al electrode to study structural and electrical properties. The nanocrystalline TiO_2 thin films were deposited by sol–gel spin coating and DC reactive sputtering methods. The dielectric constant achieved was 18 for the DC sputtering sample and 73 for the sol–gel sample by CV characterization of MOS samples. The refractive index of the films was

found to be 2.16 for sputtered and 2.42 for sol–gel samples. The refractive index value was in the range reported in the literature, so the deposited film was stoichiometric in nature. It was also confirmed by XRD. The minimum leakage current density achieved is 1.54×10^{-6} A/cm^2 at a gate bias of 1 V for the magnetron sputtering method and 2.3×10^{-4} A/cm^2. So this range of leakage current may be acceptable for high performance logic circuit and low power circuit fabrication. These results indicate that TiO_2 deposited on silicon with the right recipe may be a strong candidate to substitute the current dielectric in CMOS fabrication.

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