A 0.8–3 GHz RF-VGA with 35 dB dynamic range in 0.13 μm CMOS*

Qin Xi(秦希), Huang Xingli(黄杏丽), Qin Yajie(秦亚杰), and Hong Zhiliang(洪志良)†

State Key Laboratory of ASIC and System, Fudan University, Shanghai 201203, China

Abstract: A wideband variable gain amplifier (VGA) implemented in 0.13 μm CMOS technology is presented. To optimize noise performance, an active feedback amplifier with 15 dB fixed gain is put in the front, followed by modified Cherry–Hooper amplifiers in cascade providing variable gain, which adopt dual loop feedback for bandwidth extension. Negative capacitive neutralization and capacitive source degeneration are employed for Miller effect compensation and DC offset cancellation, respectively. Measurement results show that the proposed VGA achieves a 35 dB gain tuning range with an upper 3-dB bandwidth larger than 3 GHz and the input 1 dB compression point of –29 dBm at the lowest gain state, while the minimum noise figure is 9 dB at the highest gain state. The core VGA (without test buffer) consumes 32 mW from 1.2 V power supply and occupies 0.48 mm^2 area.

Key words: RF-VGA; wideband VGA; active balun; dual loop feedback
DOI: 10.1088/1674-4926/33/1/015009 **EEACC:** 2570

1. Introduction

Recently, a growing amount of attention is being paid to wideband variable gain amplifiers (VGAs) with bandwidth extending to RF frequencies. This trend is mainly spurred on by the boom of high-speed data communication, such as optical data links[1−3] and 60 GHz wireline/wireless communication[4−6], which mandates a large bandwidth to enhance data rate. Another motivation is the vision of implementing software defined radio (SDR) architecture, where with the absence of down-sampling mixer, RF signals should be adjusted directly by an RF-VGA to accommodate the full scale range of the following A/D convertor. The emerging technique, cognitive radio (CR), also contributes to the wideband RF front-end research by its unique characteristic—sensing the environment over huge swathes of spectrum. The surveillance of the occupied spectrum imposes stringent requirements on radio sensitivity and wideband frequency agility[7].

The most challenging part in the design of a wideband RF-VGA compared to its baseband counterpart is to realize high gain at radio frequencies. A multi-stage structure can be employed to achieve higher gain. However, the stability issue encountered in high frequency circuits due to signal cross-coupling grows significant as the number of stage increases. Meticulous simulation and layout are required to guarantee the overall stability under different gain settings and various environmental conditions. Another challenge of wideband RF-VGA is the tradeoff between bandwidth and linearity. In conventional baseband VGAs, a high gain operational amplifier is utilized and the linearity is guaranteed by negative feedback. In wideband RF-VGA, open loop circuits are used to squeeze out the largest bandwidth. Consequently, nonlinearity becomes a salient issue which needs careful analysis and special treatment.

Multi-stage VGA has been widely employed in wideband applications[4, 8, 9]. However, its noise performance varies dramatically as the gain changes. Noise figure variation of nearly 50 dB has been reported in Ref. [8]. Cherry–Hooper VGAs shows superiority over other ones in wideband performance[4, 9]. Cherry–Hooper VGAs in BiCMOS technology even improve the bandwidth to 6 GHz (9–15 GHz) at the cost of 82 mW power consumption[9]. A low-threshold voltage process was used to reduce the power consumption, but the resultant bandwidth was only 2.2 GHz[4]. Moreover, its noise figure varies from 17 dB at the highest gain to 30 dB at the lowest gain.

In this work, a wideband RF-VGA for high-speed data communication applications is proposed. A fixed gain amplifier is adopted as the first stage in order to optimize the noise performance. Single-to-differential conversion is also used to employ the merit of differential signaling.

2. Architecture of the wideband RF-VGA

To improve the noise performance of the wideband RF-VGA, a pre-amplifier with 15 dB fixed gain is used as the input stage, followed by three modified variable gain Cherry–Hooper amplifiers (CH-VGA) connected in cascade, which provides variable gain from –15 to 20 dB. An f_T-doubler buffer drives the output load for measurement purpose. The block diagram of the proposed VGA architecture is shown in Fig. 1. Since a differential signal is preferred during signal transmission and processing thanks to its interference immunity characteristic, a single-to-differential conversion function is provided by the pre-amplifier. AC coupling between pre-amplifier and CH-VGA is used due to the difference of their DC operation points. Common-mode feedback (CMFB) and DC offset cancelling (DCOC) functions are included locally in each CH-VGA, which will be described in detail later.

* Project supported by the National High Technology Research and Development of China (No. 2009AA01Z261) and the State Key Laboratory of Wireless Telecommunication, Southeast University.
† Corresponding author. Email: zlhong@fudan.edu.cn
Received 9 June 2011, revised manuscript received 8 September 2011

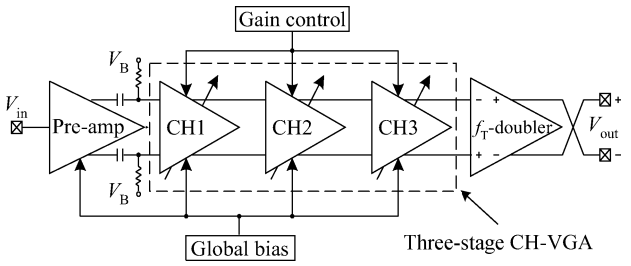

Fig. 1. Block diagram of the proposed VGA architecture.

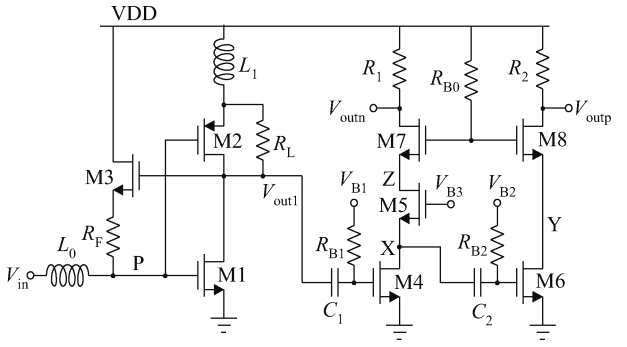

Fig. 2. Simplified schematic of the pre-amplifier.

3. Circuit implementation

3.1. Pre-amplifier

A fixed gain pre-amplifier presented at the first stage improves the overall noise performance. Active feedback and inductive peaking are employed to extent its bandwidth. The simplified schematic is shown in Fig. 2. The PMOS transistor M2 acts as another transconductor reusing the current through M1. Resistor R_L shunts part of M2's current and sets proper operating point. Inductor L_1 introduces series peaking to extent bandwidth at the drain of transistor M1 while provides source degeneration at the source of transistor M2. The tank composed of L_0–M2–L_1 boosts v_{gs2} at resonance frequency and reduces M2's noise contribution[10]. A shunt-shunt negative feedback is realized by M3 and R_F. Since a large parasitic capacitance exists at node P, this active feedback improves the frequency characteristic by reducing the input resistance at this node. When feedback is considered, this resistance is given by

$$R_P = \frac{1/g_{m3} + R_F}{1 + A_{v1}}, \tag{1}$$

where $A_{v1} = (g_{m1} + g_{m2})R_L$. The nonlinear feedback brought by M3 renders the circuit prone to linearity issue. The source degeneration resistor R_F relieves this problem by linearizing the feedback[11].

Transistors M4–M8 constitute the single-to-differential conversion circuit, which is also called the active balun. Compared to conventional circuits, the additional transistor M5 improves signal balance. To understand this, observe the circuits shown in Fig. 3. In a conventional active balun, as shown in Fig. 3(a), signals begin to divert into different branches at node X. It is obvious that the signals in branch B2 need to go through more stages than the signals in branch B1, thus an imbalance

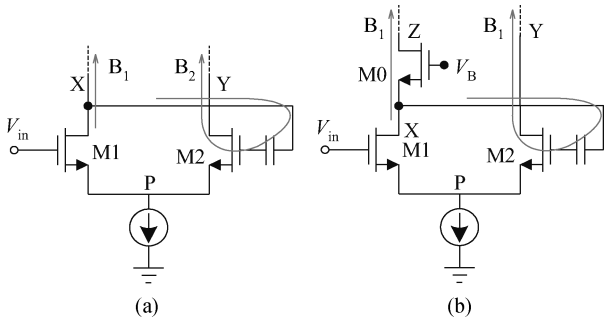

Fig. 3. Comparison of (a) conventional and (b) proposed active balun circuits.

results. To compensate this imbalance, a feedback network is used[12, 13], which may consist of area-consuming capacitors and/or inductors. The intrinsic imbalance in an active balun as shown in Fig. 3(a) can be compensated with an additional transistor M0, as shown in Fig. 3(b). Now the signal paths in branches B1 and B2 become more symmetric due to the additional common-gate amplifier, thus, the imbalance is reduced. However, imbalance still exists in the circuit shown in Fig. 3(b) because of the parasitics in parallel with the tail current source at node P. To overcome this issue and increase voltage headroom, the current source is removed. The resulting complete schematic of the proposed active balun is shown in the right part of Fig. 2, where R_1 is identical to R_2 and M7 is identical to M8. Considering channel length modulation and bulk effect, the aspect ratio of M5 is slightly smaller than M6.

Another merit of the proposed active balun is that it inherently takes advantage of noise-canceling technique[14]: The noise current of transistor M5 is partly cancelled at the output node. As a result, the overall noise performance is dominated by the input transistor M4. Since, as mentioned before, the parasitics at node X does not affect the matching property, M4's aspect ratio can be set large to increase its transconductance and consequently reduce its noise contribution, only compromising the bandwidth.

3.2. Variable gain Cherry–Hooper amplifier

3.2.1. Gain and bandwidth

Seeking circuits with inherent wideband characteristic is a key issue in the design of cascade amplifiers, since the bandwidth extension technique using inductors in a multi-stage amplifier is very area consuming. The Cherry–Hooper amplifier is a good candidate thanks to its shunt-shunt feedback structure and has been widely used in high-speed circuits[4, 6, 9, 15]. In a bipolar process, emitter-follower is always employed in combination with Cherry–Hooper amplifier to further extend its bandwidth and provide some adjustability[15], however, in modern CMOS technology, the ever-decreasing supply voltage mandates different techniques.

The total bandwidth of n identical cascade amplifiers can be expressed as

$$\mathrm{BW_{tot}} = \mathrm{BW_C}\sqrt[m]{2^{1/n} - 1}, \tag{2}$$

where m is equal to 2 for first-order stages and 4 for second-order stages[16]. If a total bandwidth of 3 GHz is required

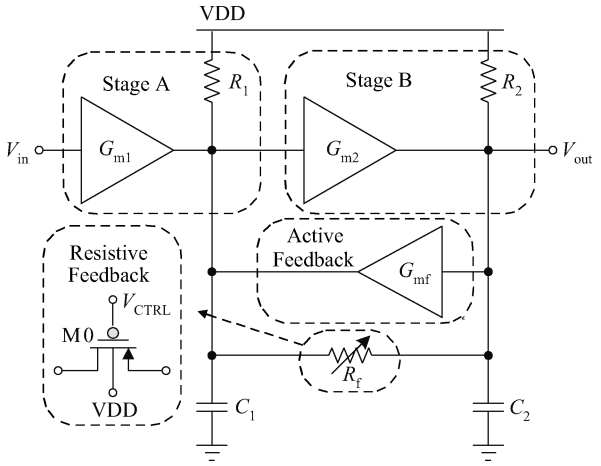

Fig. 4. Topology of the proposed Cherry–Hooper amplifier.

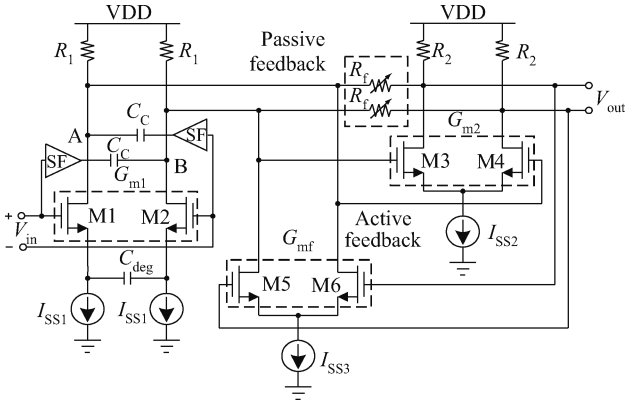

Fig. 5. Realization of the proposed variable gain Cherry–Hooper amplifier.

for the three-stage amplifier created with second-order gain cells, each stage must have a bandwidth at least 4.2 GHz accordingly. To achieve this bandwidth requirement, a modified Cherry–Hooper amplifier with an additional active feedback loop is proposed. Its topology is shown in Fig. 4. There are two feedback loops—both passive and active. The passive shunt-shunt feedback with R_f exists in conventional Cherry–Hooper amplifiers. Herein, R_f is realized by a PMOS transistor M0 working in triode region for gain tuning purpose. M0's gate voltage V_{CTRL} controls the amount of resistive negative feedback and thus determines the gain. When V_{CTRL} is high enough to cut off M0, active feedback dominates, the amplifier reaches its highest gain value. As V_{CTRL} decreases, M1 is turned on and the gain is reduced. An active feedback is added in parallel with the resistive feedback. Such an arrangement employs a transconductance G_{mf} to return a fraction of the output to the input of G_{m2}[16]. The transfer function of this amplifier can be obtained:

$$A_v(s) = G_1 G_2 R_{1f} R_{2f}[R_{1f} R_{2f} C_1 C_2 s^2 + (R_{1f} C_1 + R_{2f} C_2)\, s + G_f G_2 R_{1f} R_{2f} + 1]^{-1}, \tag{3}$$

where

$$G_1 = G_{m1}, \tag{4}$$

$$G_2 = G_{m2} + \frac{1}{R_f}, \tag{5}$$

$$G_f = G_{mf} - \frac{1}{R_f}, \tag{6}$$

$$R_{1f} = R_1 \| R_f = \frac{R_1 R_f}{R_1 + R_f}, \tag{7}$$

$$R_{2f} = R_2 \| R_f = \frac{R_2 R_f}{R_2 + R_f}. \tag{8}$$

According to Eq. (3), the second-order parameters, such as the DC gain A_{v0}, damping ratio ζ and nature frequency ω_n, can be expressed as

$$A_{v0} = \frac{G_1 G_2 R_{1f} R_{2f}}{1 + G_f G_2 R_{1f} R_{2f}}, \tag{9}$$

$$\zeta = \frac{1}{2} \frac{R_{1f} C_1 + R_{2f} C_2}{\sqrt{R_{1f} R_{2f} C_1 C_2 (1 + G_f G_2 R_{1f} R_{2f})}}, \tag{10}$$

$$\omega_n^2 = \frac{1 + G_f G_2 R_{1f} R_{2f}}{R_{1f} R_{2f} C_1 C_2}. \tag{11}$$

The above equations reveal that both the amplifier's cell gain and bandwidth are dependent on G_{mf} and R_f. From Eqs. (6) and (9), it is obvious that A_{v0} decreases while G_{mf} is increased. However, the relationship between A_{v0} and R_f is not clear. By calculating the derivative of Eq. (9) with respect to R_f, it can be found that A_{v0} is a monotonic increasing function of R_f as long as the relationship

$$1 + G_{m2}^2 R_1 R_2 \leqslant G_{m2} (R_1 + R_2) \tag{12}$$

holds. In this design, $G_{m2} \approx 8$ mS, $R_1 \approx R_2 \approx 400\ \Omega$, thus, Equation. (12) can always be satisfied.

The maximally flat Butterworth response requires $\zeta = 1/\sqrt{2}$. Under this condition, $\omega_{-3dB} = \omega_n$. From Eqs. (9) and (11), the gain bandwidth product (GBW) is given by

$$\mathrm{GBW} = A_{v0} f_{-3dB} = \frac{1}{2\pi} \frac{G_1 G_2}{C_1 C_2} \frac{1}{\omega_{-3dB}}. \tag{13}$$

Since $G_1/C_1 = G_{m1}/C_1 = 2\pi f_T$, $G_2/C_2 = (G_{m2} + 1/R_f)/C_2 = 2\pi f_T + 1/R_f C_2$, Equation. (13) can be reformulated as

$$\mathrm{GBW} = A_{v0} f_{-3dB} = f_T \frac{f_T + \dfrac{1}{2\pi R_f C_2}}{f_{-3dB}}. \tag{14}$$

According to Eq. (14), the GBW in the proposed circuit topology is extended beyond the technology f_T by a factor $(f_T + 1/2\pi R_f C_2)/f_{-3dB}$. It is larger than f_T/f_{-3dB} when only active feedback is used as described in Ref. [16]. The circuit implementation of the proposed topology is shown in Fig. 5.

3.2.2. Modified negative capacitive neutralization

In a cascade amplifier with identical gain cells, the input capacitance of each stage acts as the load of the proceeding stage and limits the bandwidth. This loading effect is further deteriorated by the Miller effect. Negative Miller capacitance (NMC) is commonly used to minimize this effect[17]. By setting the compensation capacitance C_C equal to the gate-drain capacitance C_{gd} of the input differential pair, the coupling through C_{gd} can be neutralized. However, a wideband circuit with deep-submicron technology renders C_{gd} less than 50 fF. It is thus very difficult to make C_C equal to such a small C_{gd} accurately due to layout parasitics and process variations. Furthermore, an over-emphasized C_C brings the risk of instability. To overcome this drawback, a source follower (SF) is embedded in the compensation path, as shown in Fig. 5. The net Miller capacitance under NMC compensation is given by

$$C_{MC} = C_{gd}(1 + |A_v|) + C_C(1 - |A_v A_{SF}|), \qquad (15)$$

where A_v is the voltage gain of the differential pair and A_{SF} is the voltage gain of the SF. Since A_{SF} is less than an unit, C_C should be augmented to maintain the neutralization condition. A larger C_C exhibits more tolerance to routing parasitics and process variations.

Another benefit brought by the SF is better isolation of positive feedback through C_C. When only the feedforward path is available, the stability is improved.

3.2.3. DC offset cancelling

It is a commonly used method to prevent DC offsets propagation in cascade amplifiers by AC coupling. In wideband circuits, the coupling capacitor should be made large enough to pass low frequency signals. If AC coupling is required between each stage, a large amount of chip area will be occupied by capacitors. Furthermore, the parasitic resistance and capacitance of the large coupling capacitors deteriorates signals at high frequencies. Feedback is also widely employed in DC offset cancelling, either with a low pass filter[4, 16] or with an integrator[18] in the feedback path. However, feedback should be carefully incorporated in high frequency circuits since it may bring stability issues. Herein, capacitive source degeneration is adopted to cancel DC offset locally, as shown in Fig. 5. According to the equivalent half-circuit illustrated in Fig. 6, the effective transconductance of G_{m1} is given by

$$G_{m1} = \frac{g_{m1}(sR_{SS} \cdot 2C_{deg} + 1)}{sR_{SS} \cdot 2C_{deg} + (1 + g_{m1}R_{SS})}, \qquad (16)$$

where R_{SS} is the output resistance of I_{SS1}, which is at least several kΩ. The DC gain of this amplifier is about R_1/R_{SS} and this value is always much less than 1. Thus, the DC offset is minimized with no discernible impact on high frequency gain as long as node X can be considered as AC ground, i.e.,

$$f \gg \frac{1}{2\pi}\frac{1 + g_{m1}R_{SS}}{R_{SS} \cdot 2C_{deg}}. \qquad (17)$$

3.2.4. Common mode feedback

Due to DC coupling between each CH-VGA, the operating point fluctuation of one cell would degrade the performance of all its following cells. A common mode feedback (CMFB) circuit is employed to stabilize the circuit operating point and improve its immunity to process, power supply voltage and temperature (PVT) variations. The concept of CMFB circuit is shown in Fig. 7. Partial feedback is used here considering the loop stability characteristic.

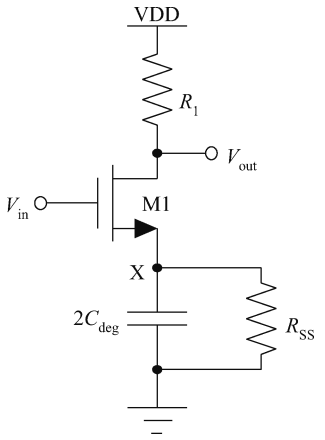

Fig. 6. Equivalent half-circuit of Gm1 for DCOC.

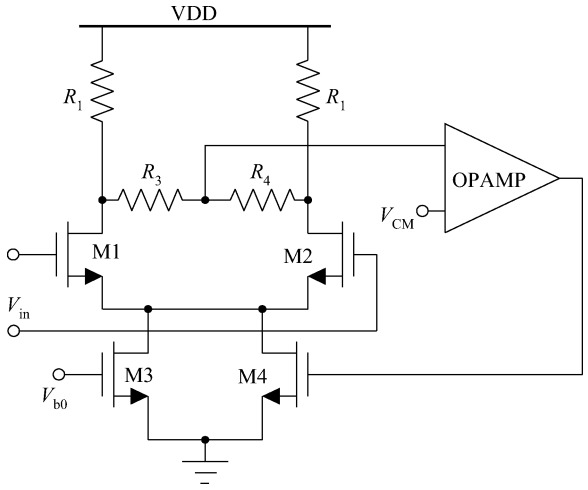

Fig. 7. The concept of CMFB.

3.3. f_T-doubler output buffer

An open drain f_T-doubler buffer[16] is employed to drive off-chip loads for measurement purposes, as shown in Fig. 8. In this topology, the input capacitance due to C_{gs} of the differential pair is reduced by half due to M3 and M4. The penalty is higher power dissipation. Off-chip inductive peaking is also used to extend the bandwidth. The power dissipation of this buffer is 10 mA.

4. Measurement results

The proposed wideband VGA was fabricated in SMIC 0.13 μm 1P8M mixed-signal and RF CMOS technology with inductors that are implemented by using the top metal layer. There are other building blocks fabricated together in the same chip. The microphotograph of the proposed VGA is shown in Fig. 9. The core VGA area is 0.86 × 0.56 mm^2. The chip is

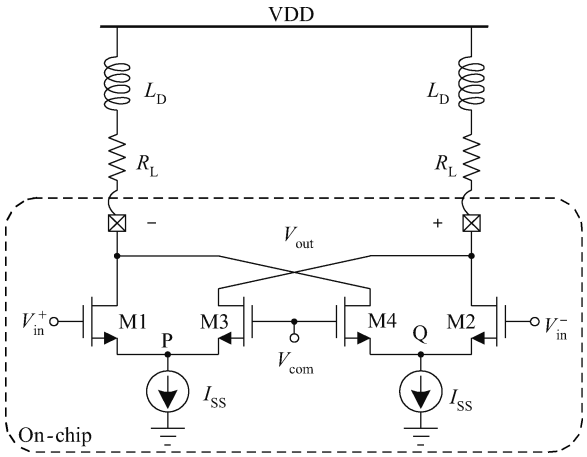

Fig. 8. f_T-doubler output buffer.

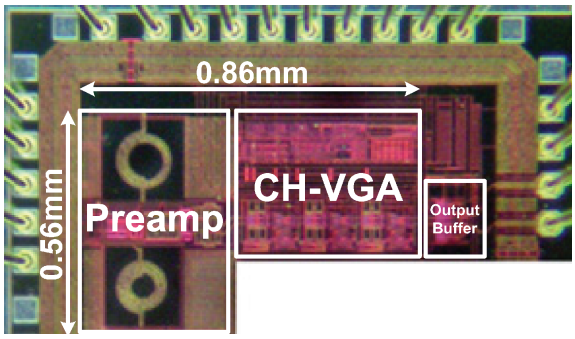

Fig. 9. Die microphotograph of the proposed VGA.

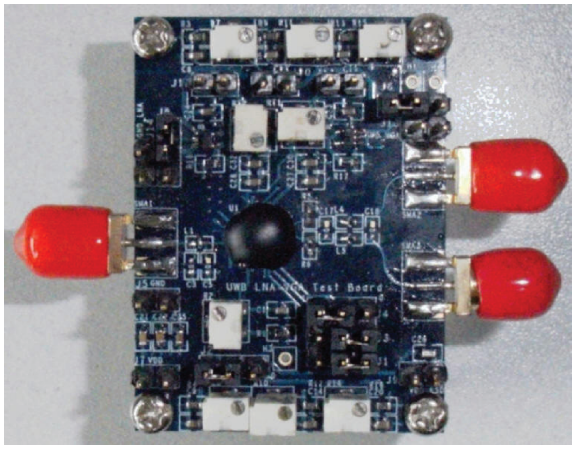

Fig. 10. Test PCB.

directly bonded to a 4-layer FR-4 substrate for measurement, as shown in Fig. 10.

A vector network analyzer (Agilent E5071B), a signal source generator (Agilent E8267D) and a spectrum analyzer (Agilent E4440A) were used to measure the VGA's gain, linearity and noise performance. Figure 11 displays the measured frequency responses with control voltage V_{CTRL} ranging from 0.5 to 0.8 V in 0.05 V steps. The measured bandwidth of the VGA is from 0.8 to 3 GHz with a gain control range of 35 dB (0–35 dB). The lower 3-dB bandwidth is limited by the DCOC circuit as described in Section 3.2.3. Herein, the source degeneration capacitance is set to be 1.2 pF. According to Eq. (16), the lower 3-dB bandwidth of a single CH-VGA can be calculated to be about 560 MHz. When three such stages are cascaded, the overall lower 3-dB bandwidth is 800 MHz, which is consistent with the measured result. The frequency response at the highest gain state (V_{CTRL} = 0.8 V) shows some ripples. The probable reason can be explained as follows: the resistive feedback path in CH-VGA is cut off when the gain reaches its largest value, which renders the nonlinearity characteristic free of any suppression. Then harmonics are generated and contaminate the frequency response spectrum.

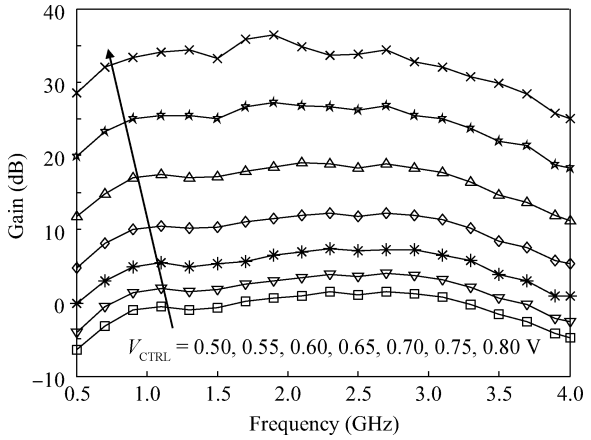

Fig. 11. Measured frequency response under different control voltages.

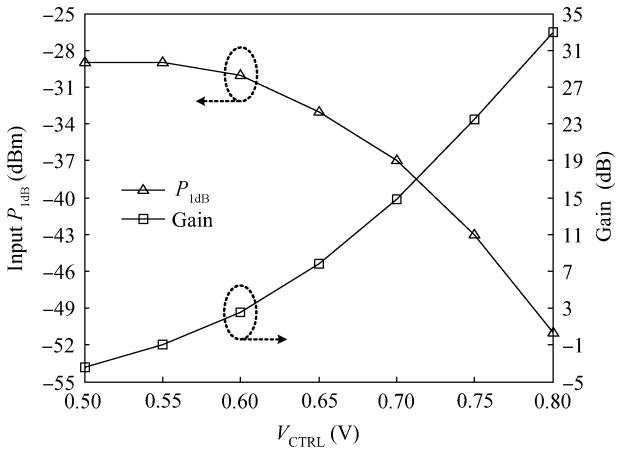

Fig. 12. Measured P_{1dB} and gain versus V_{CTRL} @ 1.9 GHz.

The measured input 1 dB compression point (P_{1dB}) and voltage gain are presented as a function of the control voltage V_{CTRL} at a test frequency 1.9 GHz in Fig. 12, revealing input P_{1dB} of –29 dBm at –3 dB gain, and –51 dBm at 33 dB gain. P_{1dB} decreases as the gain increases. The measured noise figure performance at different gain settings are shown in Fig. 13. The noise figure varies from 9 to 17 dB in the frequency range between 0.8 and 3 GHz. It is minimized at the maximum gain state and increases as the gain decreases.

The proposed VGA dissipates 26 mA under 1.2 V power supply and the output buffer uses 10 mA current to drive the output load. The measurement results and a comparison with previous studies are summarized in Table 1.

Table 1. Performance summary and comparison.

Reference	Ref. [4]	Ref. [8]	Ref. [9]	This work
Process	90 nm CMOS*	0.18 μm CMOS	0.13 μm BiCMOS	0.13 μm CMOS
Supply voltage (V)	1	1.8	1.8	1.2
Bandwidth (GHz)	2.2	0.004–0.9	9–15	0.8–3
Gain (dB)	–10 to 50	–39 to 55	–3 to 16	0–35
P_{1dB} (dBm)	–55 to –13	–59 to –11	—	–51 to –29
NF (dB)	17–30	6.8–55.3	—	9–17
Power (mW)	2.5	20.5	82	32
VGA area (mm^2)	0.01	0.42	0.8**	0.49

* Low-threshold voltage devices are used. ** Area with pads.

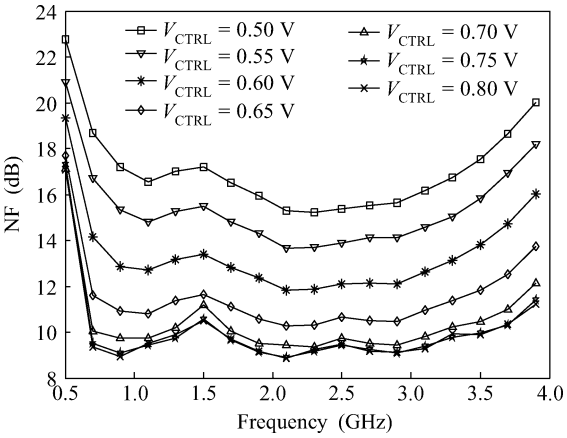

Fig. 13. Measured noise figure response versus various control voltage V_{CTRL}.

5. Conclusion

A wideband CMOS VGA has been designed and implemented on silicon. The proposed VGA utilizes a fixed gain preamplifier to reduce noise. A novel active balun circuit was used for single-to-differential conversion. Modified Cherry–Hooper amplifiers are connected in cascade to realize the gain tunable stage. Dual loop feedback has been proposed to extend the CH-VGA's bandwidth. To compensate the Miller effect, negative capacitive neutralization technique has been improved, resulting in reduced sensitivity of compensation capacitor to layout parasitics and better isolation in the positive feedback path. The chip prototype was fabricated in an SMIC 0.13 μm CMOS process, which achieves a gain tuning range from 0 to 35 dB within the bandwidth from 0.8 to 3 GHz.

References

[1] Momeni O, Hashemi H, Afshari E. A 10-Gb/s inductorless transimpedance amplifier. IEEE Trans Circuit Syst II: Express Briefs, 2010, 57(12): 926

[2] Han J, Choi B, Seo M, et al. A 20-Gb/s transformer-based current-mode optical Receiver in 0.13-μm CMOS. IEEE Trans Circuit Syst II: Express Briefs, 2010, 57(5): 348

[3] Huang H, Chien J, Lu L H. A 10-Gb/s inductorless CMOS limiting amplifier with third-order interleaving active feedback. IEEE J Solid-State Circuits, 2007, 42(5): 1111

[4] Wang Y, Afshar B, Cheng T, et al. A 2.5 mW inductorless wideband VGA with dual feedback DC-offset correction in 90 nm CMOS technology. IEEE RFIC Symp Dig, 2008: 91

[5] Sobel D, Brodersen R. A 1 Gb/s mixed-signal baseband analog front-end for a 60 GHz wireless receiver. IEEE J Solid-State Circuits, 2009, 44(4): 1281

[6] Afshar B, Wang Y, Niknejad A. A robust 24 mW 60 GHz receiver in 90 nm standard CMOS. ISSCC Dig Tech Papers, 2008: 182

[7] Cabric D, Chen M, Sobel D, et al. Future wireless systems: UWB, 60 GHz, and cognitive radios. IEEE CICC, 2005: 793

[8] Lee H, Lee K, Hong S. A wideband CMOS variable gain amplifier with an exponential gain control. IEEE Trans Microw theory Tech, 2007, 55(6): 1363

[9] Abbott J, Plett C, Rogers J. A 15 GHz, 1.8 V, variable-gain, modified Cherry–Hooper amplifier. IEEE RFIC Symp Dig, 2005: 645

[10] Joo S, Choi T, Jung B. A 2.4-GHz resistive feedback LNA in 0.13-μm CMOS. IEEE J Solid-State Circuits, 2009, 44(11): 3019

[11] Borremans J, Wambacq P, Soens C, et al. Low-area active-feedback low-noise amplifier design in scaled digital CMOS. IEEE J Solid-State Circuits, 2008, 43(11): 2422

[12] Joo S, Choi T, Kim J, et al. A 3-to-5 GHz UWB LNA with a low-power balanced active balun. IEEE RFIC Symp Dig, 2009: 303

[13] Rajashekharaiah M, Chen E. A new gain controllable on-chip active balun for 5 GHz direct conversion receiver. IEEE ISCAS, 2005: 5115

[14] Blaakmeer S C, Klumperink E A M, Nauta B, et al. An inductorless wideband balun-LNA in 65 nm CMOS with balanced output. IEEE ESSCIRC Dig Tech Papers, 2007: 364

[15] Holdenried C, Haslett J, Lynch M. Analysis and design of HBT Cherry–Hooper amplifiers with emitter-follower feedback for optical communications. IEEE J Solid-State Circuits, 2004, 39(11): 1959

[16] Galal S, Razavi B. 10-Gb/s limiting amplifier and laser/modulator driver in 0.18-μm CMOS technology. IEEE J Solid-State Circuits, 2003, 38(12): 2138

[17] Haines G, Mataya J, Marshall S. IF amplifier using Cc compensated transistors. IEEE ISSCC Dig Tech Papers, 1968: 120

[18] Crain E, Perrott M. A 3.125 Gb/s limit amplifier in CMOS with 42 dB gain and 1 μs offset compensation. IEEE J Solid-State Circuits, 2006, 41(2): 443