A 0.18 μm CMOS Gilbert low noise mixer with noise cancellation*

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Abstract: This paper presents a broadband Gilbert low noise mixer implemented with noise cancellation technique operating between 10 MHz and 0.9 GHz. The Gilbert mixer is known for its perfect port isolation and bad noise performance. The noise cancellation technique of LNA can be applied here to have a better NF. The chip is implemented in SMIC 0.18 μm CMOS technology. Measurement shows that the proposed low noise mixer has a 13.7–19.5 dB voltage gain from 10 MHz to 0.9 GHz, an average noise figure of 5 dB and a minimum value of 4.3 dB. The core area is 0.6×0.45 mm^2.

Key words: noise cancellation; mixer; LNA; low noise figure

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1. Introduction

Nowadays, there are several kinds of industry professional wireless networks in China. The RF front-ends of these networks are difficult to match with each other. Given that the working frequency band of these networks mainly lies between the 100 MHz to 1.2 GHz range, a broadband front-end covering this band is needed. The down-conversion mixer is one of the critical blocks in the front-end. The most popular topology is the Gilbert mixer, which can have a good performance of port isolation and a high conversion gain. However, the large noise figure of the Gilbert mixer will degrade the entire transceiver performance. This usually requires the former block LNA, a high gain and a low noise figure. To improve the NF of LNAs, power dissipation will be a problem. This can be solved if the NF of the mixer is low enough.

There are two main sources of noise: the transconductor stage and the switch stage. According to Ref. [1], the $1/f$ noise of the switch stage is proportional to the DC current flowing through it. References [2, 3] apply the current injection technique to lower the DC current of switch stage to reduce the $1/f$ noise. However, this technique has no benefit for the white noise of the transconductor stage.

There are several solutions for getting better noise performance of LNAs. The noise cancellation technique is a good candidate to handle it. The concept of noise cancellation is first proposed in Ref. [4]. Lately, this concept has been utilized to design a low noise figure LNA in Refs. [2, 5]. The NF can be reduced significantly. This LNA NF improving technique can be applied in the Gilbert mixer.

In this paper, a CMOS broadband Gilbert mixer is presented with the transconductor stage implemented by the noise cancellation technique. The noise is much less than the traditional Gilbert mixer. Meanwhile, the gain of the mixer is high enough to take off the LNA. This leads to a lower power dissipation of the whole system. The mixer works between 10 MHz to 0.9 GHz and has a better NF and conversion gain performance over other broadband mixers.

2. Basic noise cancellation principle

To understand how to cancel the noise generated by the MOSFET, the schematic of a basic amplifier is shown in Fig. 1. I_n represents the channel noise of the a MOSFET working in saturation region. I_n^2 which is the channel noise spectral density and can be expressed as $4KT\gamma g_{d0}$, where the g_{d0} is the drain–source conductance when the V_{DS} equals zero. K is the Boltzmann constant and T is the absolute temperature. The value of the parameter γ depends on the channel length of the MOSFET.

There are two critical nodes of this topology, which are defined as node X and node Y. The MOSFET is biased as a CS configuration. So the signal in node X and node Y are out-of-phase.

The noise current of I_n flows out of the MOSFET through the R and R_s (Fig. 1). With respect to ground, the noise of node X and node Y are in-phase. If a voltage adder can be applied

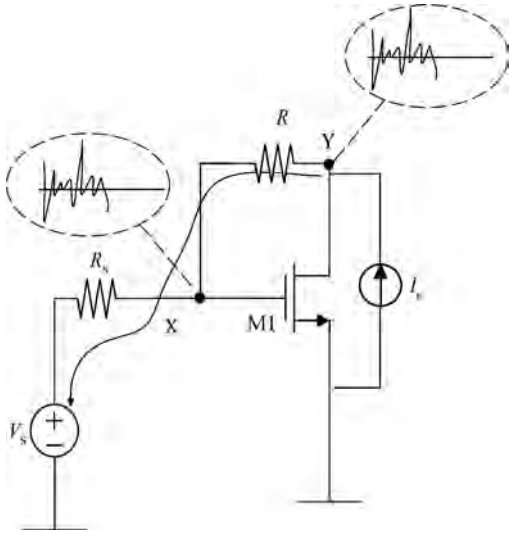

Fig. 1. Basic noise cancellation concept.

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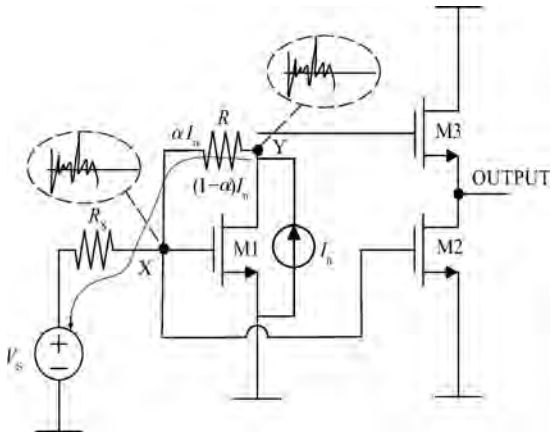

Fig. 2. Noise cancellation transconductor.

after this stage, the signal of node X and node Y can be added while the noise of these two nodes can be cancelled. This leads to a zero contribution of noise to the output by the input matching MOSFET.

3. NF of noise cancellation transconductor

Figure 2 shows the transconductor of the mixer. It has the topology of a noise cancellation cell. There are three main MOSFETs used in this noise cancellation cell, M1, M2 and M3.

M1 acts as the stage of input matching. The impedance of this network is $Z_{\rm IN} = 1/g_{\rm m1}$ and the voltage gain of Y over X is $A_{\rm YX} = V_{\rm Y}/V_{\rm X} = 1 - g_{\rm m1}R$[1]. If $1/g_{\rm m1} = R_{\rm S}$, input matching is satisfied.

Now let us analyze noise contribution of all the noise sources and the NF of this transconductor. As R changes, a part of the noise of M1 described as $\alpha I_{\rm n}$ will flow through $R_{\rm S}$ and R, with $0 < \alpha < 1$. The noises of node X and node Y due to the noise of M1 are in-phase. The voltage adder is formed by M2 and M3.

M2 is a CS configuration, therefore the noise voltages of node X and the output node have opposite signs. M3 is a source follower construction leading to a same sign of noise at the output node and node Y. These two different functions will cancel the noise at the output node due to M1. Meanwhile, the signal of input will be added at the output node through these two paths.

The noise voltages at node X and node Y are

$$\begin{aligned} V_{\rm X,n} &= \alpha I_{\rm n} R_{\rm S}, \\ V_{\rm Y,n} &= \alpha I_{\rm n}(R_{\rm S} + R). \end{aligned} \tag{1}$$

Then the noise output due to M1 is equal to

$$\begin{aligned} V_{\rm OUT,n} &= V_{\rm Y,n} + V_{\rm X,n}A_{\rm V2} \\ &= \alpha I_{\rm n}(R_{\rm S} + R) + \alpha I_{\rm n} R_{\rm S} A_{\rm V2}. \end{aligned} \tag{2}$$

If output noise due to M1 is zero, $V_{\rm OUT,n} = 0$, the voltage gain of M2 can be achieved

$$A_{\rm V2} = \frac{V_{\rm Y,n}}{V_{\rm X,n}} = -\left(1 + \frac{R}{R_{\rm S}}\right). \tag{3}$$

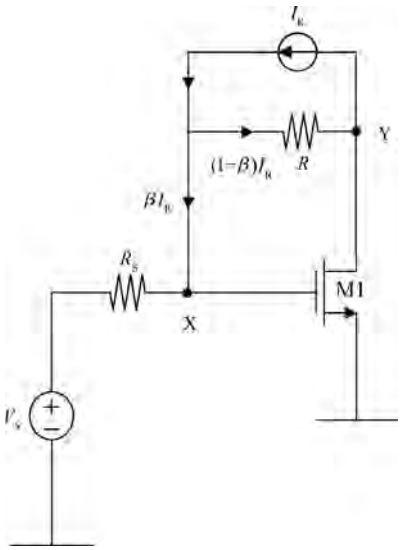

Fig. 3. Noise current of feedback resistor R.

By circuit inspection, this gain can also be described as

$$A_{\rm V2} = -\frac{g_{\rm m2}}{g_{\rm m3}}. \tag{4}$$

The total signal gain by adding the two paths signal is

$$\begin{aligned} A_{\rm OX} &= \frac{V_{\rm OUT}}{V_{\rm X}} = 1 - g_{\rm m1}R + A_{\rm V2} \\ &= -g_{\rm m1}R - \frac{R}{R_{\rm S}} = -2\frac{R}{R_{\rm S}}. \end{aligned} \tag{5}$$

In Fig. 2, the noise voltage at node X controls the noise current flowing through M1,

$$\alpha I_{\rm n} R_{\rm S} g_{\rm m1} = (1 - \alpha) I_{\rm n}. \tag{6}$$

So $\alpha = 1/2$ if the input matching is satisfied.

$$\begin{aligned} {\rm NF_{M1}} &= \frac{4KT\gamma g_{\rm m1}\alpha^2(R_{\rm S} + R - R_{\rm S}A_{\rm V2})^2}{4KTR_{\rm S} \times \dfrac{1}{4} \times A_{\rm V2}^2} \\ &= \frac{\gamma g_{\rm m1}(R_{\rm S} + R - R_{\rm S}A_{\rm V2})^2}{R_{\rm S}A_{\rm OX}^2}. \end{aligned} \tag{7}$$

The white noise of resistor R is $I_{\rm R}$, which is divided into two branches $\beta I_{\rm R}$ and $(1 - \beta)I_{\rm R}$, as shown in Fig. 3.

Then the noise voltages of node X and node Y due to resistor R are

$$\begin{aligned} V_{\rm X,nR} &= \beta I_{\rm R} R_{\rm S}, \\ V_{\rm Y,nR} &= \beta I_{\rm R} R_{\rm S}(1 - g_{\rm m1}R), \\ V_{\rm X,nR} - V_{\rm Y,nR} &= (1 - \beta) I_{\rm R} R. \end{aligned} \tag{8}$$

Then $\beta = 1/2$ if $1/g_{\rm m1} = R_{\rm S}$.

Then

$${\rm NF_R} = \frac{(\beta I_{\rm R} R_{\rm S})^2}{4KTR_{\rm S} \times \dfrac{1}{4}} = \frac{\dfrac{1}{4}\dfrac{4KT}{R}R_{\rm S}^2}{4KTR_{\rm S} \times \dfrac{1}{4}} = \frac{R_{\rm S}}{R}. \tag{9}$$

Table 1. Noise contribution of the sources.

Noise source	Contribution
R_S	76.97%
NM_1	0.01%
NM_2	15.79%
NM_3	3.85%
R	0.03%

The last noise source is the voltage adder consisting of M2 and M3. The NF of this source is

$$\mathrm{NF}_{\mathrm{M2,3}} = \frac{\dfrac{4KT\gamma g_{\mathrm{m2}}}{g_{\mathrm{m2}}^2} + \dfrac{4KT\gamma}{g_{\mathrm{m3}}}}{4KTR_{\mathrm{S}} \times \dfrac{1}{4} \times A_{\mathrm{OX}}^2} = \frac{\gamma}{g_{\mathrm{m2}}}\left(\frac{1}{R_{\mathrm{S}}} + \frac{3}{R} + \frac{2R_{\mathrm{S}}}{R^2}\right). \tag{10}$$

So the total NF can be expressed as

$$\mathrm{NF} = 1 + \mathrm{NF}_{\mathrm{M1}} + \mathrm{NF}_{\mathrm{R}} + \mathrm{NF}_{\mathrm{M2,3}}.$$

With the noise cancellation working, the $\mathrm{NF}_{\mathrm{M1}}$ equals to 0. Then the NF is only determined by the latter two parts.

From the expressions, we can see that to have a low NF_{R}, the resistor R should be as large as possible. But a large R will cause some problems. From Eqs. (3) and (4), we can know that a large R means a large g_{m2} and a small g_{m3}. A small g_{m3} requires a large overdrive voltage which pushes the M2 into triode region. This problem will be discussed in the following sections.

To have a low $\mathrm{NF}_{\mathrm{M2,3}}$, the g_{m2} should be as large as possible according to Eq. (10). This will dissipate more power. This relationship shows the trade-off between power dissipation and NF.

To verify this derivation of the formula, a simulation about the noise contribution of the noise sources is done in Table 1.

This result shows that the theory of noise cancellation is right and available for low noise design. The noise contribution of the NM1 has been reduced to close to zero. The noise contribution of the source impedance R_{S} has been raising to as high as 76.97%. For a circuit whose source impedance keeps a constant of 50 Ω, the less the contribution of the source impedance, the less the NF.

4. Switch stage and current injection

As shown in Section 3, in order to reduce the noise contribution of the M2, a large DC current should flow through M2 to the switch stage. According to Ref. [6], a large amount of DC current in the switch stage will cause a large $1/f$ noise. Also, a large overdrive voltage of switch stage is required. This leads to a slow switching, making the conversion gain of the mixer lower.

To solve this problem, a current injection block is used to reduce the DC current of switch stage as shown in Fig. 4. The DC current of transconductor stage will mainly flow into Min2 and Min3. Then the DC current of switch stage can be small

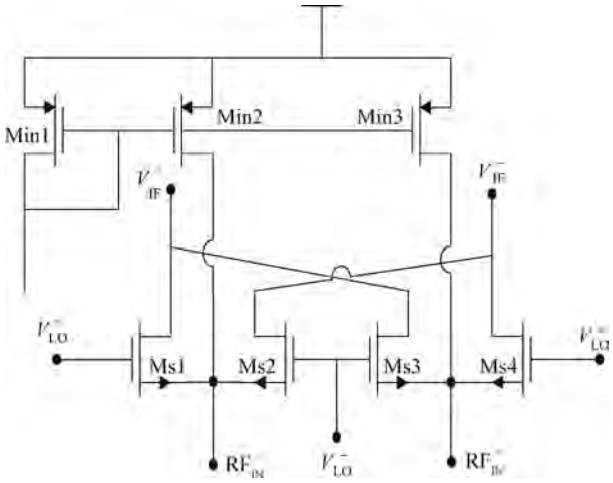

Fig. 4. Switch stage with a current injection block.

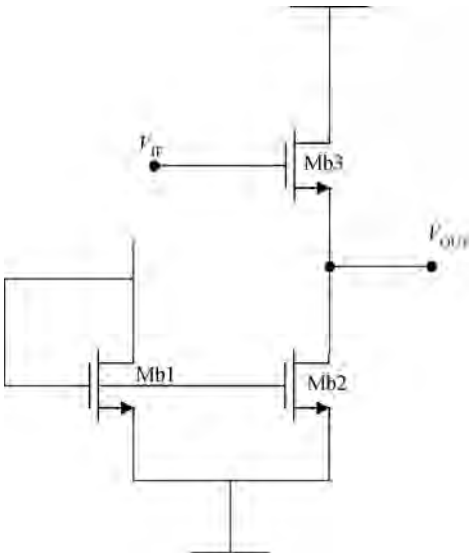

Fig. 5. Buffer for the output matching.

enough to have a low overdrive voltage. The noise and conversion gain performance of the mixer with this current injection block can be better.

5. Buffer for the output matching

In order to have a good output matching, a source follower construction is used as shown in Fig. 5. To ensure the output impedance is 50 Ω, the g_{mb3} should be 20 mS. With this buffer, the overall conversion gain will have a loss of 6 dB. So, the actual gain of the mixer should be 6 dB larger than the measurement result.

6. The proposed circuit

Figure 6 shows the proposed circuit of the noise cancellation mixer. According to Section 3, to have a large R, g_{m2} should be large while g_{m3} should be small. If the DC current in M2 is as large as that in M3, the large overdrive voltage of

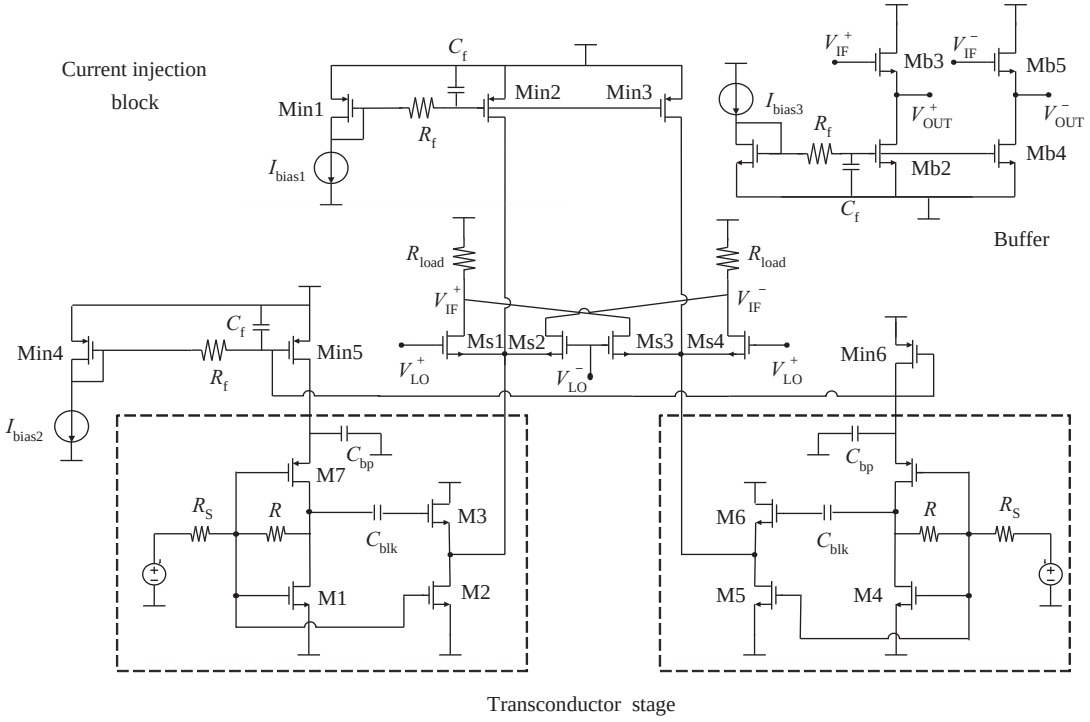

Fig. 6. Schematic of the proposed circuit (biasing not shown).

Table 2. Summary and performance comparison.

Parameter	This work	Ref. [7]	Ref. [8]	Ref. [6]
Technology (μm)	0.18	0.18	0.09	0.13
Frequency band (GHz)	0.1–0.9	0.9	0.1–3.85	1–5.5
Voltage gain (dB)	13.7–19.5	13	20	11.5
NF_{DSB} (dB)	4.6–7.2	8	9–12 (0.1–1 GHz)	3.9
P_{1dB} (dBm)	–20 (0.9 GHz)	–23	–12.83 (2.3 GHz)	–10.5
S_{11} (dB)	< -9.3	–31	< -10	< -8.8
Core size (mm^2)	0.27	0.33	0.88	0.315
Power (mA)	14	6.7	8.15	23

M3 will push M2 into triode region. Fortunately, the current injection block for a low $1/f$ noise of the switch stage can deal with it. If the current of Min2 is close to that of M2, then currents flowing in M3 and switch stages are small enough to avoid these problems.

The input matching network is made up with a NMOS and PMOS to reuse the DC current for a lower power dissipation. Another advantage of this technique is that there is no requirement for the DC bias.

In the transconductor stage, there are two capacitors C_{blk} and C_{bp}. C_{blk} is a blocking capacitor. C_{bp} is a bypass capacitor to make sure the source of M7&M8 virtual ground.

For good output matching, a source follower is used to provide an output impedance of 50 Ω. R_f and C_f are used to filter out the noise of current from the outside.

The mixer was designed using SMIC 0.18 μm technology. The simulation and layout were done with a Cadence spectreRF. PCB measurements were carried out. The LO frequency is 900 MHz.

Figure 7(a) shows the chip photograph of the total circuit. The core occupies 0.6×0.45 mm^2. Figure 7(b) shows the S_{11} covering the frequency from 10 MHz to 1 GHz. The best input matching is achieved when the S_{11} can reach to –27 dB. Over all the band of measurement, $S_{11} < -9.3$ dB. Figure 7(c) shows the S_{22} of the working band. Between 10 MHz and 1 GHz, even the worst S_{22} still reaches to –10 dB.

Figure 8 shows the NF of the mixer from 10 to 900 MHz. We can see that a minimum NF of 4.6 dB is achieved when the frequency is 92 MHz. As the frequency rises, the NF has a tendency of rising. This can be explained that as the frequency rises, the parasitic capacitor of MOSFET will affect the phase of the noise at node X and node Y, making the noise cancellation less efficient. The balun used for single signal transforming into differential signals has an insert loss of 0.32 dB. So, the NF of the measurement should minus this insert loss. This means the minimum NF is 4.3 dB. Figure 8 also shows the conversion gain of the proposed mixer. The conversion gain is 7.7 to 13.5 dB between 10 to 900 MHz. The buffer for output matching will degrade the gain by 6 dB. So the actual conversion gain of the proposed mixer is 13.7 to19.5 dB.

Table 2 shows a comparison between this work and other similar mixer. This work has a better performance of conversion gain than other works. Also, the NF of this work has a competitive advantage over the other two mixers. The pro-

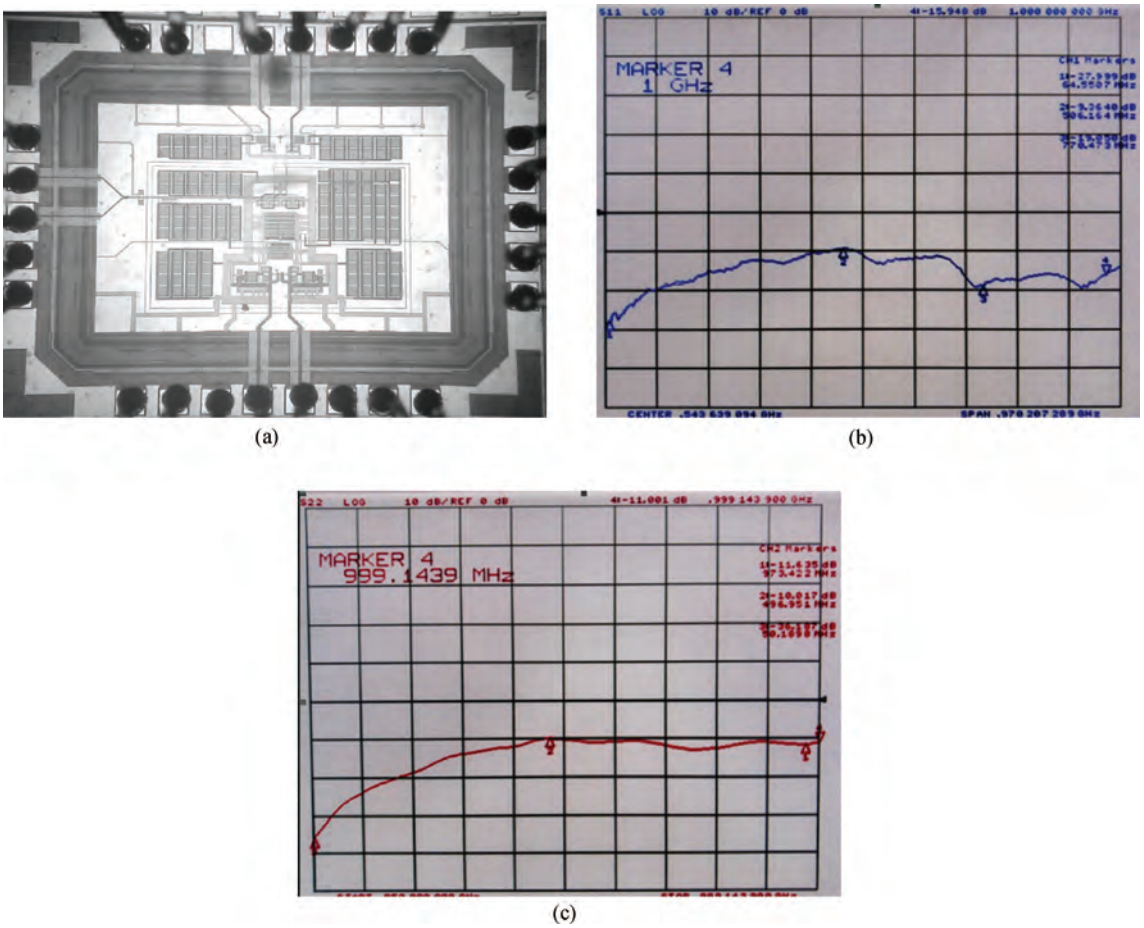

Fig. 7. (a) Chip photograph. (b) Measured S_{11}. (c) Measured S_{22}.

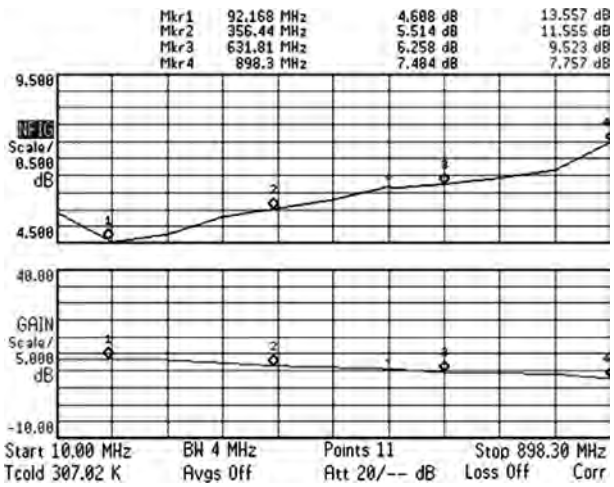

Fig. 8. Measured NF and conversion gain.

posed work and Reference [6] shows the trade-off between the NF and the power dissipation.

7. Conclusion

A low noise mixer using a noise cancellation technique is presented. The proposed mixer works between 10 MHz and 0.9 GHz. The conversion gain of this mixer is 13.7 to 19.5 dB over the working band. The NF has a minimum value of 4.3 dB while 6.9 dB when the frequency rises. The S_{11} achieves the best performance of –27 dB. The core of this mixer is only 0.27 mm^2.

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