Continuous analytic I–V model for GS DG MOSFETs including hot-carrier degradation effects

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Abstract: We have studied the influence of hot-carrier degradation effects on the drain current of a gate-stack double-gate (GS DG) MOSFET device. Our analysis is carried out by using an accurate continuous current–voltage (I–V) model, derived based on both Poisson's and continuity equations without the need of charge-sheet approximation. The developed model offers the possibility to describe the entire range of different regions (subthreshold, linear and saturation) through a unique continuous expression. Therefore, the proposed approach can bring considerable enhancement at the level of multi-gate compact modeling including hot-carrier degradation effects.

Key words: GS DG MOSFET; hot-carriers degradation effects; compact modeling; piece-wise models
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1. Introduction

Double-gate MOSFET architectures have been recognized as a leading candidate to extend the scaling limit of conventional bulk MOSFETs to 25 nm gate length and beyond due to their significant reduction of the short channel effects, which prevail in bulk MOSFETs[1]. The use of undoped Si films for DG MOSFETs avoids the problems resulting from dopant-impurity location randomness and improves carrier transport by the resulting mobility enhancement, so the idea of an undoped body is expected to become widespread in the coming years as miniaturization advances[2]. Several analytic potential and drain current models for undoped symmetric double gate MOSFETs have been derived by solving Poisson's and current continuity equations with the gradual channel approximation. The obtained expressions are able to take account of the volume inversion effects, which is not the case for charge-sheet approximation based models[3].

However, as device feature size shrinks down to deep submicron region, in order to get better device performance and higher package density, the characteristics degrade because of the hot-carrier effect[4]. For a deep submicron device, hot-carrier induced degradation becomes a major reliability concern and affects the optimal function. The main cause of the hot-carrier degradation effect in multi-gate devices is already discussed in many literature reviews[5, 6]. Recent works discussing the elaboration of new closed analytical models have been proposed to study DG MOSFET structures including the interfacial hot-carrier effects. This is achieved in order to investigate the scaling limits of these devices when defects generated by the injected carriers near the drain side are present. However, explored studies have shown two basic drawbacks: firstly, the majorities of these works are limited to the subthreshold regime and cannot be used to study device behavior in the linear or saturation regimes[7] and, secondly, the models employed are based on the charge-sheet approximation and some physics phenomena are missed[8]. Therefore, a profound analysis of the interfacial hot-carrier effects on the drain current is a mandatory requirement in order to facilitate the design of future CMOS integrated circuits.

In this paper, we propose a new continuous analytical model to study the performances of the GS DG MOSFET including hot-carrier degradation effects, based on closed-form solutions of Poisson's and current continuity equations. The possibility of developing an extended formulation for the GS DG MOSFET with an interfacial trap density is carried out in the rest of this paper and the model has three distinctive features.

(1) The device channel is assumed to be undoped (lightly doped) instead of the usual high channel doping density. Such absence of dopant atoms in the channel further reduces the mobility degradation by eliminating impurity scattering and avoiding random microscopic dopant fluctuations.

(2) The analytic drain current model covers all three regions of MOSFET operations, subthreshold, linear and saturation, thus maintaining strong continuity between different regions without the need for adjustable parameters, which are in general meaningless physically.

(3) The compact model for a GS DG MOSFET including the hot-carrier degradation effect is derived based on the Pao-Sah integral without the charge-sheet approximation, so that the volume inversion phenomenon in the subthreshold region can be properly predicted.

Our proposed long-channel model is ideally suitable for being the kernel of a GS DG MOSFET including a hot-carrier effects compact formulation. In addition, it can be used as a passage between analytical compact modeling and circuit simulators such as SPICE, Cadence and Anacad's Eldo in order to analyze the electrical circuit performance degradation due to age-related phenomena. For a complete compact model, this long-channel core would need to be enhanced with additional physical effects, such as short-channel and quantum mechanical effects.

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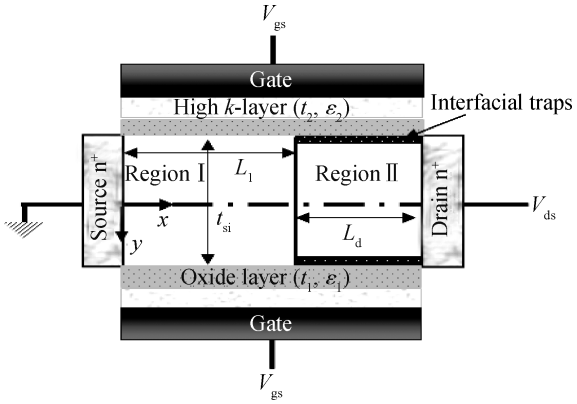

Fig. 1. Schematic diagram of a GS DG MOSFET with an interfacial trap density near the drain side.

2. Modeling approach

We consider a symmetric GS DG undoped n-channel MOSFET, as illustrated in Fig. 1.

We also consider a channel long enough so that the device electrostatics are described by 1-D Poisson's equation in the direction vertical to the channel. Neglecting the hole density, Poisson's equation in the silicon film is given by,

$$\frac{\mathrm{d}^2\psi(x)}{\mathrm{d}x^2} = \frac{\mathrm{d}^2\left(\psi(x)-V\right)}{\mathrm{d}x^2} = \frac{qn_\mathrm{i}}{\varepsilon_\mathrm{si}}\mathrm{e}^{q\left(\frac{\psi(x)-V}{kT}\right)}, \tag{1}$$

where q is the electronic charge, n_i the intrinsic carrier concentration, ε_si the permittivity of silicon, $\psi(x)$ the silicon band bending, and V the electron quasi-Fermi potential.

Despite that the drift–diffusion mechanism has been widely considered as the cornerstone modeling tool for various long channel devices, it is worthwhile employing more elaborated schema such as ballistic transport equations especially when dealing with the nanoscale case, where the mean free path of the carriers is bigger than that of the silicon film width[9].

Since the current mainly flows along the y-direction, we assume that V is constant along the x-direction; i.e., $V = V(y)$. This is the so called gradual channel approximation. Equation (1) can then be integrated twice to yield the solution[10],

$$\psi(x) = V - \frac{2kT}{q}\ln\left(\frac{t_\mathrm{si}}{2\beta}\sqrt{\frac{q^2n_\mathrm{i}}{2\varepsilon_\mathrm{si}kT}}\cos\frac{2\beta x}{t_\mathrm{si}}\right). \tag{2}$$

The constant β is related to ψ through the boundary condition deduced from Gauss's law,

$$\varepsilon_\mathrm{ox}\frac{V_\mathrm{gs}-\Delta\phi-\psi\left(x=\pm\frac{t_\mathrm{si}}{2}\right)}{t_\mathrm{oxeff}} = \pm\varepsilon_\mathrm{si}\left.\frac{\mathrm{d}\psi(x)}{\mathrm{d}x}\right|_{x=\pm\frac{t_\mathrm{si}}{2}}. \tag{3}$$

Here ε_ox is the permittivity of oxide, V_gs is the voltage applied to both gates, t_si and t_oxeff are the silicon and the effective oxide thicknesses, and $\Delta\phi$ is the work function of both the top and bottom gate electrodes with respect to the intrinsic silicon. The effective oxide layer thickness of insulator layer t_oxeff is given by the superposition of the thickness of the SiO_2 layer and the thickness of the high-k layer as follows[11],

$$t_\mathrm{oxeff} = t_1 + \frac{\varepsilon_1}{\varepsilon_2}t_2. \tag{4}$$

By substituting Eq. (2) into Eq. (3), we get a nonlinear equation relating β explicitly to different basic parameters,

$$\frac{2\varepsilon_\mathrm{si}t_\mathrm{oxeff}}{\varepsilon_\mathrm{ox}t_\mathrm{si}}\beta\tan\beta - \ln(\cos\beta) + \ln\beta = \frac{q\left(V_\mathrm{gs}-\Delta\phi-V\right)}{2kT} - \ln\left(\frac{2}{t_\mathrm{si}}\sqrt{\frac{2\varepsilon_\mathrm{si}kT}{q^2n_\mathrm{i}}}\right). \tag{5}$$

The hot-carrier-induced oxide-interface charge has a significant influence on two device properties: (1) it affects the local electric potential in the adjacent drain region; and (2) it changes the local channel electron mobility. The potential effect can be accounted for as an additional term in the total mobile charge per unit gate area Q_inv in the damaged region. By using Eq. (2) combined with $\frac{Q_\mathrm{inv}}{\varepsilon_\mathrm{si}} = 2\left.\frac{\mathrm{d}\psi(x)}{dx}\right|_{x=\frac{t_\mathrm{si}}{2}}$, required quantity Q_inv expressed in terms of β yields for each region,

$$Q_\mathrm{inv}(\beta) = \begin{cases} \dfrac{8\varepsilon_\mathrm{si}}{t_\mathrm{si}}\dfrac{kT}{q}\beta\tan\beta, & 0 \leqslant y \leqslant L_1, \\ \dfrac{8\varepsilon_\mathrm{si}}{t_\mathrm{si}}\dfrac{kT}{q}\beta\tan\beta - 2qN_\mathrm{f}, & L_1 \leqslant y \leqslant L. \end{cases} \tag{6}$$

The reduction of channel electron mobility can be represented by Mathiessen's rule, as proposed by Nishida and Sah[12]. This approach assumes that the total reciprocal mobility is composed of bulk mobility μ_o and oxide interface charge scattering mobility μ_ox as follows,

$$\mu_{i=1,2} = \begin{cases} \mu_0, & 0 \leqslant y \leqslant L_1, \\ \dfrac{\mu_0\mu_\mathrm{ox}}{\mu_0+\mu_\mathrm{ox}}, & L_1 \leqslant y \leqslant L, \end{cases} \tag{7}$$

where the electron mobility caused by the charge scattering is given by,

$$\mu_\mathrm{ox} = 1000 \times \frac{3\times10^{11}T}{80N_\mathrm{f}}. \tag{8}$$

For a given V_gs, β can be solved from Eq. (5) as a function of V. Note that V varies from the source to the drain, the functional dependence of $V(y)$ and $\beta(y)$ is determined by the current continuity equation, which requires the current I_ds given by $I_\mathrm{ds} = \mu WQ_\mathrm{inv}\mathrm{d}V/\mathrm{d}y$ to be constant, independent of V or y. The parameter μ is the effective mobility, and W is the device width. Note that $\mathrm{d}V/\mathrm{d}\beta$ can also be expressed as a function of β by differentiating Eq. (5) to get,

$$\frac{\mathrm{d}V}{\mathrm{d}\beta} = -\frac{2kT}{q}\left[\frac{1}{\beta} + \tan\beta + 2\frac{\varepsilon_\mathrm{si}t_\mathrm{oxeff}}{\varepsilon_\mathrm{ox}t_\mathrm{s}i}\frac{\mathrm{d}}{\mathrm{d}\beta}(\beta\tan\beta)\right]. \tag{9}$$

The solution of Pao–Sah's integral can be found in two adjacent channel regions by integrating both sides of the continuity equation from the source to the boundary of the damaged

Table 1. Asymptotic values and dominance rules for different regions of operation.

Regime	$f_r(\beta_s)$	$f_r(\beta_p)$	β_s	β_p	$g_r(\beta_s)$	$g_r(\beta_p)$
Subthreshold	$\ll -1$	$\ll -1$	$\ll 1$	$\ll 1$	—	—
	$\ln\beta_s$	$\ln\beta_p$	—	—	${\beta_s}^2/2$	${\beta_p}^2/2$
Linear	$\gg 1$	$\gg 1$	$\sim \pi/2$	$\sim \pi/2$	—	—
	$\beta_s\tan\beta_s$	$\beta_p\tan\beta_p$	—	—	$(\beta_s\tan\beta_s)^2$	$(\beta_p\tan\beta_p)^2$
Saturation	$\gg 1$	$\ll -1$	$\sim \pi/2$	$\ll 1$	—	—
	$\beta_s\tan\beta_s$	$\ln\beta_p$	—	—	$(\beta_s\tan\beta_s)^2$	${\beta_p}^2/2$

region L_1 then from the boundary to the drain[13] and valid expressions of the drain current in these regions are carried out as follows: for the fresh region we have,

$$I_{ds} = \mu_1 \frac{W}{L_1}\int_0^{V_p} Q_{inv}(V)\mathrm{d}V = \mu_1 \frac{W}{L_1}\int_{\beta_s}^{\beta_p} Q_{inv}(\beta)\frac{\mathrm{d}V}{\mathrm{d}\beta}\mathrm{d}\beta. \tag{10}$$

Substituting different factors in Eq. (10) and carrying out the integration analytically,

$$I_{ds} = \mu_1 \frac{4W\varepsilon_{si}}{t_{si}L_1}\left(\frac{2kT}{q}\right)^2 \times \left[\beta\tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si}t_{oxeff}}{\varepsilon_{ox}t_s i}(\beta\tan\beta)^2\right]_{\beta_p}^{\beta_s}, \tag{11}$$

and for the damaged region,

$$I_{ds} = \mu_2 \frac{W}{L_d}\int_{V_p}^{V_{ds}} Q_{inv}(V)\mathrm{d}V = \mu_2 \frac{W}{L_d}\int_{\beta_p}^{\beta_d} Q_{inv}(\beta)\frac{\mathrm{d}V}{\mathrm{d}\beta}\mathrm{d}\beta. \tag{12}$$

Substituting appropriate parameters as previously then carrying out the integration analytically yields,

$$I_{ds} = \mu_2 \frac{4W\varepsilon_{si}}{t_{si}L_d}\left(\frac{2kT}{q}\right)^2 \times \left[\beta\tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si}t_{oxeff}}{\varepsilon_{ox}t_{si}}(\beta\tan\beta)^2\right]_{\beta_d}^{\beta_p} - \mu_2 \frac{4WN_f kT}{L_d}\left[\ln\frac{\beta}{\cos\beta} + \frac{2\varepsilon_{si}t_{oxeff}}{\varepsilon_{ox}t_s i}(\beta\tan\beta)\right]_{\beta_d}^{\beta_p}. \tag{13}$$

As is clear from the obtained expressions of drain current in both considered regions, the channel length modulation effect is ignored, which can be explained by the fact that our framework is based on a long channel model. In order to take into account such phenomenon for scaled devices, we have to introduce a new effective length and some fitting parameters[14].

To compute the drain current we define the following two functions representing the right-hand side of Eqs. (5) and (11),

$$f_r(\beta) = 2r\beta\tan\beta - \ln(\cos\beta) + \ln\beta, \tag{14}$$

$$g_r(\beta) = \beta\tan\beta - \frac{\beta^2}{2} + r(\beta\tan\beta)^2. \tag{15}$$

Note that the range of β is $0 < \beta < \pi/2$ and r is a structural parameter defined as $r = \varepsilon_{si}t_{ox}/\varepsilon_{ox}t_{si}$ For given V_{gs} and V_{ds}, β_s and β_d are calculated from the conditions,

$$f_r(\beta_s) = (q/2kT)\left(V_{gs} - V_0\right), \tag{16}$$

$$f_r(\beta_d) = (q/2kT)\left(V_{gs} - V_0 - V_{ds}\right), \tag{17}$$

where

$$V_0 = \Delta\phi + \frac{2kT}{q}\ln\left(\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right).$$

At this level, β_p can be also obtained numerically by equating drain current expressions of both damaged and fresh regions.

In the limit case of a fresh device, all parameters correspond to those of the fresh region, hence $\beta_p \to \beta_d$, and as a result, our compact model reduces to the drain current model established in Ref. [15],

$$I_{ds} = \mu_1 \frac{4W\varepsilon_{si}}{t_{si}L}\left(\frac{2kT}{q}\right)^2 \times \left[\beta\tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si}t_{oxeff}}{\varepsilon_{ox}t_{si}}(\beta\tan\beta)^2\right]_{\beta_d}^{\beta_s}. \tag{18}$$

Here we have in hand all the ingredients required for the elaboration of the drain current model taking account of the hot-carrier degradation effects. Then we can write,

$$I_{ds} \propto \left[g_r(\beta_s) - g_r(\beta_p)\right]. \tag{19}$$

The asymptotic values and dominance rules characterizing different operation modes in the case of a fresh double gate device have been presented in Ref. [16] and extended later to the surrounding gate device[17]. Based on the same formalism, some useful expressions, needed for the piece-wise models deduction, are elaborated for the case of GS DG MOSFET including the hot-carrier degradation effect, as summarized in Table 1. It should be noted that without loss of generality, only the fresh region of the device is considered and the interfacial traps density effect is introduced through the intermediate parameter β_p and the reduced mobility in the damaged region μ_2.

3. Piece-wise model deduction

In the following, the GS DG MOSFET including hot-carrier effect regions of operation are derived from this continuous analytical model based on approximations given in Table 1.

(1) Subthreshold region[18]:

$$I_{ds} = I_{ds1} + I_{ds2}, \tag{20}$$

with

$$I_{ds1} = \mu_1 \frac{W t_{si} n_i kT}{L_1} e^{\frac{q(V_{gs}-\Delta\phi)}{kT}} \left(1 - e^{-\frac{qV_p}{kT}}\right),$$

and

$$I_{ds2} = \mu_2 \frac{W t_{si} n_i kT}{L_d} e^{\frac{q(V_{gs}-\Delta\phi)}{kT}} \left(1 - e^{-\frac{q(V_{ds}-V_p)}{kT}}\right),$$

are the subthreshold currents associated with the fresh and damaged regions in a similar way to the methodology proposed for 4-T and 3-T DG MOSFET based on the basic diffusion current[19],

$$J_n(y) = qD_n \frac{n_{min}(y)}{L} \left(1 - e^{\frac{V_{ds}}{V_t}}\right), \tag{21}$$

where D_n denotes the diffusion constant, and $n_{min}(y)$ is the minimum carriers concentration at a fixed location along the channel. The subthreshold current is proportional to the cross sectional area of the device, but independent of t_{oeffx}, which is a manifestation of "volume inversion" that cannot be reproduced by standard charge-sheet-based I–V models.

(2) Linear region above threshold[20]:

$$I_{ds} = 2\mu_1 C_{ox} \frac{W}{L_1} \left(V_{gs} - V_{th} - \frac{V_p}{2}\right) V_p, \tag{22}$$

where V_{th} is the threshold voltage, and C_{ox} is the oxide capacitance.

(3) Saturation region:

$$I_{ds} = \mu_1 C_{ox} \frac{W}{L_1} \times \left[\left(V_{gs} - V_{th}\right)^2 - 2r\left(\frac{2kT}{q}\right)^2 e^{\frac{q(V_{gs}-V_0-V_p)}{kT}}\right], \tag{23}$$

where the saturation current depends on $(V_{gs} - V_{th})^2$, as expected for a MOSFET. The saturation current approaches the saturation value with a difference term exponentially decreasing with V_p, in contrast to common piecewise models in which the current is made to be constant in saturation[21].

Since all precedent expressions of the drain current depend on the voltage at the boundary of both regions V_p rather than the parameters β_p, an implicit formula for V_p can be obtained from the boundary condition (5),

$$V_p = V_{gs} - \Delta\phi - \frac{2kT}{q} \times \left[\ln\left(\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right) + 2r\beta_p \tan\beta_p - \ln\frac{\cos\beta_p}{\beta_p}\right]. \tag{24}$$

4. Results and discussion

Values of the parameters used for the validation of our proposed model are summarized in Table 2. The range of some geometrical parameters is fixed according to our initial long channel device assumption, so that many alterations of the model regarding the scaling effects can be neglected.

Table 2. Values of parameters used in the simulation.

Parameter	Value
T	300 K
L	2×10^{-5} cm
L_1	$2L/3$ cm
N_f	1×10^{12} cm^{-2}
W	3×10^{-6} cm
t_{si}	2×10^{-6} cm
t_1	1×10^{-7} cm
ε_1	3.9
t_2	1.5×10^{-7} cm
ε_2	10
n_i	1.45×10^{10} cm^{-3}
μ_0	800 cm^2/(V·s)

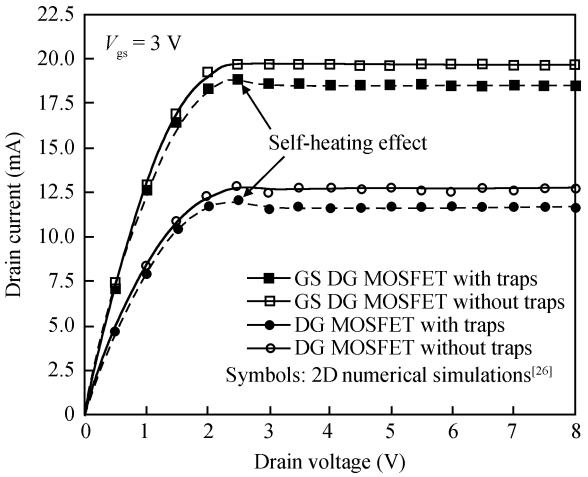

Fig. 2. I_{ds}–V_{ds} characteristics for DG and GS DG MOSFETs with and without traps.

Figures 2 and 3 show the I–V characteristics of DG and GS DG MOSFETs with and without hot-carrier stress. It can be seen that the GS DG device has higher current as compared with the DG device.

As shown in Fig. 2, a decrease of drain current above the linear regime in the case of damaged devices has been observed and this phenomenon can be explained by the channel self-heating effect caused by the presence of an interfacial charge density at the boundary contributing to the increase of coulomb scattering of electrons, which in turn leads to a decrease in the amount of heat flux passing through the interface. Such a process affects the whole thermal behavior of the device over long term work periods. In fact, other constraints can aggressively make the situation worse, such as the introduction of materials with instable thermal conductivity or the significant increase in the phonon boundary scattering generated by thin semiconductor films[22]. Since the thermal resistance R_{th} constitutes a mandatory factor in the self-heating effect, it is possible to extract from the static output characteristics such parameters and the device temperature rise as a function of temperature with the help of some additional data[23]. It should be noted that our model including the law of mobility degradation is equivalent in a simplified manner to the introduction of some thermal effects in the whole approach.

It is also clear that a reduction in the drain current can be

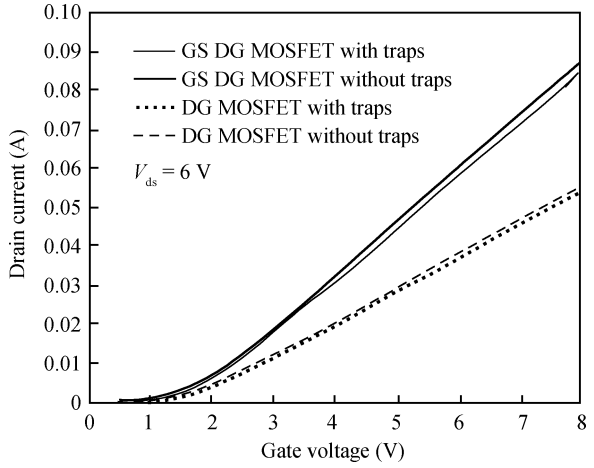

Fig. 3. I_{ds}–V_{gs} characteristics for DG and GS DG MOSFETs with and without traps.

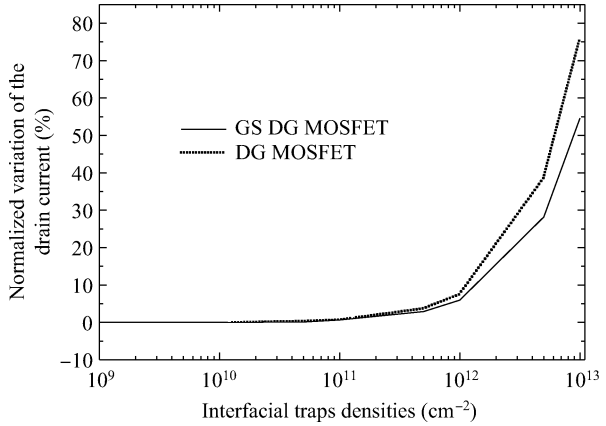

Fig. 4. Variation of the normalized drain current of the DG MOSFET as function of interfacial traps densities for both cases: with and without high-k layer ($V_{gs} = 3$ V, $V_{ds} = 4$ V).

observed in the case of damaged devices (Figs. 2 and 3) and this reduction can be explained by the effect of the trapped electrons in the damaged region on the drain current density. Moreover, the drain current degradation becomes more apparent when the gate voltage is increased to higher values. The GS DG MOSFET brings prominent advantages in terms of derived drain current and immunity against the hot-carrier degradation effect compared with conventional DG MOSFETs, which clearly implies that the GS DG design leads to a reduction in hot-carrier effects and impact ionization and, therefore, the hot-carrier reliability is considerably improved.

The comparison of both structures' performance in terms of immunity against the hot-carrier degradation can be illustrated by determining the normalized variation of the drain current, which constitutes a pertinent parameter for the characterization of such ageing phenomenon[24].

The degradation of conventional and GS DG MOSFETs as function of charge density and length of the damaged region is illustrated in Figs. 4 and 5.

As shown in Fig. 4 for several different levels of interfacial trap densities, it can be seen that the increase of charge density leads to an increase of the normalized variation of the

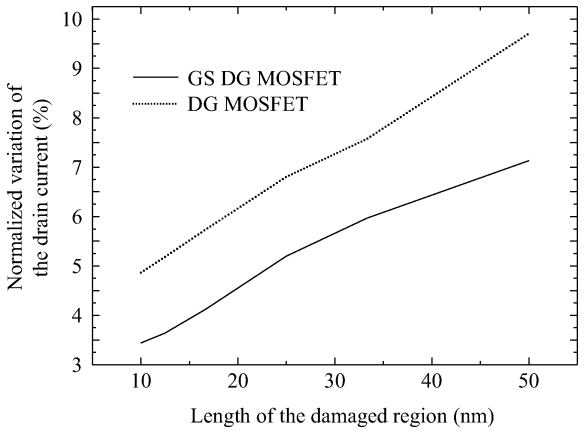

Fig. 5. Variation of the normalized drain current of the DG MOSFET as a function of the damaged region length for both cases: with and without high-k layer ($V_{gs} = 3$ V, $V_{ds} = 4$ V).

drain current in both cases. However, the drain current degradation is slower for the GS DG MOSFET structure compared with the conventional one, which confirms well our assumption regarding the immunity of the device. Based on the same parameter, the variation with the length of the damaged region follows also an increasing behavior where the GS DG MOSFET structure presents the lower vulnerability toward the hot-carrier degradation effect, as indicated in Fig. 5. The immunity of gate-stack-based devices was also demonstrated for other types of architectures[25].

5. Conclusion

In this work, original analytical models that include hot-carrier effects for symmetrical lightly doped gate-stack double-gate (GS DG) MOSFETs are presented. The models were used to study the impact of interfacial hot-carrier on the device electrical parameters such as drain current and inversion charge for GS DG MOSFETs. In addition, the proposed models inherit all the favorable features from the accurate models associated with each regime. Therefore, all the regions of operation and the transitions are correctly described without charge-sheet approximation or fitting parameters. A good match is shown between model predicted values and 2D device simulations done with similar physical effects turned on. Finally, the closed-form expressions to model various device parameters can be easily implemented into circuit simulators such as PSPICE for more accurate predictions of DG FET-based circuits.

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