Energy capability enhancement for isolated extended drain NMOS transistors

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Abstract: Isolated extended drain NMOS (EDNMOS) transistors are widely used in power signal processing. The hole current induced by a high electric field can result in a serious reliability problem due to a parasitic NPN effect. By optimizing p-type epitaxial (p-epi) thickness, n-type buried layer (BLN) and nwell doping distribution, the peak electric field is decreased by 30% and the peak hole current is decreased by 60%, which obviously suppress the parasitic NPN effect. Measured I–V characteristics and transmission line pulsing (TLP) results show that the on-state breakdown voltage is increased from 28 to 37 V when 6 V V_{gs} is applied and the energy capability is improved by about 30%, while the on-state resistance remains unchanged.

Key words: energy capability; isolated extended drain NMOS transistors; safe operating area; parasitic NPN; TLP; on-state breakdown voltage

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1. Introduction

Many mixed-signal applications require larger power-handling capabilities at higher voltages or larger currents. Discrete devices are often used to control power to motors, LCD drivers, power management, relays, lights and other energy consuming elements. Today it is necessary for power devices to be integrated into IC chips, where they work more efficiently with their control circuits. This helps us to reduce the overall system cost and size[1, 2].

The lateral DMOS (LDMOS) transistors and isolated extended drain MOS (EDMOS) transistors are often used in delivering power. In general, LDMOS transistors have the characteristics of high voltage and low on-state resistance. However, LDMOS transistors have to add at least one mask and implant step to increase the doping concentration beneath the gate and have the penalty of an increase in threshold voltage. Because EDMOS transistors feature high voltage, medium on-state resistance and low manufacturing costs, they are more suitable for handling medium power.

In a CMOS process fabricated on p-sub, if the p-body where NMOS transistors are formed is connected to p-sub, the source voltage may vary with respect to p-body, and the characteristics of NMOS transistors will change. The dependence of MOSFET characteristics (such as the gate threshold voltage V_{TH}, the device transconductance and the output impedance etc.) on the source-to-body bias V_{SB} is called the body effect which complicates the design of analog (and even digital) circuits[3, 4]. Thus, EDNMOS transistors isolated from p-sub are often essential for IC designers. If the source of NMOS is always connected to the p-body which is isolated from the p-sub, the threshold voltage remains constant and many secondary order effects derived from the source-to-body bias can be effectively eliminated.

Nevertheless, in the switching state, both high voltage and current are simultaneously present, which may lead to excessive heat dissipation and to failure of the devices. In smart-power applications, power transistors are often connected to the inductive components which must discharge their stored energy during turnoff. The energy handling capability of integrated power MOSFETs has become a limiting factor in the design and reliability of silicon smart-power ICs. The static and dynamic safe operating area (SOA) of power LDMOS transistors have been studied extensively[1, 2, 5–9], also there is a need to investigate the SOA of isolated EDNMOS transistors. For isolated EDNMOS transistors, both the lateral electric field intensity from a pwell-nwell junction and vertical electric field from a pwell-BLN junction should be considered, which is quite different from the non-isolated EDNMOS transistors.

In this paper, the simulation results of electric field, ionization rate and hole current, which activates parasitic bipolar transistors, are presented. By optimizing p-type epitaxial thickness, BLN and nwell doping concentration, electric field intensity and the hole current can be decreased, and the parasitic NPN effect can be suppressed. The devices are developed in a 0.5 μm p-epi CMOS process with BLN.

2. Device description and fabrication

Figure 1 shows a cross section of isolated EDNMOS and 5 V CMOS devices (breakdown voltage $BV_{ds} \leqslant 11$ V) used in the analysis. 5 V NMOS transistors are formed in the pwell, while 5 V PMOS transistors are formed in the nwell. In this process, 40 V extended drain PMOS, isolated EDNMOS and non-isolated EDNMOS transistors are developed simultaneously, where 20 V NPN/PNP transistors with perfect characteristics can also be achieved.

Figure 2 shows the main process flow of the proposed

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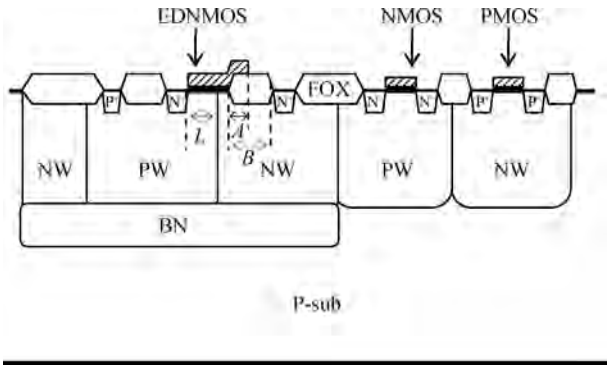

Fig. 1. Cross section of isolated EDNMOS, low voltage NMOS and PMOS transistors.

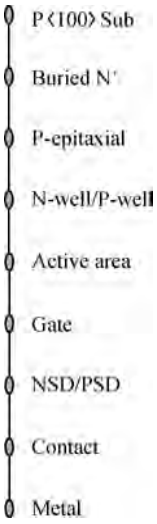

Fig. 2. Main process flow.

device. The conventional and the optimized devices are fabricated using 0.5 μm CMOS with BLN and p-type epitaxial growth on p-sub. The p-well and the n-well have been used as the drift regions of 40 V extended drain PMOS and extended drain NMOS devices respectively，without adding any other layer or process step. The highly doped BLN is used in the isolated EDNMOS transistor to isolate the p-body (p-well) from the p-sub so that the source and p-body of the isolated EDNMOS transistor can be connected together, while BLN is not used in the non-isolated EDNMOS device.

The isolated EDNMOS device is an n-type isolated transistor with a field oxide in the drift regions. The key electrical parameters of the devices are the threshold voltage V_{TH}, the on-resistance R_{ON} (measured at $V_{gs} = 5$ V, and $V_{ds} = 0.5$ V), the on-state breakdown voltage V_{bdon} and the off-state breakdown voltage V_{bdoff}. The critical dimensions for the isolated EDNMOS transistor are channel length $L = 3$ μm, poly overlap field oxide $A = 2$ μm and drift region $B = 3$ μm (Fig. 1).

The thin gate oxide is 20 nm and the field oxide is 500 nm respectively. The fabrication process after epitaxial growth is the same as for conventional CMOS.

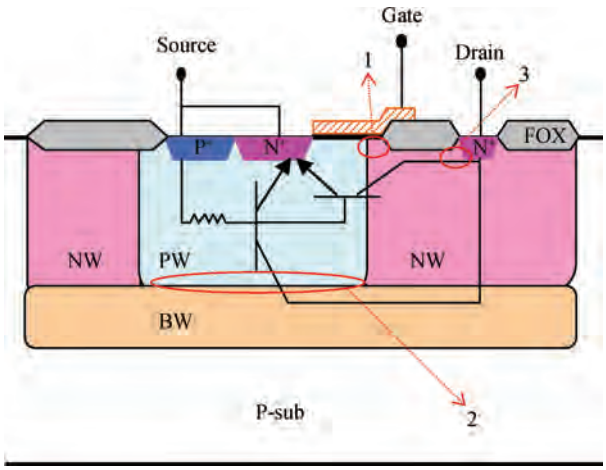

Fig. 3. Cross section of the isolated EDNMOS device containing the parasitic lateral and vertical NPN transistor effect. 1, 2, and 3 indicate high electric field regions to induce hole current.

3. Parasitic NPN effect of an isolated EDNMOS transistor and its suppression

In general, catastrophic failure of a power MOSFET is due to the triggering of the intrinsic bipolar transistor by excess carriers, being generated electrically (avalanche) or thermally. When the voltage drop is above 0.6 V in the base region, a portion of the parasitic NPN transistor will be turned on. Because of the high avalanche breakdown voltage V_{av}(> 25 V) of the isolated EDNMOS transistor and high power dissipation at the reverse-biased collector-base junction, the second breakdown voltage V_{t2} is usually smaller than the avalanche breakdown voltage V_{av}. Once a portion of parasitic NPN transistor turn-on is initiated, it must handle a higher injection current until the second breakdown phenomenon takes place while the rest of the parasitic NPN transistor has not been turned on. So efforts must be taken to prevent the turn on of the parasitic NPN transistor[2, 10].

In the isolated EDNMOS device in Fig. 3, the voltage drop V_b in the p-body (p-well) is given by

$$V_b = R_b I_{gen} = R_b (M-1) I_p, \tag{1}$$

where R_b is the resistance in the base region, I_{gen} is the base current, M is the avalanche multiplication factor and I_p is the drain current.

V_b is linear with base resistance R_b. As the threshold voltage V_{TH} of all types of NMOS device (EDNMOS included) is dependent on the pwell (i.e., the base of the parasitic NPN) concentration, the effect of suppressing parasitic NPN by reducing the base resistance R_b is limited.

Avalanche multiplication factor M can be described in terms of the impact ionization of the impact ionization coefficient, which is given by

$$M = \frac{1}{1 - \int_0^{x_d} \alpha \mathrm{d}x}, \tag{2}$$

where x_d is the width of the depletion region, and α is given by

$$\alpha = A \exp \frac{-B}{E}, \tag{3}$$

where A and B are constants and E is the electric field in the high field region. E will vary across the depletion region for a weak avalanche.

Empirically, M has been described as[11]

$$M = \frac{1}{1-(V_{\rm j}/V_{\rm av})^n}, \tag{4}$$

where $V_{\rm av}$ is the avalanche breakdown voltage and n is a fitting parameter ranging from 2 to 6 depending on the type of junction being considered. M and the generated hole current increase sharply as the applied voltage $V_{\rm j}$ approaches $V_{\rm av}$. As the avalanche breakdown voltage $V_{\rm av}$ is dependent on electric field, the hole current generated by the electric field is more influential on the turn on of the parasitic NPN.

Electrons injected from the source into the substrate are collected at the drain and a lateral NPN (LNPN) is formed with the drain as the collector, the source as the emitter and the substrate as the base. At the same time, electrons are also collected at the BLN and a parasitic vertical NPN (VNPN) is formed with the same emitter and base, but the BLN as the collector (Fig. 3). The high electric field region from which the avalanche carriers may come will depend on the electric field intensity of the region (region 1 near the pwell-nwell junction or region 2 near the pwell-BLN junction in Fig. 3).

As $V_{\rm gs}$ increases, the current density (mostly electron drift current) in the drain region increases, leading to a corresponding increase in electron density. Eventually the electron density reaches a point where it is equal to the nwell donor concentration. Further increases develop a net negative charge within the drain region. As this charge increases, the field must increase at the drain contact (i.e., high electric field region 3 in Fig. 3). Eventually, a significant hole current is generated at the drain and a point is reached where snapback occurs, which is called the Kirk effect as same as LDMOS[12]. The hole current induced by the Kirk effect can be controlled by enlarging the drift region, which may enhance the on-resistance $R_{\rm ON}$. Increasing doping of the nwell results in the increase of the electronic field of the pwell–nwell junction, while it also decreases the Kirk effect[12].

In the conventional process of a 0.5 μm p-epi CMOS process with BLN, the epitaxial layer thickness and the BLN concentration are chosen so that a 20 V NPN transistor with good characteristics can be developed. The conventional BLN doping concentration is of the order of 10^{18} cm^{-3} and the typical sheet resistance is about 60 Ω/□. The BLN should have sufficient doping to reduce the collector series resistance of 20 V NPN. A thinner epitaxial thickness reduces the collector–emitter breakdown voltage but benefits the collector–emitter saturation voltage. Thicker epitaxial thickness may increase the collector–emitter saturation voltage. Moreover, if the thickness is increased by 25% over the conventional one, it is possible that the originally isolated pwell may be connected to the p-sub and then the isolated EDNMOS transistor becomes a non-isolated EDNMOS transistor.

When the relationship of peak electric field and impact ionization rate with p-epi thickness is studied, the BLN doping is in conventional value. The p-epi thickness is measured in relative units: 100% refers to the conventional value. It is clear that when the thickness of the p-epi is increased by 20%, the peak electric field of the pwell–BLN junction is decreased by 13% and the impact ionization rate is decreased by 60%.

Table 1. Simulated peak electric field and impact ionization rate versus p-epi thickness and BLN doping ($V_{\rm gs}$ = 6 V, $V_{\rm ds}$ = 35 V).

P-epi thickness	BLN doping	Peak electric field (10^5 V/cm)	Impact ionization (10^{25} cm^3/S)
100%	Conventional	3.18	2.14
110%	Conventional	3.05	1.06
120%	Conventional	2.78	0.89
Conventional	10%	2.53	0.0919
Conventional	50%	2.95	0.915
Conventional	100%	3.18	2.14

When the effect of peak electric field and impact ionization rate on BLN doping is investigated, p-epi thickness is a conventional value and the BLN implant doses are varied from 10% to 100% of the conventional value. From Table 1, it can be seen that as the BLN doping concentration is decreased by 1 order of magnitude, the peak electric field is reduced by about 20%. But this has the penalty that the collector–emitter saturation voltage of the NPN transistor is increased. The dual-step implant with different BLN doses can be used to keep the collector–emitter saturation voltage of the NPN unchanged and the peak electric field reduced.

4. Simulation results of SOA characteristics

Figure 4 shows the electric field contours of the conventional and eventually optimized isolated EDNMOS transistor when 6 V is applied to the gate and 35 V is applied to the drain. From TCAD simulations, there is a high electric field region in the conventional isolated EDNMOS transistor. It is right around the buried layer. By optimizing the p-epi thickness, the BLN concentration and the junction profile of the pwell–BLN junction, the peak electric field in the optimized EDNMOS transistor is decreased to about 2.3×10^5 V/cm, while the peak electric field of the conventional one is about 3.2×10^5 V/cm. It reveals that the electric field intensity near the BLN of the optimized one is reduced by 30% compared to that of the conventional one. The lowering of electric field has a good effect on SOA characteristics.

Figure 5 shows the carrier generation rate by impact ionization of the conventional EDNMOS transistor and the optimized one. The impact ionization of the optimized isolated EDNMOS transistor near the BLN is reduced by 2 orders of magnitude, compared with that of the conventional one.

The impact ionization rate is distributed all over the n-type drift region after optimization, which results in the reduction of the generation of the hole current. Figure 6 shows that the peak hole current of the optimized isolated EDNMOS transistor is decreased by 60% (from 2200 to 900 A/cm^2), compared with the conventional one. The smaller hole current makes parasitic NPN operating difficult and enhances SOA characterics.

5. Measurements and discussion

After optimizing of the p-epi thickness, BLN and nwell doping, the key electric parameters remain unchanged except

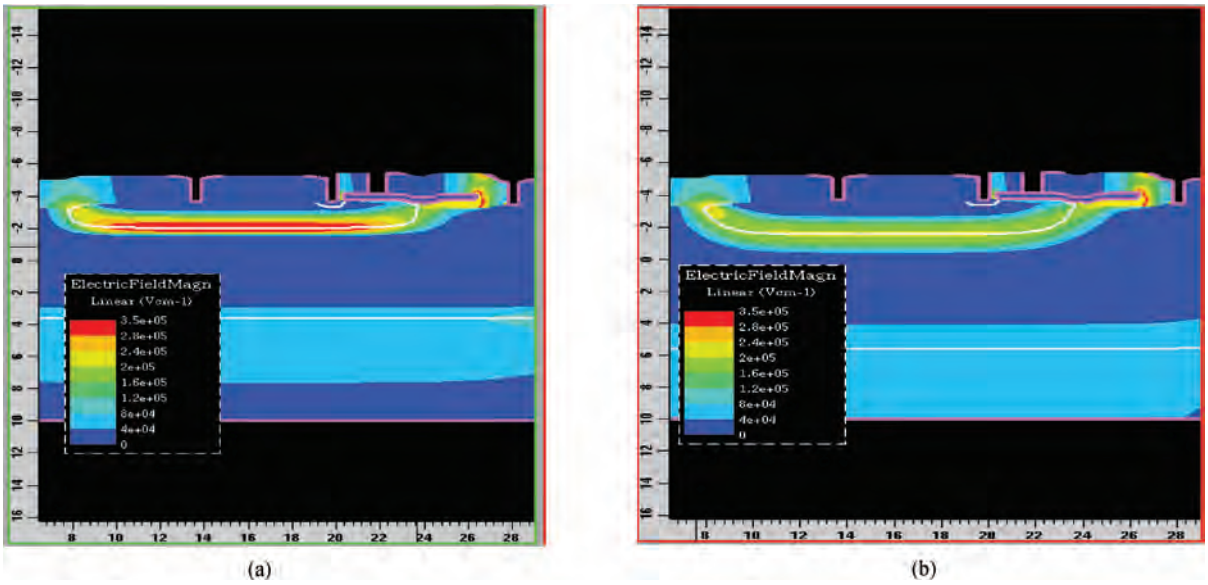

Fig. 4. Electric field of (a) the conventional isolated EDNMOS transistor and (b) the optimized one at $V_{gs} = 6$ V, $V_{ds} = 35$ V.

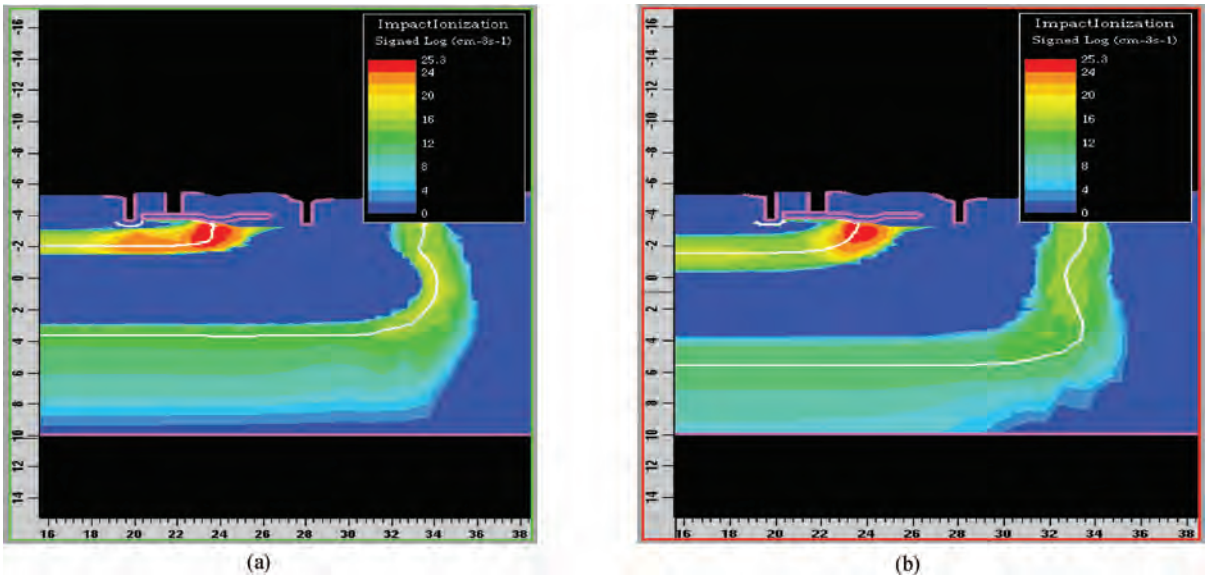

Fig. 5. Impact ionization rate of (a) the conventional isolated EDNMOS transistor and (b) the optimized one at $V_{gs} = 6$ V, $V_{ds} = 35$ V.

for the collector–emitter saturation voltage of the NPN transistor. For the NPN transistor with an area of 30 × 30 μm^2, the collector–emitter saturation voltage is increased from 0.5 to 0.6 V (measured at $I_b = 0.5$ mA and $I_c = 5$ mA). For both isolated EDNMOS transistors, measured threshold voltage V_{TH} is 0.75 V, and on-state resistance R_{ON} is 220 mΩ·mm^2 (measured at $V_{gs} = 5$ V, $V_{ds} = 0.5$ V). It can be noted that the off-state breakdown voltage V_{bdoff} of the optimized device increases from 38 V of the conventional one to 43 V.

To verify the ability to suppress the parasitic NPN of the conventional and the optimized isolated EDNMOS devices, the parameter analyzer HP4155B is used to measure I–V output characteristics. The measured DC I–V curves of both EDNMOS devices with a channel width of 20 μm and length of 3 μm under different V_{gs} are shown in Fig. 7. When 4 V V_{gs} is applied, the on-state breakdown voltage of the optimized EDNMOS is increased to 39 V, which is 26% bigger than the 31 V of the conventional one. When 6 V V_{gs} is applied, the on-state breakdown voltage of the optimized one is increased to 37 V, which is 32% bigger than the 28 V of the conventional one.

As DC-characterization causes strong self-heating at higher currents and does not address transient behavior, pulsed characterization techniques are necessary. The TLP system provides a single and continually-increasing-amplitude to the device under test. In order to indicate the triggering of parasitic NPN, 100 ns-TLP experiments are performed.

Figure 8 gives schematics of the isolated EDNMOS devices under TLP at wafer level. The gate is externally biased by a Keithley 2004 power supply. A 10 nF capacitor is used between the gate and the source needles in order to stabilize the gate voltage, while a 10 kΩ resist between gate and the source is placed to prevent excessive current. Pulse rise time is 2 ns. Figure 9 shows the TLP waveforms of these two types of isolated EDNMOS devices. During the TLP test, a 100 ns

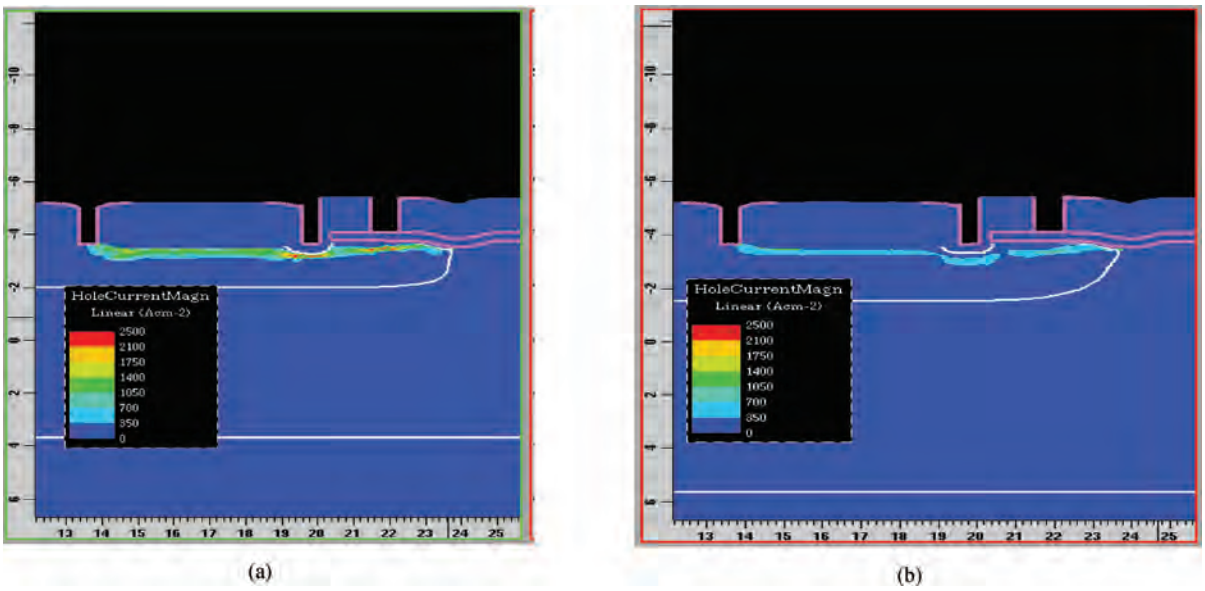

Fig. 6. Hole current of (a) the conventional isolated EDNMOS transistor and (b) the optimized one at $V_{gs} = 6$ V, $V_{ds} = 35$ V.

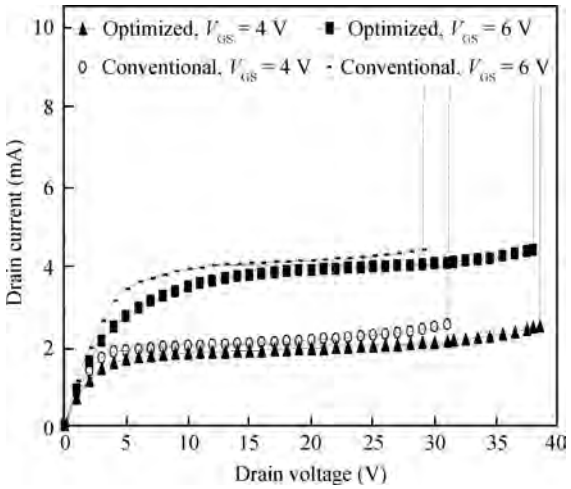

Fig. 7. The measured I–V characteristics of the conventional and the optimized isolated EDNMOS transistor. The gate width/length = 20 μm/3 μm.

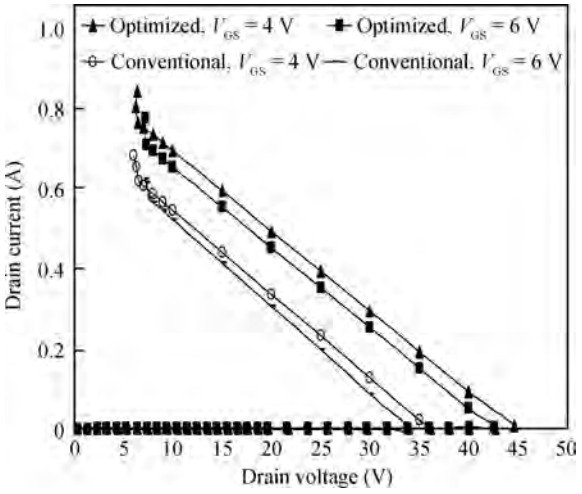

Fig. 9. TLP measured I–V curves of the conventional and the optimized isolated EDNMOS transistor. The gate width/length = 20 μm/3 μm.

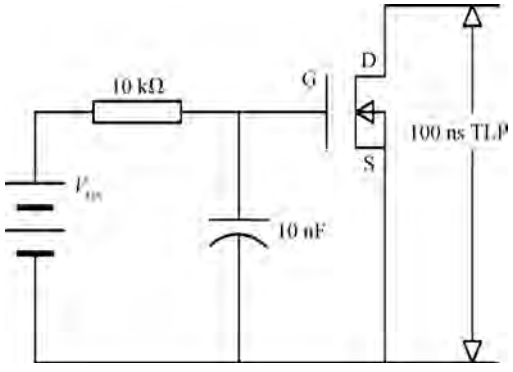

Fig. 8. Schematics of the device under TLP at wafer level.

current pulse is injected into the drain of the device. The gate width and length of both devices are 20 μm and 3 μm. From the TLP results, it can be seen that the first snapback voltage is increased from 34 to 44 V when 6 V V_{gs} is applied, which means that the energy capability can be increased by 30% for the optimized one. The measured key electric parameters for the two types of isolated EDNMOS devices are summarized in Table 2.

Table 2. Measured key electric parameters for the two types of isolated EDNMOS devices (V_{bdon} is measured at $V_{gs} = 6$ V).

Parameter	Conventional EDNMOS	Optimized EDNMOS	Relative variation
V_{bdoff} (V)	38	43	13.2%
V_{bdon} (V)	28	37	32.1%
R_{ON} (mΩ·mm^2)	220	220	0
V_{TH} (V)	0.75	0.75	0

6. Conclusions

By optimizing the p-epi thickness, the BLN concentration and the junction profile of the pwell-BLN junction, an optimized isolated EDNMOS device is achieved. TCAD simulation results show that the peak electric field intensity is decreased by 30%, the impact ionization near BLN is reduced by 2 orders of magnitude and the peak hole current generation is decreased by 60%, compared with the conventional one. These two types of EDNMOS devices are developed in a 0.5 μm p-epi CMOS process with BLN. The I–V characteristics measured by the parameter analyzer HP4155B show that the on-state breakdown voltage is increased from 28 to 37 V when 6 V V_{gs} is applied. TLP experiments at wafer level show that the energy capability is increased by 30%, while other key electric parameters (such as threshold voltage V_{TH} and on-state resistance R_{ON}) remain unchanged. And the optimized process has been used as the nominal process to fabricate isolated EDNMOS transistors with improved energy capability in a leading analog IC foundry of China.

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