Design of a low noise distributed amplifier with adjustable gain control in 0.15 μm GaAs PHEMT*

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Abstract: A low noise distributed amplifier consisting of 9 gain cells is presented. The chip is fabricated with 0.15-μm GaAs pseudomorphic high electron mobility transistor (PHEMT) technology from Win Semiconductor of Taiwan. A special optional gate bias technique is introduced to allow an adjustable gain control range of 10 dB. A novel cascode structure is adopted to extend the output voltage and bandwidth. The measurement results show that the amplifier gives an average gain of 15 dB with a gain flatness of $\pm$1 dB in the 2–20 GHz band. The noise figure is between 2 and 4.1 dB during the band from 2 to 20 GHz. The amplifier also provides 13.8 dBm of output power at a 1 dB gain compression point and 10.5 dBm of input third order intercept point (IIP3), which demonstrates the excellent performance of linearity. The power consumption is 300 mW with a supply of 5 V, and the chip area is 2.36×1.01 mm^2.

Key words: distributed amplifiers; low noise; adjustable gain control; GaAs PHEMT
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1. Introduction

With the rapid development of wireless and optical communications, the continuous increase of data transfer rates requires a higher bandwidth for amplifiers. Wideband amplifiers are the critical building blocks of broadband transceivers and the essential components of wireless communication networks[1]. Distributed amplifiers (DAs) provide an effective solution to extending the bandwidth and therefore are widely used in the design of ultra-high broadband systems.

The concept of DAs was initially proposed in 1937 by Percival[2]. In 1950, it was implemented by Horton for the first time[3]. With the development of semiconductor processes, the bandwidth of DAs is pushed to a higher bandwidth limit. III–V HEMT/PHEMT devices show a high transconductance that leads to very high frequency and low-noise performance, which makes it suitable for the design of ultra-band LNAs. In recent years, much research into III–V HEMT/PHEMT distribution amplifiers was reported. Jiao *et al.*[4] designed a distributed amplifier fabricated with 0.5-μm GaAs PHEMT which shows a 12 dB gain in the near 20 GHz band and the noise figure (NF) varies from 3.03 to 6.5 dB. Reference [5] gives a low noise distributed amplifier fabricated with composite channel $Al_{0.3}Ga_{0.7}N/Al_{0.05}Ga_{0.95}N/GaN$ HEMTs (CC-HEMTs), of which the associated gain is more than 7 dB and the gain ripple is less than 1 dB in the frequency range of 2 to 10 GHz, while the noise figure is less than 5 dB in the 2 to 6 GHz frequency range.

This paper presents a low noise distributed amplifier with an AGC (adjustable gain control), which consists of 9 gain cells. The chip is fabricated with 0.15-μm GaAs PHEMT technology from Win Semiconductor of Taiwan. A novel cascode structure is introduced to extend the output voltage and bandwidth. A special optional gate bias technique is used to allow an adjustable gain control range of 10 dB. The measurement results show that the amplifier gives an average gain of 15 dB with a gain flatness of $\pm$1 dB in the 2–20 GHz band. The noise figure is typically 2.6 dB and less than 4.6 dB during the 2 to 20 GHz band. The amplifier provides 13.8 dBm of output power at a 1 dB gain compression point and 10.5 dBm of IIP3, which demonstrates the excellent performance of linearity. The power consumption is 300 mW with a supply of 5 V, and the chip area is 2.36×1.01 mm^2. The excellent performance makes it suitable for telecom infrastructure microwave radio and VSAT, military and space, test instrumentation and fiber optics applications.

2. Principle of distribution amplifier in PHEMT process

Transmission line theory is the basis of the design of DAs. In DAs, the input and output capacitances of the transistors are combined with lumped inductors to form artificial transmission lines according to

$$Z_0 = \sqrt{\frac{2L}{C}}, \tag{1}$$

where Z_0 is the characteristic impedance of the artificial transmission lines.

In this way the gain-bandwidth product of an amplifier may be increased greatly.

Normally, the phase delays of the input and the output transmission lines are typically matched to maximize the gain of the amplifier. Therefore, the currents generated by the individual gain cells can be added constructively at the output of

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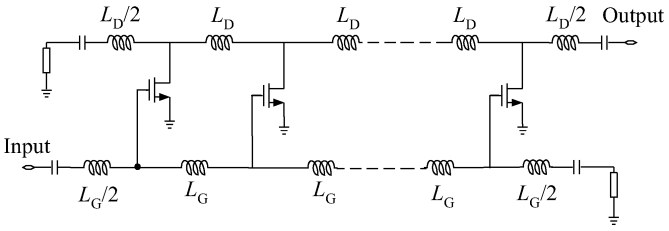

Fig. 1. Classical distributed amplifier.

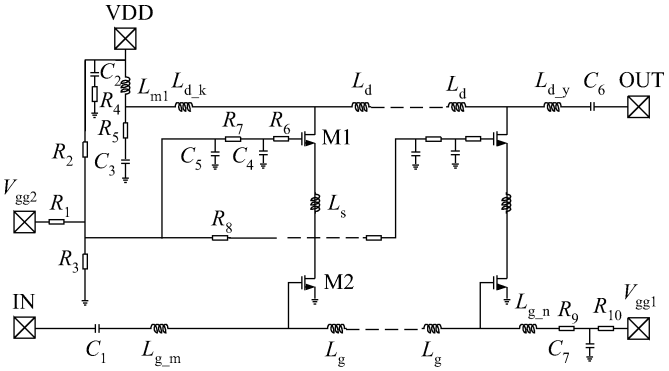

Fig. 2. The designed distributed amplifier with 9 cascode stages.

the amplifier. Assuming that the transmission lines are lossless, the low-frequency gain of a 1-D DA can be estimated by

$$A_v = \frac{1}{2} n g_m Z_0, \tag{2}$$

where n is the number of the distributed stages, g_m represents the transconductance of each stage, and Z_0 is the characteristic impedance.

Figure 1 shows the simplified schematic of a classical DA. The inductances of the gate line are given by its characteristic impedance and the gate–source capacitance:

$$L_b = \frac{Z_{0G}^2 C_{GS}}{2}. \tag{3}$$

The cut-off frequency of the gate line can be expressed by

$$f_c = \frac{1}{2\pi\sqrt{L_G C_{GS}}}. \tag{4}$$

The characteristic impedances and cut-off frequency of the drain line can be calculated analogically.

3. Circuit design

The designed DA is shown in Fig. 2. The small-signal equivalent circuit model of the transistors between the gate and source, drain and source for PHEMT can be described by the shunt of a resistance and a capacitance, which form the gate and drain transmission lines together with the on-chip inductors (L_d, L_{d_k}, L_{d_y}, L_g, L_{g_m} and L_{g_n} in Fig. 2). The values of the inductors L_d and L_g can be calculated approximately according to Eq. (3), which are 205 pH and 230 pH respectively. The inductors L_{d_k}, L_{d_y}, L_{g_m} and L_{g_n} are designed for impedance matching at the end of transmission lines, and they are fabricated with metal interconnection and verified by

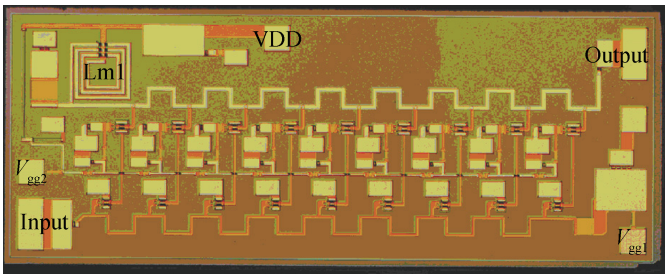

Fig. 3. Die photograph.

electromagnetism simulation. R_2 and R_3 make up a voltage divider to provide the gate bias of M1. R_5 combined with C_3 works as the absorbing load of the drain line. Two RC low-pass filters are in series in the gate of M1 to further improve the noise performance. Also, the combinations of R_9, R_{10} and C_7 comprise the absorbing load of the gate line, which provides the bias path while filtering the noise in low frequency.

In a lossless system, increasing the number of stages is a good choice to get higher gain. However, the system definitely suffers loss, and the attenuations of gate line together with drain line also increase at the same time. The distributed amplifiers are usually designed with 4 or 6 stages. Considering that the loss in GaAs PHEMT is much lower than that in silicon technology due to the high resistivity of the substrate, we use 9 gain cells to get a high voltage gain while maintaining a low power consumption.

In DA design, the cascode unit-cells have been used to reduce the loading of the drain line and lower gate-to-drain capacitance[6, 7]. As is well known, there are two advantages in using a cascode gain cell: (1) the output impedance of the cascode structure can be decreased at high frequency, which can compensate the loss of drain transmission line and improve the gain; (2) the Miller effect can be reduced, so the input capacitance in the common source (CS) structure will be decreased, and the bandwidth will be broadened[8]. These factors give the distributed amplifier excellent broadband performance[9].

If the two transistors are loaded by the optimum impedance, the cascode output voltage should be twice as high as that of a single transistor. However, the conventional cascode configuration does not meet these conditions since the common gate (CG) transistor's input impedance is too low to get a higher output voltage.

A novel cascode structure is adopted in our design to extend the output voltage and the bandwidth, which consists of M1, L_s and M2 shown in Fig. 2. Compared with the conventional cascode structure, the series inductor (L_s) is placed between the CS and CG transistors in each gain cell to tune out the middle pole of the cascode and to extend the output voltage as well as the bandwidth. This technique was successfully applied in the CMOS technique[10] and HBT technique[11]. It is proving to be useful in the PHEMT technique in our study. To the best of our knowledge, this is the first time that this use in the PHEMT process has been reported.

An optional voltage V_{gg2} is set which can directly influence the gate bias of M1, and it controls the forward gain of the circuit. When we need to change the forward gain of the circuit, we just give a suitable voltage signal at the port of V_{gg2}. The

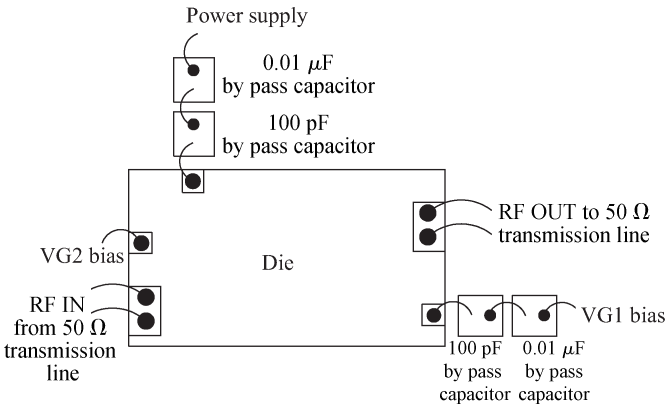

Fig. 4. Test bench.

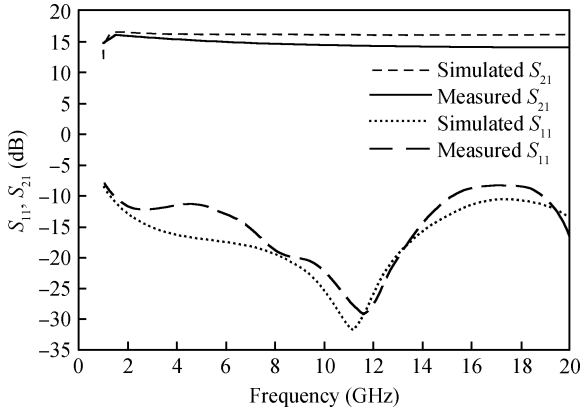

Fig. 5. Simulated and measured S_{21} and S_{11}.

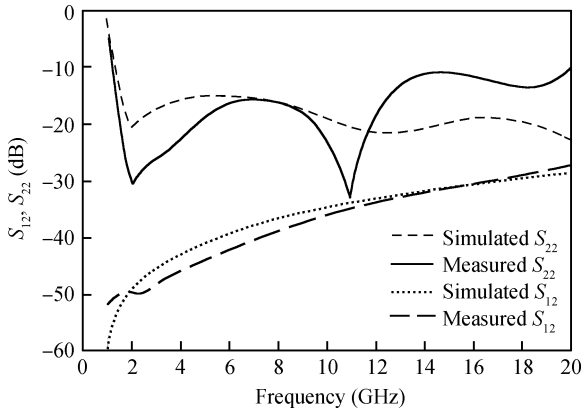

Fig. 6. Simulated and measured S_{22} and S_{12}.

circuit provides an adjustable gain control function，which can be very useful in many applications.

4. Experimental results

The photograph of the designed distributed amplifier is shown in Fig. 3. The area of the die is 2.36 × 1.01 mm^2. The circuit is measured via bonding test and the test bench is shown in Fig. 4. The measurements were carried out using an Agilent E8363B vector network analyzer and E4440A spectrum analyzer.

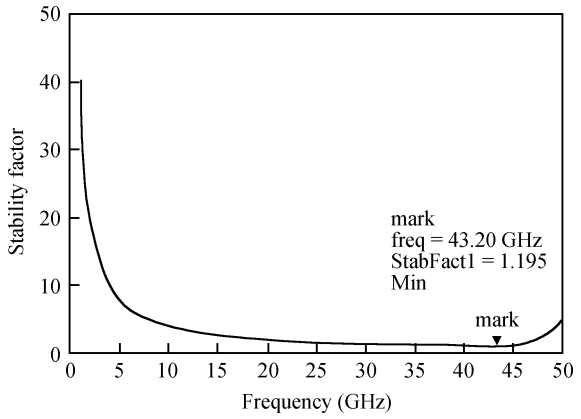

Fig. 7. Stability factor.

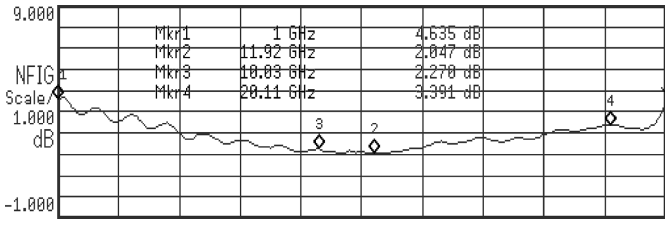

Fig. 8. Noise figure.

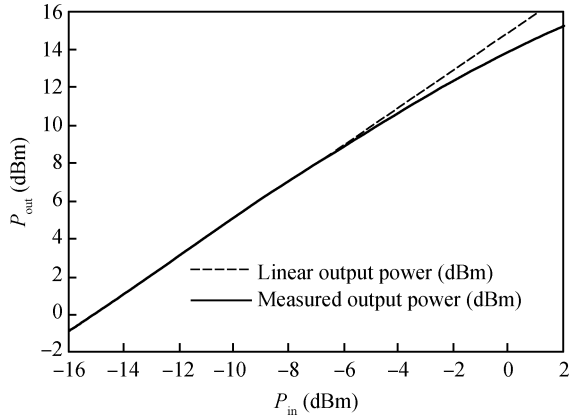

Fig. 9. Output power at frequency 10 GHz.

Figures 5 and 6 give the S parameter of the circuit. The forward gain (S_{21}) is 15 dB from 2 to 20 GHz with a gain flatness of ±1 dB. The input return loss (S_{11}) is less than –10 dB from 2 to 15 GHz and less than –8 dB from 2 to 20 GHz. In the 2 to 20 GHz band the output return loss (S_{22}) is typically less than –10 dB and the reverse isolation (S_{12}) is less than –28 dB. The measurements show excellent agreement with the simulated results. The circuit illustrates good stability during testing and its stability factor is shown in Fig. 7.

The measured noise figure curve is shown in Fig. 8. The NF is lower than 4.1 dB in the band from 2 to 20 GHz.

Figure 9 gives the output power changes with the input power at 10 GHz, and the circuit provides 13.8 dBm of output power at a 1 dB gain compression point. Figure 10 shows how the output P_{1dB} changes with the frequency. Figure 11 illustrates the two-tone test for the third order intercept point (IP3)

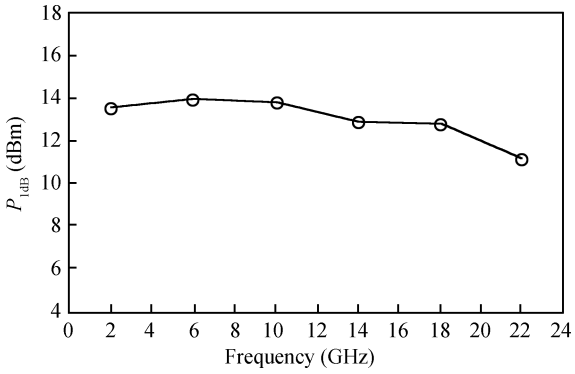

Fig. 10. Output power changes with the frequency.

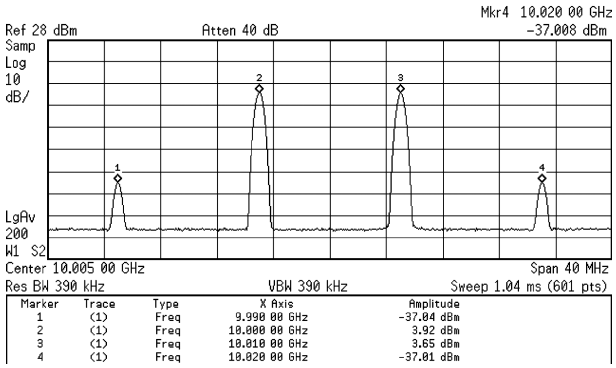

Fig. 11. IIP3 test at frequency 10 GHz.

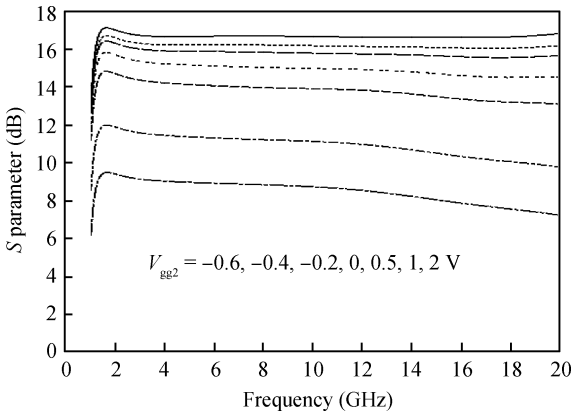

Fig. 12. Gain changes with the bias V_{gg2}.

in the frequency domain. The inputs to the amplifier are two sine waves (fundamental) with –10 dBm input power, one at 10 GHz and the other at 10.01 GHz. According to Fig. 11, an IIP3 of 10.5 dBm can be calculated by the following equation:

$$\mathrm{IIP3} = P_{\mathrm{in}} + \frac{\Delta P}{2}, \tag{5}$$

where ΔP is the difference between output power and third-order intermodulation distortion (IM3).

The adjustable gain control performance is presented in Fig. 12. We can see that the gain can be tuned from 5 to 17 dB by changing the voltage V_{gg2} from −0.6 to 2 V, which allows a typical adjustable gain control of 10 dB.

5. Conclusions

This paper presents a low noise distributed amplifier with auto-gain control function in 0.15-μm GaAs PHEMT. A novel cascode gain cell is adopted to extend the output voltage and bandwidth effectively. The circuit consists of 9 gain cells which provides a gain of 15 dB with a gain flatness of $\pm$1 dB in the 2–20 GHz band. The circuit gives a noise figure from 2 to 4.1 dB in a band of 18 GHz while providing an excellent performance of linearity. The whole circuit requires only 60 mA from a +5 V supply. The satisfied performance of the circuit makes itself ideal for many applications such as telecom infrastructure microwave radio and VSAT, military and space, test instrumentation and fiber optics among others.

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