A low power mixed signal DC offset calibration circuit for direct conversion receiver applications

Yang Lijun(杨利君)[1,†], Yuan Fang(袁芳)[2], Gong Zheng(龚正)[2], Shi Yin(石寅)[2], and Chen Zhiming(陈治明)[1]

[1]Department of Electronic Engineering, Xi'an University of Technology, Xi'an 710048, China
[2]Suzhou-CAS Semiconductors Integrated Technology Research Center, Suzhou 215021, China

Abstract: A low power mixed signal DC offset calibration (DCOC) circuit for direct conversion receiver applications is designed. The proposed DCOC circuit features low power consumption, fast settling time and a small die area by avoiding the trade-off between loop response time and the high pass frequency of the DCOC servo loop in conventional analog DCOC systems. By applying the proposed DC offset correction circuitry, the output residue DC offset voltages are reduced to less than 38 mV and the DCOC loop settling time is less than 100 μs. The DCOC chip is fabricated in a standard 0.13-μm CMOS technology and drains only 196 μA from a 1.2-V power supply with its chip area of only 0.372×0.419 mm^2.

Key words: mixed signal DC offset calibration; analog to digital converter; digital control logic unit; digital to analog converter; least significant bit

DOI: 10.1088/1674-4926/32/12/125008 **EEACC:** 2570

1. Introduction

Direct conversion architecture is one of the most popular conversion architectures due to its power consumption, simple architecture and higher integration level[1]. However, this architecture has some design challenges: (1) DC offsets, (2) second order intermodulation, (3) LO leakage, self mixing, and (4) amplitude and phase mismatch[2].

As shown in Fig. 1, the signal leakage caused by the finite amount of feedthrough from the LO port to the inputs of the LNA and of the mixer is again mixed with the LO signal, producing a DC component at the baseband chain. A similar effect occurs if a large interferer from the LNA or mixer input leaks to the LO port and is multiplied by itself. Moreover, the total gain of the baseband chain is typically around 60 dB large enough to amplify the microvolt DC offset to a level that can saturate the following stages.

In addition, the third-order inter-modulation between the input signal and the DC-offset generates second-order distortions. The propagation of the amplified second-order distortion from stage to stage in the baseband chain not only degrades the signal-to-noise ratio (SNR) but also saturates circuits[3].

Among the above design challenges, the DC offset caused by device mismatch and self-mixing may corrupt the useful signal and more importantly saturate the baseband chain, and lead to second-order distortions arising from the third-order nonlinearity in a balanced baseband circuit[3, 4]. So it is necessary to apply the DC-offset cancelling circuit to eliminate the DC-offset.

In this paper, the system architecture of the proposed mixed signal DC offset calibration core including an analog-to-digital converter (ADC), digital control logic, digital-to-analog converter (DAC) is described with comparisons to conventional analog DCOC topology. The experimental results of the proposed mixed signal DCOC circuit are also shown.

2. DCOC architecture

In a conventional analog DCOC system, as shown in Fig. 2, the DCOC servo loop high pass frequency f_c is set to a very low value to keep the desired signal band intact, typically lower than 0.1% of the data rate, and can be expressed as

$$f_c = f_0 \times A\beta_0, \tag{1}$$

where f_0 is the cut-off frequency of the low pass filter in the DCOC feedback circuit, A is the forward gain of the baseband chain and β_0 is the low frequency gain of the feedback portion. If the demanded f_c is 10 kHz, f_0 is nearly 10 Hz, which requires a huge chip area occupied by the low pass filter to achieve the large RC time constant. The closed loop transfer function of the baseband path of Fig. 2 can be expressed as

$$H(s) = \frac{A(s+\omega_0)}{s + (1 + A\beta_0)\omega_0}, \tag{2}$$

where ω_0 is the corner frequency of the low pass filter. From Eq. (2), the settling time of the analog DCOC loop is determined by the time constant of $1/[(1 + A\beta_0)\omega_0]$, which can be

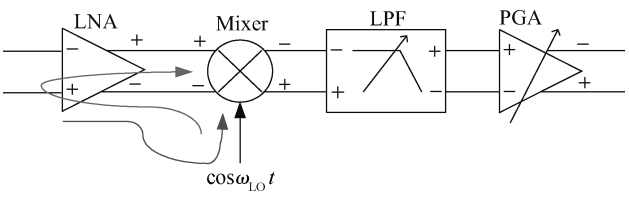

Fig. 1. Self-mixing.

† Corresponding author. Email: ljyang@sci-inc.com.cn
Received 19 July 2011, revised manuscript received 13 September 2011

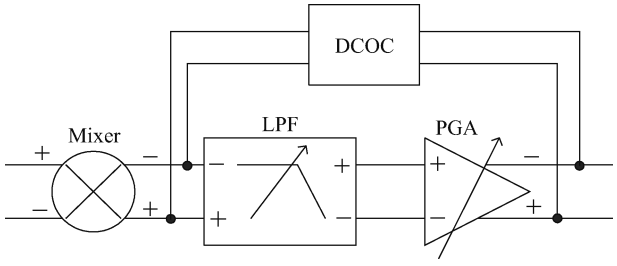

Fig. 2. Conventional analog DCOC.

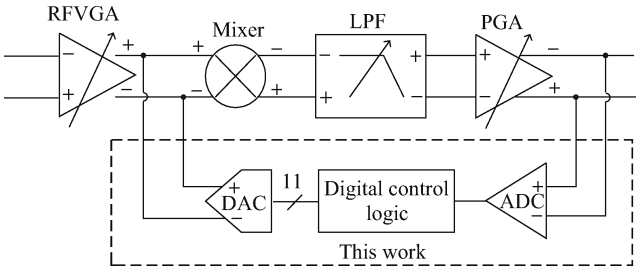

Fig. 3. A simplified schematic of the DCOC.

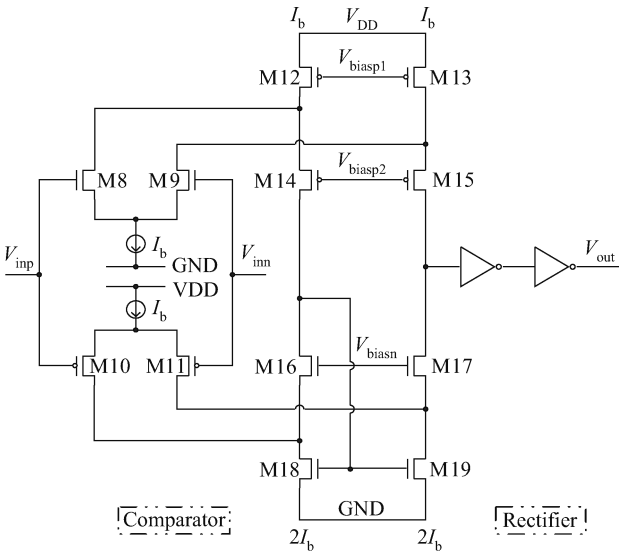

Fig. 4. Schematic of the 1-bit ADC.

very large and the response time can be quite long in proportion to the above time constant. So Equation (2) also reveals that there is trade-off between the lower band frequency of the receiver path and the response time of the DCOC loop.

In this paper, a digital calibration scheme is proposed for cancelling the DC offset in the baseband chain. Here, the critical second-order distortion issue in the analog baseband is tackled by using a mixed signal calibration mechanism. This technique benefits from low power consumption as well as a fast settling time by avoiding the trade-off between the DCOC loop response time and the lower band of the received signal faced by conventional analog DCOC topologies.

A simplified schematic of the proposed DC offset calibration circuit is shown in Fig. 3. In the analog baseband, the DC-offset calibration is carried out by the servo loop connected between the output of the baseband programmable gain amplifier (PGA), from which the tunable gain range is from 5 to 55 dB and the input of the mixer. The servo loop includes an ADC, the digital control logic and a DAC.

The DCOC system consists of a 1-bit analog to digital converter (ADC), a digital control logic and an 11-bit digital-to-analog converter (DAC). The ADC samples the DC output voltage of the PGA and outputs 1 bit digital code, then the digital control logic tunes the 11-bit digital code according to the ADC output. Finally the DAC converts the digital control signal to analog current signal through this 11-bit digital code to compensate the DC offset at the mixer stage.

In the proposed scheme, the residual DC offset voltage depends on the resolution of the ADC and the LSB of the DAC. The settling time depends on the digital control method. The following sections will discuss ADC, DAC and the digital control block in detail.

2.1. ADC

DC-offset of balanced branches in the PGA can be sensed by a 1-bit voltage-mode ADC as shown in Fig. 4. The 1-bit ADC is composed of a comparator and a rectifier. The comparator compares the differential output voltages of the PGA and then the rectifier converts the output of the comparator into a 1-bit digital code. To ensure that the input transistors of the ADC work in saturated region regardless of the high input sensed DC offset level, the input of the comparator adopts complementary rail-to-rail architecture. Since the residue DC offset voltage depends on the resolution of the ADC, which depends on the gain of the comparator, the cascode structure is used and achieves a DC gain as high as 65 dB. The proposed circuit can resolve the DC offset as small as 2 mV.

2.2. DAC

Since the DC-offset calibration range and resolution depends on the full scale and LSB current of DAC, respectively, an 11-bit balanced DAC based on a sub-sectional structure is designed. The DAC converts DC error correction code from the digital control block outputs to the DC-offset correction current, which is fed back to the input of the active mixer to eliminate DC-offset. The simplified schematic of this DAC is shown in Fig. 5.

As shown in Fig. 5, for achieving low power and small chip area, the 11-bit DAC is divided into three parts: P_cells and N_cells are controlled by thermometer codes P_{bi} ($i = 0, 1, \ldots,15$) and N_i ($i = 0, 1, 2, \ldots,14$), respectively, and the two thermometer codes P_{bi} and N_i are converted from the higher 4 bits D⟨10–7⟩ and the middle 4 bits D⟨6–3⟩ of the 11 bit of the DAC input code. The N_cell_16 is controlled by binary code generated from the lower 3 bits D⟨2–0⟩ of the DAC's 11-bit code. By dividing the 11-bit DAC into three sub-sections as described above, its power consumption and chip area is greatly reduced.

For example, when D⟨10,9,8,7⟩ is set to ⟨0,0,0,0⟩, the one hot code P_{ai} ($i = 0, 1, 2, \ldots 15$) makes all switches from P_{a0} to P_{a15} open except P_{a0}, and the corresponding reference branch current 'I' is divided into 16 identical parts and flows to the node 'I_b'. Then the thermometer code N_i ($i = 0, 1, 2, \ldots 14$) control reference currents flow either to 'I_{out1}' or 'I_{out2}'. Each of the $I/16$ current steered to the N_cell_16 is further divided

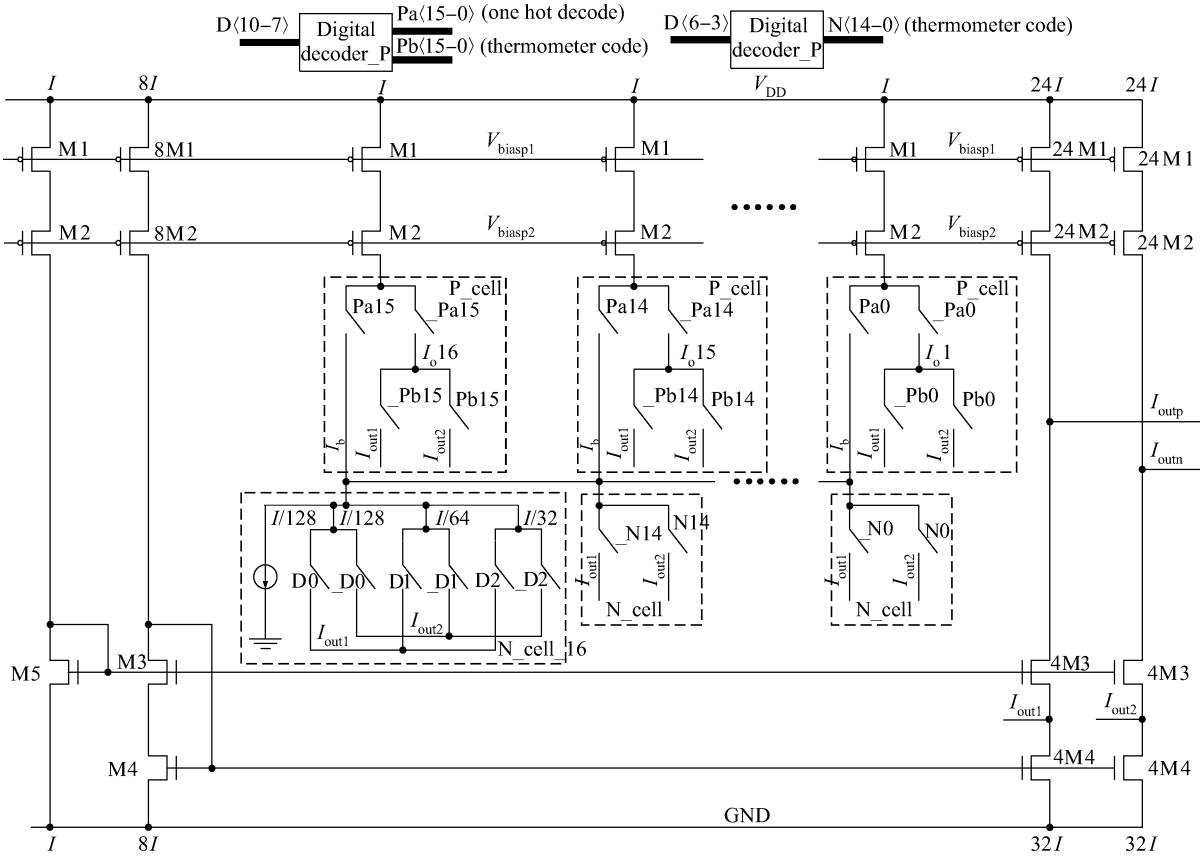

Fig. 5. Schematic of the DAC.

into 8 identical parts and the DAC lower 3-bit code decide. At the same time all switches from $\_P_{a0}$ to $\_P_{a15}$ close except $\_P_{a0}$, then the thermometer code P_{bi} ($i = 0, 1, 2, \ldots 15$) controls the corresponding reference currents flow either to 'I_{out1}' or 'I_{out2}'. By using this method, the DAC's monotonicity is guaranteed.

From the above discussion, the differential output current of the DAC is derived as follows:

$$\begin{aligned}\Delta I_{out} &= I_{out1} - I_{out2} \\ &= [(1024K_{10} + 512K_9 + \cdots + 2K_1 + K_0) - 1024]\ \text{LSB},\end{aligned} \tag{3}$$

where K_i ($i = 0, 1, 2, \ldots 10$) is the 11-bit code of the DAC and 1024 LSB $= 8I$. From Eq. (3), the tunable current range is from $-8I$ to $8I$. Initially the DAC code is set to the middle of the full range, namely: <10000000000>. At this time, the output current is fully balanced, corresponding to the status when the DC offset is very small and does not need any calibration process.

The bias circuit of the DAC is shown in Fig. 6. Since the gain of the active mixer in this paper is designed to be tunable by changing its feedback resistors, which will lead to DC-offset variation referred to the input of analog baseband and request for the individual DAC to readjust DC-offset cancellation codes corresponding to different gain of the mixer. Therefore, as shown in Fig. 6, the transistor M4 is tunable and has four steps according to the gain of the mixer. Because the drain current of the transistor M4 is constant, the gate voltage of M4 follows the changing of the size of M4. If the source voltage

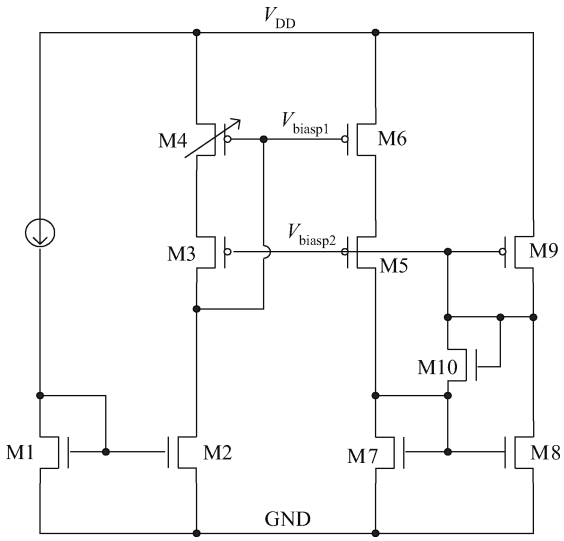

Fig. 6. Bias circuit of the DAC.

of transistor M3 were fixed, it may thus easily enter the linear region. By adopting the proposed circuit, the gate voltage of the M3 will follow the changes of the size of the transistor M4 to keep M3 in the saturation region as will be explained below.

In Fig. 6, the diode connected transistor M9 provides the bias voltage for the transistor M3. The drain current of the transistor M9, I_{D9}, changes according to the size of the M3. For example, if the size is increased, I_{D9} decreases, then the gate voltage of M3 V_{g3} (equal to V_{g9}) increases. Because the size and

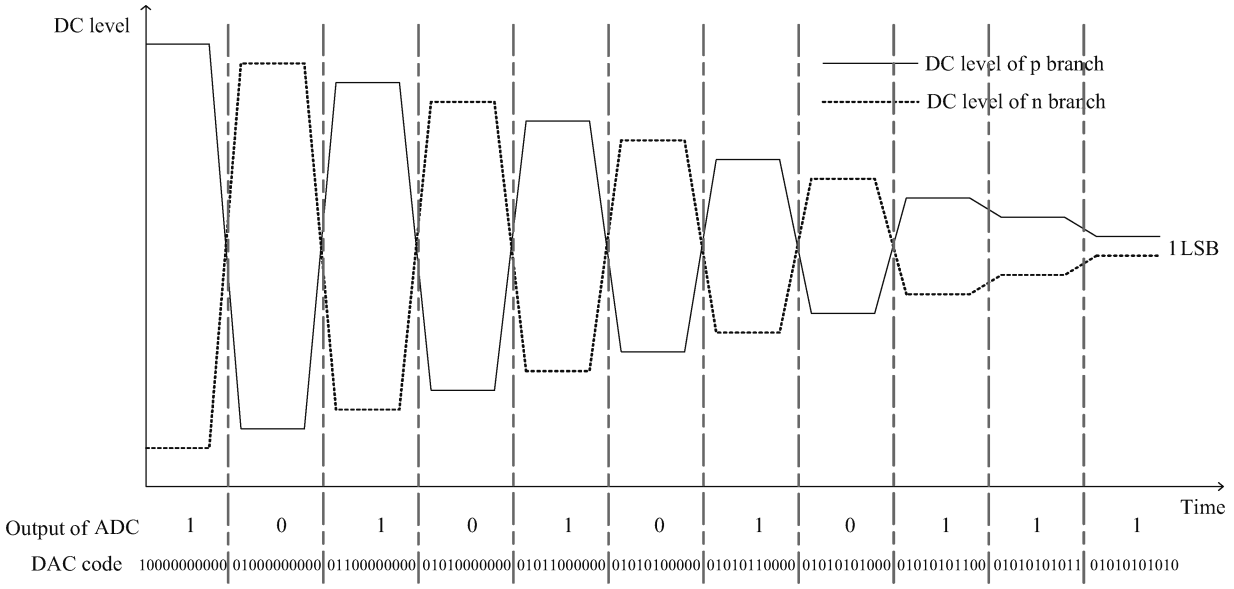

Fig. 7. Simulation result of the DCOC.

the drain current of M3 is constant, the source voltage of M3 is also increased, which makes the change of the drain–source voltage of M3 V_{ds3} acceptable, and transistor M3 works in the saturation region.

Transistor M10 forms the start-up circuit to ensure that the loop including M5, M7, M8 and M9 can start up correctly.

2.3. Digital control logic unit

The digital control logic sets the DAC output current according to the 1-bit ADC output and performs a binary and step-by-step mixed searching mechanism, which can reduce the settling time and ensure the resolution of the DCOC loop: when the output DC-offset is larger than a threshold value, the digital control logic performs binary searching mechanism, on the other hand, when the DC-offset is less than this threshold value, a step-by-step searching mechanism is performed.

Figure 7 shows an example of the DC-offset calibration procedure. Initially, the DAC input code is set to the middle as <10000000000>. Then, the output of the 1-bit ADC is '1', which means that the output DC at the 'p' branch of the PGA is much higher than that of the 'n' branch. The digital controller applies the binary searching method to adjust the 11-bit DAC code to <01000000000> to compensate more current to the 'n' branch of mixer than to the 'p' branch. After that, the output of the 1-bit ADC becomes '0', indicating that the output DC at the 'p' branch of PGA is now lower than that of the 'n' branch. The DAC input code then is reset as <01100000000> by using the digital control logic unit to compensate more current to the 'p' branch of mixer, and so on. Then, the output DC at the 'p' branch of PGA is close to that of 'n' branch, the digital control logic now performs a step-by-step searching method by successively subtracting the DAC input code by '1' at a time. When all of the eleven bits of DAC are properly set, the DC-offset of the PGA is calibrated to the minimum value limited by the LSB current of DAC, which is set to 120 μA in this design. In this example, after the calibration process, the final 11-bit DAC control code is set to <01010101010>.

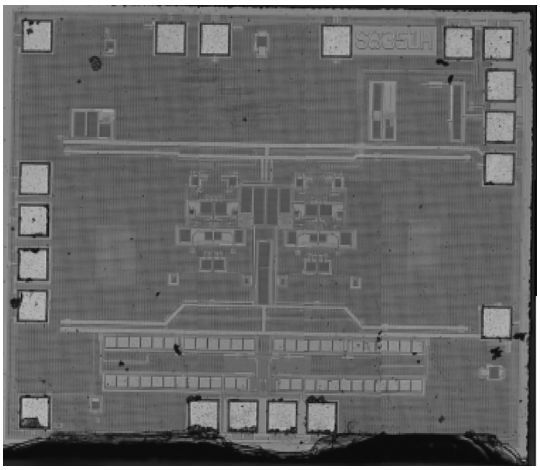

Fig. 8. Die photograph of the DAC.

In the system level, the ADC is powered down after the calibration process is finished for low power consumption and the DAC keeps active to maintain the DC offset calibration current. As a reference clock of 30 MHz is used, the time consumed by calibrating the DC-offset is only less than 1 μs in theory. To avoid interference caused by power supply spurs, the digital control logic re-calibrates 16 times to get an average value, by which the calibration accuracy is greatly improved. Moreover, the digital control logic needs to wait 1 μs every time before resetting the 11-bit DAC for the low pass filter and the PGA's transient response. Especially for the filter, auto-tuning system needs 1 μs to tune its cut frequency. In practice, different PGA gain makes the offset before calibration at the PGA outputs also different, the DC-offset calibration time therefore ranges from tens of nano-seconds to the worst case of less than 100 μs.

3. Experimental results

The die photograph of the proposed DAC circuit is shown in Fig. 8. The DAC has been implemented in a 0.13 μm

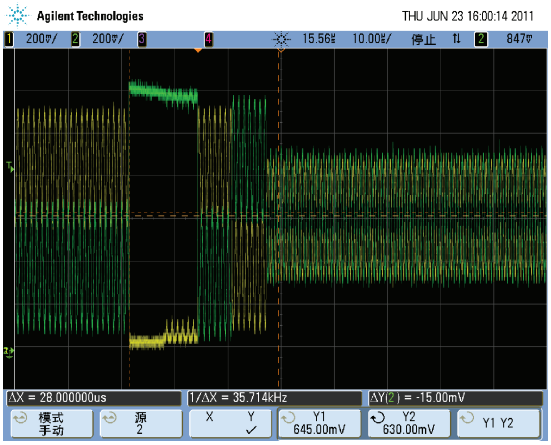

Fig. 9. Experimental transient response of the DCOC system under 30 dB of the PGA.

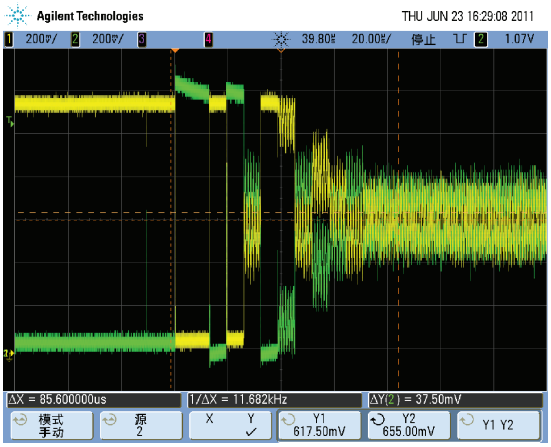

Fig. 10. Experimental transient response of the DCOC system under 55 dB of the PGA.

Table 1. Summary of the experimental results at 25 ℃.

Parameter	Experimental result
Technology	TSMC 0.13 μm
DCOC prototype	Mixed signal
Supply	1.2 V
Power drain	0.196 mA × 1.2 V
Tunable DC offset value	< 38 mV
Settling time	< 100μs
Area	0.372 × 0.419 mm^2

CMOS technology. The active area of the ADC chip is 0.372 × 0.419 mm^2. Dummy transistors are widely used for reliability purpose.

The experimental transient response of the mixed signal DC offset calibration loop with low gain and high gain of the PGA is shown in Figs. 9 and 10, respectively. As shown in Fig. 9, the initial DC offset level is 470 mV, which is reduced as 15 mV when the mixed signal DCOC is activated and the calibration time is only 28 μs. As shown in Fig. 10, the initial DC offset level of almost rail-to-rail is reduced to 37.5 mV by the proposed mixed signal DCOC calibration circuit and the calibration time is 85.6 μs.

Complete experimental results of the proposed DCOC circuit are summarized in Table 1.

Table 2. Comparison of performance with other DCOCs.

Parameter	Ref. [5]	Ref. [6]	Proposed
Technology (μm)	0.18	0.35	0.13
DCOC prototype	Mixed signal	Analog	Mixed signal
Power supply (V)	1.8	1	1.2
Power drain (mW)	11 (with PGA)	6.8–7.9 (with PGA)	0.235
Tunable DC offset value (mV)	< 100	< 17.7	< 38
Settling time (μs)	—	305	< 100

Table 2 compares the performances of the proposed mixed signal DC-offset calibration circuit with the referenced works, among which the proposed DCOC circuit has the lowest power consumption and the fastest response time.

4. Conclusion

This paper proposes a mixed signal DC offset calibration circuit for direct conversion architecture applications. The proposed DCOC architecture consists of a 1-bit analog to digital converter, a digital control block and an 11-bit digital-to-analog converter. Experimental results show that the DC offset calibration circuitry reduces the DC offset voltage to less than 38 mV with less than 100 μs settling time. The DCOC chip is fabricated in a 0.13-μm CMOS technology and drains 0.196 mA from a 1.2-V power supply. The active chip area is only 0.372 × 0.419 mm^2.

Acknowledgments

The authors would like to thank Yan Jun for his suggestions and assistance in preparation of the paper and the reviewers for their constructive comments, which resulted in numerous improvements in the manuscript, and we also thank Wen Dongmei, He Juan and Liu Cong for their help with the layout.

References

[1] Laferriere P, Rahn D, Plett C, et al. A 5 GHz direct-conversion receiver with DC offset correction. IEEE ISCAS, 2004: 267
[2] Abidi A. Direct-conversion radio transceivers for digital communications. IEEE J Solid-State Circuits, 1995, 30(12): 1399
[3] Razavi B. Design considerations for direct conversion receivers. IEEE Trans Circuits Syst Ⅱ: Analog and Digital Processing, 1997, 44(8): 428
[4] Dufrene K, Boos Z, Weigel R. Digital adaptive IIP2 calibration scheme for CMOS down conversion mixers. IEEE J Solid-State Circuits, 2008, 43(11): 2434
[5] Cheng Z S, Bor J C. A CMOS variable gain amplifier with DC offset calibration loop for wireless communications. IEEE Proc Int Symp VLSI Design, Autom and Test, 2006: 1
[6] Mak P I, Seng-Pan U, Martins R P. On the design of a programmable-gain amplifier with built-in compact DC-offset cancellers for very low-voltage WLAN systems. IEEE Trans Circuits Syst I: Regular Papers, 2008, 55(2): 496