A simplified compact model of miniaturized cross-shaped CMOS integrated Hall devices

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Abstract: A simplified compact model for a miniaturized cross-shaped CMOS integrated Hall device is presented. The model has a simple circuit structure, only consisting of a passive network with eight non-linear resistors and four current-controlled voltage sources. It completely considers the following effects: non-linear conductivity, geometry dependence of sensitivity, temperature drift, lateral diffusion, and junction field effect. The model has been implemented in Verilog-A hardware description language and was successfully performed in a Cadence Spectre simulator. The simulation results are in good accordance with the classic experimental results reported in the literature.

Key words: miniaturized Hall device; compact model; lateral diffusion; junction field effect
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1. Introduction

CMOS integrated Hall magnetic sensors have been widely applied in industrial control systems, intelligent instruments, consumer electronic products, and so on. They have demonstrated great advantages of high reliability, compact size, high accuracy and low cost since they are easily embedded on one chip with the electrical circuits in a standard CMOS process. Unfortunately, CMOS integrated Hall sensors have low sensitivity compared with BiCMOS Hall sensors. In addition, they are very vulnerable to the variations of fabrication process, temperature drift, and package-induced mechanical stress[1]. These negative factors cause a serious offset and low frequency noise even in the absence of a magnetic field, which may be large enough to obscure the Hall signal. As a consequence, the special processing circuits with the spinning current method are widely used to eliminate offset and low frequency noise[1]. In order to facilitate the analysis of an electrical circuit with the integrated sensors, it is necessary to extract a precise simulation model which has to take into account important physical effects and the influence of materials and technological parameters on electrical characteristics. Moreover, the extracted model should be compatible with current circuit analysis software packages, such as SPICE-like simulators. In addition, the model should be accurate and simple.

With the continuous scaling down of CMOS processes, miniaturized integrated Hall device with low power, high sensitivity, and small size are urgently required. Demierre *et al.* proposed a miniaturized Hall device with an N-well implantation widow of 2.4 μm, and Janossy *et al.* developed an even smaller Hall device with an active area of about 0.1 $\times$ 0.1 μm^2 in silicon technology[2, 3]. Owing to an obvious reduction of doping level resulting from the N-well lateral diffusion, the current-related sensitivity of miniaturized Hall devices is greatly improved compared with that of conventional Hall devices. Unfortunately, miniaturized Hall devices suffer from the junction field effect more easily, which can result in a higher offset. Therefore, the simulation model for miniaturized Hall devices should be improved, which should appropriately analyze the lateral diffusion effect during the process and the junction field effect. Several previous models fail in simultaneously simulating the non-linear conductivity, the shaped-dependent sensitivity, temperature drift, lateral diffusion, etc.[4−6] Recently, a completely scalable accurate lumped-circuit model was proposed by Dimitropoulos *et al.*[7]. This model performed well in analyzing geometrical, temperature, field-dependent mobility and junction field effects for several Hall sensors. It consists of the basic components, including JFETs and current-controlled current sources. The amount of these components can be freely increased to achieve a required accuracy at the expense of computation efficiency. However, this macro model increases circuit simulation complexity. In addition, it needs an accurate JEFT device model, which cannot usually be provided by using standard CMOS technology.

In this paper, a simplified compact model for miniaturized cross-shaped CMOS integrated Hall devices is developed. The model only consists of a passive network, including eight non-linear resistances and four current-controlled voltage sources. It completely covers the following phenomena: the lateral diffusion of the N-well, the junction field effect, the non-linear conductivity effect, the geometrical effect, and temperature drift. In this work, we mainly deal with the sensors working in a weak magnetic field; accordingly, two strong magnetic-field-related effects of magneto-resistance and carriers scattering are not taken into account. The model has been implemented in Verilog-A hardware description language with only ten key

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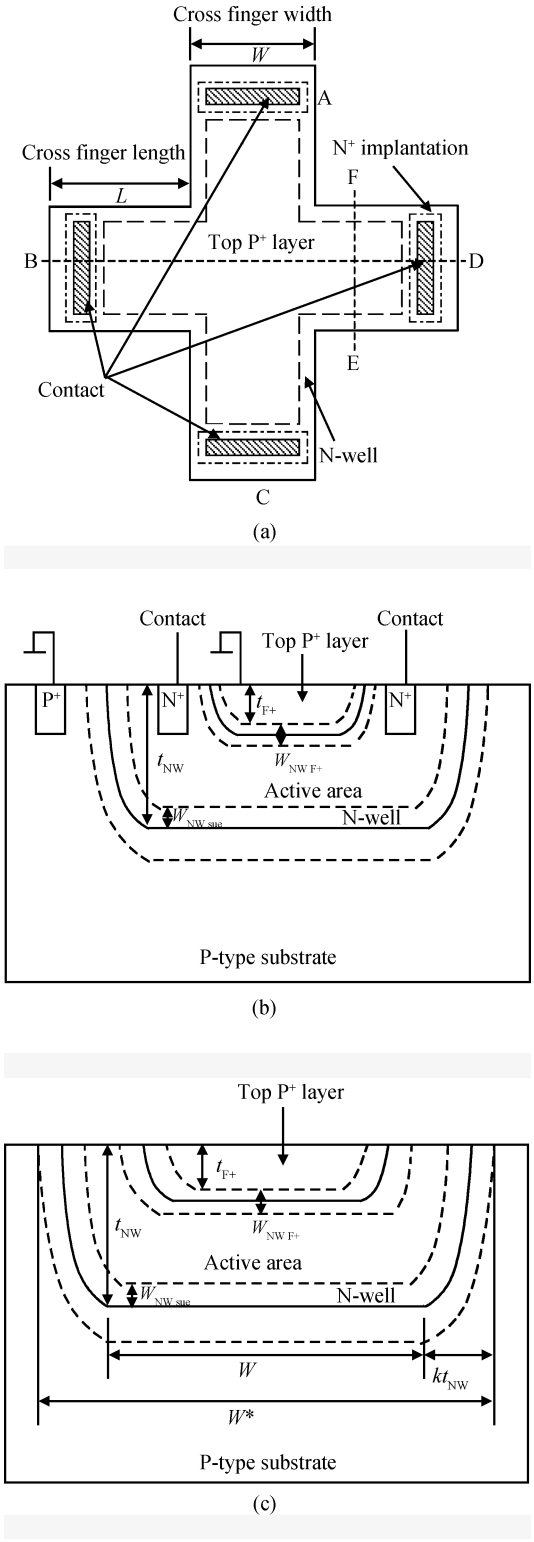

Fig. 1. Cross-shaped Hall sensor fabricated in standard CMOS technology. (a) Top view. (b) View with the cross-section along BD line. (c) View with the cross-section along EF line.

technological and physical parameters and can be conveniently used in standard SPICE-like EDA tools. It is noted that besides the cross-shaped Hall devices, the model is also suitable for other horizontal Hall devices with symmetrical shapes, such as square or diamond.

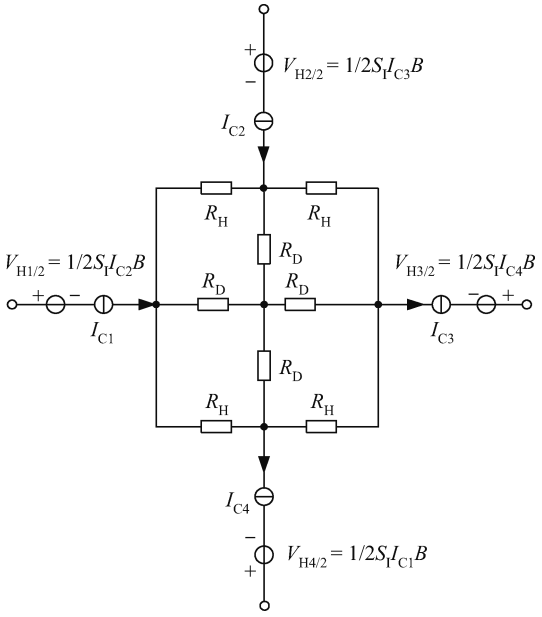

Fig. 2. A simplified model for the cross-shaped CMOS integrated Hall devices.

2. The simplified compact model

Nowadays, the cross-shaped Hall device with a 90° symmetry structure (seen in Fig. 1) has been broadly used due to its relative high sensitivity and immunity to alignment tolerances from the fabrication process[5, 6]. Here, the active area of a Hall device is usually implemented by a lowly doped N-well diffusion region which is isolated from the P-type substrate by the reverse-biased well/substrate p–n junction. In order to reduce flicker noise and surface carrier losses, a shallow highly doped P^+ conductive top layer often covers the surface of the active area. The P-type substrate and P^+ top layer are generally grounded together. In addition, there are four contact regions in the N-well, which are highly N^+ doped concentration with the source and drain formation processing step in CMOS technology.

2.1. Structure of the model

The conventional compact model is based on a 4-resistance Wheatstone bridge to model the behaviors of Hall sensors. For the 4-resistance model, the value of equivalent resistance between two adjacent contacts is not accurate since the current flowing through the two adjacent contacts does not effectively cross the central region of the device. In addition, it cannot accurately model the offset induced by the piezo-resistance effect of silicon. In contrast to the complicated Dimitropoulos model mentioned above, a simplified 8-resistance symmetric model is developed, as illustrated in Fig. 2. Here, besides the four resistances R_H on the H-bridge, the other four resistances R_D sit between the contacts of each diagonal, respectively. In addition, there are four voltage sources $V_{Hi/2}$ ($i = 1$ to 4) used to model the Hall generator. Each Hall voltage source $V_{Hi/2}$ is controlled by a current source I_{ci} ($i = 1$ to 4) flowing through the closer contact and is proportional to the perpendicular magnetic field and bias current. Here, I_{ci} as a circuit branch current measurement is a zero-voltage current source.

In order to determine the values of the two resistances $R_{\rm H}$ and $R_{\rm D}$, we skillfully combine the Van der Pauw method and the model's circuit structure[8−10]. In the Van der Pauw method, the N-well sheet resistance $R_{\rm s}$ of the Hall plate is related to one measured resistance value of $R_{\rm AB,\,CD}$ by

$$R_{\rm AB,\,CD} = \frac{\ln 2}{\pi} R_{\rm s}, \tag{1}$$

where $R_{\rm AB,\,CD} = V_{\rm CD}/I_{\rm AB}$ denotes the potential difference between contacts C and D per current flowing $I_{\rm AB}$ from contact A to contact B. The contacts of A, B, C and D are illustrated in Fig. 1(a).

Meanwhile, in terms of the model structure of the Hall plate, $R_{\rm AB,\,CD}$ can be calculated by

$$R_{\rm AB,\,CD} = \frac{R_{\rm H}}{4}\frac{2R_{\rm D} - R_{\rm H}}{2R_{\rm D} + R_{\rm H}}. \tag{2}$$

On the other hand, the internal equivalent resistance between two diagonal contacts, A and C, can be obtained according to the circuit structure of the model and the geometrical structure of the Hall device:

$$R_{\rm AC} = \frac{2R_{\rm D}R_{\rm H}}{2R_{\rm D} + R_{\rm H}} = \left(2\frac{L}{W} + \frac{2}{3}\right) R_{\rm s}. \tag{3}$$

Here, $2L/W + 2/3$ is the effective number of squares of the N-well diffusion resistance. L and W are the finger length and finger width of the cross-shaped Hall devices, respectively. The center square number of the cross-shaped Hall devices is approximately reduced to 2/3 because the two fingers for sensing Hall signal are placed in parallel. Using Eqs. (1), (2) and (3), we finally obtain

$$R_{\rm H} = \frac{2R_{\rm s}}{\pi}\left[\left(2\frac{L}{W} + \frac{2}{3}\right)\pi - 2\ln 2\right], \tag{4}$$

and

$$\frac{R_{\rm H}}{R_{\rm D}} = 2 - \frac{8}{\pi}\frac{\ln 2}{2L/W + 2/3}. \tag{5}$$

2.2. Geometry dependent sensitivity effect

When a magnetic field is orthogonally applied on the device plane and two diagonal contacts are biased with a current I or a voltage V, the Hall voltage $V_{\rm H}$ appears on other two diagonal contacts. The equation linking Hall voltage $V_{\rm H}$ with bias current and magnetic field is equal to

$$V_{\rm H} = S_{\rm I} I B, \tag{6}$$

and

$$S_I = \frac{G r_{\rm H}}{q N_{\rm D,\,NW} t_{\rm eff}}, \tag{7}$$

where $S_{\rm I}$ is defined as the current related sensitivity of the Hall device, which is determined by a geometrical correction factor G, effective thickness $t_{\rm eff}$ of the Hall device, Hall factor $r_{\rm H}$ of the majority carriers and the N-well doping concentration $N_{\rm D,\,NW}$.

For a cross-shaped Hall device, if the geometrical condition of $W/2L \leqslant 0.39$ is met, G can be calculated by following equation with accuracy better than 0.5%[11]:

$$G = 1 - 5.0267\frac{\theta_{\rm H}}{\tan\theta_{\rm H}}\exp\left(-\frac{\pi}{2}\frac{W + 2L}{W}\right), \tag{8}$$

where $\theta_{\rm n} = \tan^{-1}(\mu_{\rm H} B)$ is the Hall angle. $\mu_{\rm H} = r_{\rm H}\mu_{\rm n}$ is the Hall mobility. $\mu_{\rm n}$ is the electron mobility.

If the applied magnetic field is low, Eq. (8) can be further simplified to

$$G = 1 - \exp\left(-\frac{\pi L}{W}\right). \tag{9}$$

After considering the geometrical effect, each Hall voltage $V_{{\rm H}i/2}$ in Fig. 2 is modeled using the current-controlled voltage sources with the following equation:

$$V_{{\rm H}i/2} = \frac{1}{2} S_{\rm I} I_{{\rm C}i} B, \quad i = 1, 2, 3, 4. \tag{10}$$

2.3. Non-linear conductivity effect

The sheet resistance of the N-well dominates the important behaviors of the model, which is defined as:

$$R_{\rm s} = \frac{1}{q\mu_{\rm n} N_{\rm D,\,NW} t_{\rm eff}}. \tag{11}$$

As shown in Fig. 1(b), the effective depth of an N-well is equal to

$$t_{\rm eff} = t_{\rm NW} - t_{\rm P+} - w_{\rm NW,\,SUB} - w_{\rm NW,\,P+}, \tag{12}$$

$$w_{\rm NW,\,SUB}(U_{\rm pn}) = \sqrt{\frac{2\varepsilon_{\rm s}}{q}\frac{N_{\rm A,\,SUB}}{(N_{\rm A,\,SUB} + N_{\rm D,\,NW})N_{\rm D,\,NW}}(V_{\rm bi,\,SUB} + U_{\rm pn})}, \tag{13}$$

$$w_{\rm NW,\,P+}(U_{\rm pn}) = \sqrt{\frac{2\varepsilon_{\rm s}}{q}\frac{N_{\rm A,\,P+} + N_{\rm D,\,NW}}{N_{\rm A,\,P+}N_{\rm D,\,NW}}(V_{\rm bi,\,P+} + U_{\rm pn})}. \tag{14}$$

Here, $t_{\rm NW}$ is the depth of N-well implantation, and $t_{\rm P+}$ is the effective thickness of the top conductive layer. $V_{\rm bi,\,P+}$ and $V_{\rm bi,\,SUB}$ are the built in potential of PN junction, $V_{\rm bi,\,P+} = \frac{KT}{q}\ln\frac{N_{\rm A,\,P+}N_{\rm D,\,NW}}{n_i^2}$ and $V_{\rm bi,\,SUB} = \frac{KT}{q}\ln\frac{N_{\rm A,\,SUB}N_{\rm D,\,NW}}{n_i^2}$. $N_{\rm D,\,NW}$, $N_{\rm A,\,P+}$, $N_{\rm A,\,SUB}$ are defined as the doping concentration of the N-well, the top P^+ layer and the substrate, respectively. $w_{\rm NW,\,SUB}$ is the bottom depletion region at the N-well side between the N-well and the P-type substrate. $w_{\rm NW,\,P+}$ is the upper depletion region situated between the N-well and the top P^+ conductive layer.

It is well known that the thickness of a depletion region is obviously changed by the reverse biased PN junction voltage $U_{\rm pn}$. Therefore, the sheet resistance $R_{\rm s}$ suffers from strong voltage dependence of non-linearity. Compared with the bottom depletion region, the thickness of the upper depletion region is smaller due to the high doping of the top P^+ layer. As a result, the thickness variation of the upper depletion region induced by a negative bias voltage can be ignored. According

to Eq. (11), a Taylor expansion up to second order with Lagrange's remainder term of the third order. Since the value of the remainder term is small, it can be neglected and a simplified equation for calculating the voltage dependence of sheet resistance R_s is obtained[6, 10]:

$$\begin{aligned} R_s(U_{pn}) &= \frac{1}{q\mu_n N_{D,NW}(t^*_{eff} - \sqrt{k_1 V_{bi}})} \\ &+ \frac{1}{2}\frac{\sqrt{k_1 V_{bi}}}{q\mu_n N_{D,NW}(t^*_{eff} - \sqrt{k_1 V_{bi}})^2 V_{bi}} U_{pn} \\ &+ \left[-\frac{1}{8}\frac{\sqrt{k_1 V_{bi}}}{(t^*_{eff} - \sqrt{k_1 V_{bi}})V_{bi}^2} + \frac{1}{4}\frac{k_1}{(t^*_{eff} - \sqrt{k_1 V_{bi}})^2 V_{bi}}\right] \\ &\times \left[q\mu_n N_{D,NW}\left(t^*_{eff} - \sqrt{k_1 V_{bi}}\right)\right]^{-1} U_{pn}^2 + O(U_{pn}^3) \\ &\approx R_s(0\,\mathrm{V}) + \mathrm{BBR}_1 R_s(0\,\mathrm{V}) U_{pn} + \mathrm{BBR}_2 R_s(0\,\mathrm{V}) U_{pn}^2, \end{aligned} \tag{15}$$

where $R_s(0\ \mathrm{V})$ is the zero-biased N-well sheet resistance of a Hall device and its two reverse biased voltage coefficients are described by BBR_1 and BBR_2. $t^*_{eff} = t_{NW} - t_{P+} - w_{NW,P+}$ (0 V), and $k_1 = \frac{2\varepsilon_{si}}{q}\frac{N_{A,SUB}}{(N_{A,SUB}+N_{D,NW})N_{D,NW}}$.

Besides the Hall device resistances, the sensitivity is also subject to a reverse biased PN junction effect and can be calculated by using the same method. The current-related magnetic sensitivity is given by

$$S_I(U_{pn}) = S_I\left(1 + \mathrm{BBS}_1 \cdot U_{pn} + \mathrm{BBS}_2 \cdot U_{pn}^2\right). \tag{16}$$

Here, the coefficients of BBS_1 and BBS_2 are the first and second voltage dependence of sensitivity, respectively.

2.4. Lateral diffusion effect

Special attention should be given to the lateral diffusion effect of miniaturized Hall devices with a narrow N-Well implantation strip. Based on the N-well implantation depth and its average doping concentration $N_{D,NW}$, the N-well implantation dose using the depth of implantation t_{NW} can be estimated by[12]:

$$D_{NW} = (N_{A,SUB} + N_{D,NW})t_{NW}. \tag{17}$$

Being a miniaturized Hall device, the lateral diffusion effect of an N-well cannot be ignored. Since the lateral diffusion length is proportional to the depth of implantation, the equivalent implantation length is defined with a factor of k (see Fig. 1(c)):

$$W^* = W + 2kt_{NW}. \tag{18}$$

Here, W is the implantation width of N-well (i.e. cross finger width in Fig. 1(c)), $k \approx 0.8$ for a low doped substrate.

Considering the lateral diffusion of N-well implantation, an approximate half ellipse cross-section with area S^* in Fig. 1(c) is obtained:

$$S^* = \frac{\pi}{4}W^* t_{NW}. \tag{19}$$

From Eqs. (17), (18) and (19), the effective N-well doping level after implantation through a narrow strip can be calculated by[12]:

$$\begin{aligned} N^*_{D,NW} &= \frac{D_{NW}}{S^*}W - N_{A,SUB} \\ &= \frac{4}{\pi}\frac{W}{W^*}(N_{A,SUB} + N_{D,NW}) - N_{A,SUB}. \end{aligned} \tag{20}$$

2.5. Junction field effect

We have known that the N-well of cross-shaped Hall devices is surrounded by P-type substrate and a top P^+ layer. The active cross-section of a Hall device is obviously decreased because of the reverse biased PN junction field effect (JFE). The narrower the implantation width of a Hall device is, the more serious the junction field effect becomes. For miniaturized Hall sensors, we should first take into account the lateral diffusion effect. Therefore, the thickness of the two depletion regions in Eqs. (13) and (14) should be recalculated with the effective N-well doping concentration $N^*_{D,NW}$ instead of actual N-Well implantation doping concentration $N_{D,NW}$.

According to the Hall sensor cross-section shown in Fig. 1(c) and considering the junction field effect, the cross-section S^*_{JFE} of the N-well active area is obtained[12]:

$$\begin{aligned} S^*_{JFE} &= \frac{\pi}{4}(t_{NW} - t_{p+} - w_{NW,SUB} - w_{NW,P+}) \\ &\times (W + 2kt_{NW} - 2w_{NW,SUB}). \end{aligned} \tag{21}$$

Hence, the sheet resistance per square R_s in Eq. (11) is rewritten as:

$$R_s = \frac{1}{q\mu_n N^*_{D,NW}}\frac{W}{S^*_{JFE}}. \tag{22}$$

Accordingly, the current related sensitivity S_I in Eq. (7) is rewritten as:

$$S_I = \frac{Gr_H}{qN^*_{D,NW}}\frac{W}{S^*_{JFE}}. \tag{23}$$

2.6. Temperature effect

It is well known that Hall device characteristics, such as sensitivity, resistance of N-well and offset, are sensitive to temperature drift. The temperature behavior of N-well sheet resistance can be well approximated by the second order polynomial:

$$R_s(T, U_{pn}) = R_s(U_{pn}) \cdot \left(1 + R_{TC1}\Delta T + R_{TC2}\Delta T^2\right). \tag{24}$$

Here, $\Delta T = T - 300$ K, R_{TC1} and R_{TC2} are temperature coefficients which can be directly obtained from the foundry technology files.

Assuming the G and t_{eff} are independent on temperature, the thermal drift of current related sensitivity α_{SI} can be formulated by[11–13]

$$\alpha_{SI} = \frac{1}{S_I}\frac{dS_I}{dT} = \alpha_{rH} - \alpha_N, \tag{25}$$

where α_{rH} and α_N are the temperature coefficient of the Hall factor and the N-well carrier concentration, respectively.

Due to the combination of the temperature dependent α_{rH} and α_N, α_{SI} is about in the range of $\pm$ 500 ppm/℃ throughout

Table 1. Key model parameters (AMS CXQ 0.8 μm CMOS technology).

Parameters	Definition	Default value
$N_{D,NW}$	Doping concentration in N-well	4×10^{16} cm^{-3}
$N_{A,P+}$	Doping concentration in top P+ layer	1×10^{20} cm^{-3}
$N_{A,SUB}$	Doping concentration in substrate	1×10^{16} cm^{-3}
t_{NW}	Depth of N-well	4 μm
t_{P+}	Depth of top P+ layer	0.3 μm
μ_n	Electrons mobility	950 cm^2/(V·s)
r_H	Hall factor	1.2
R_{TC1}	Temperature coefficient of N-well	0.5 %/℃
R_{TC2}	Temperature coefficient of N-well	20 ppm/℃
α_{SI}	Temperature coefficient of S_I	±500 ppm/℃

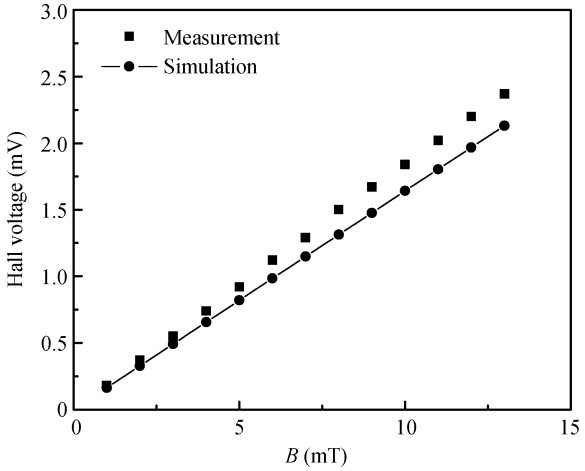

Fig. 3. The simulated and measured output Hall voltage versus magnetic field.

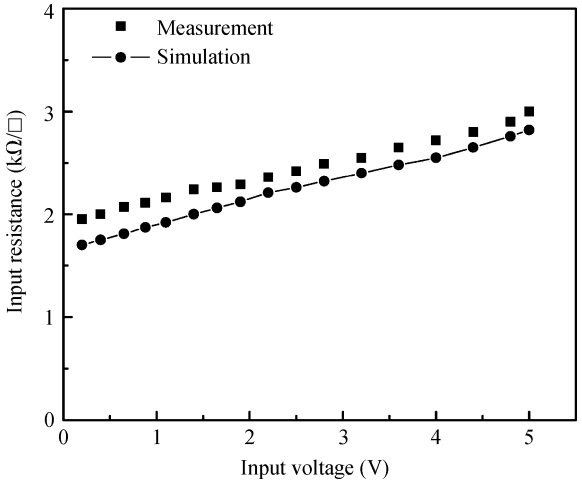

Fig. 4. Comparisons between the simulations and measurements of N-well resistance per square versus input voltage.

the industrial temperature range for a typical N-well doping concentration of 4×10^{16} cm^{-3}[13]. A zero temperature coefficient of sensitivity could be obtained near room temperature.

Considering the thermal drift effect, Eq. (16) can be rewritten as

$$S_I(\Delta T, U_{pn}) = S_I(U_{pn})(1 + \alpha_{SI}\Delta T). \quad (26)$$

3. Simulation results

The new simulation model code has been implemented in behavioral Verilog-A language, including ten key technological and physical parameters. The model simulation was performed using AMS CXQ 0.8 μm CMOS technological parameters by using a Cadence Spectre simulator. Table 1 shows the used key parameters[10−12]. For the CMOS N-well, with a doping concentration of 4×10^{16} cm^{-3}, the electrons mobility μ_n and Hall factor r_H are about 950 cm^2/(V·s) and 1.2, respectively. It is noted that the parameter of N^+ contacts with 0.3 μm thickness and 6×10^{19} cm^{-3} doping level is not included in this model. Since the N^+ contact resistance is relatively very small compared to the N-Well resistance, it can be neglected. To verify the accuracy of the model, the corresponding experimental results of cross-shaped Hall devices fabricated in the same technology are compared to the model's simulation results[11, 12].

Figure 3 shows the simulated Hall voltage versus the variations of magnetic field at room temperature. When the Hall device implantation width is 2.4 μm and the Hall device is biased with 1 mA, the simulated Hall voltage is about 0.164, 0.82 and 1.64 mV at 1, 5 and 10 mT magnetic fields, respectively. A current-related sensitivity of about 164 V/AT is obtained. In contrast to the plot of measurements, as shown in Fig. 3, this value is close to the tested value of about 185 V/AT[11, 12]. Figure 4 illustrates the simulated N-well resistance per square versus variations of input voltage for 2.4 μm implantation width. The simulated input resistance per square is increased from 1.7 to 2.8 kΩ/□ when the input voltage sweeps from 0 to 5 V. By comparison, the simulation results are approximated to the measured results shown in Fig. 4[12]. Further, a comparison of the current related sensitivity versus different input voltages between the simulated and tested results is shown in Fig. 5. We observe that the simulated current-related sensitivity increases from 150 to 180 V/AT with the input voltage increasing from 0 to 5 V. The simulation results are in good accordance with the measured results[12]. Due to the voltage dependent junction field effect, the N-well thickness is decreased with the input voltage increasing. Accordingly, the current-related sensitivity is also increased. In addition, we simulated the thermal drift of the current related sensitivity without considering packaging stress. We suppose α_{SI} linearly changes from −500 to 500 ppm/℃ in the temperature range from −40 to 110 ℃. Figure 6 shows the simulated and measured relative variation of α_{SI} (related to the value at 30 ℃) as a function of temperature.

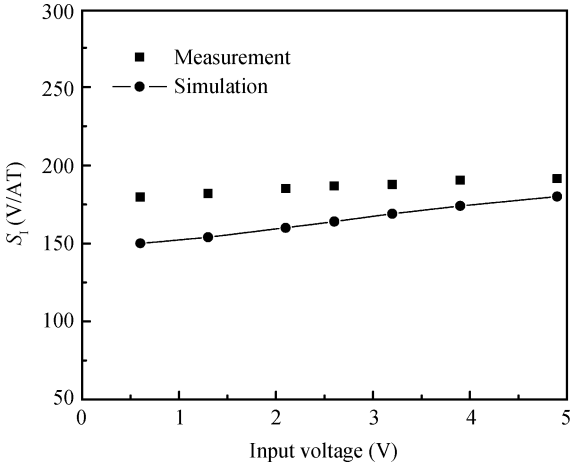

Fig. 5. Comparisons between the simulations and measurements of the current related sensitivity versus input voltage.

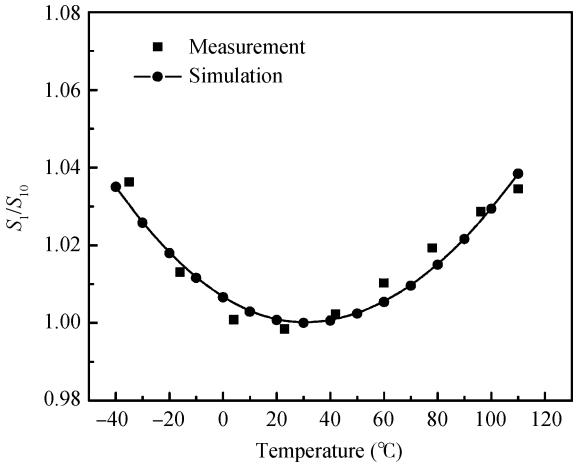

Fig. 6. Comparisons between the simulated and measured relative variation of the current related sensitivity (related to the value S_{I0} at 30 ℃) versus temperature.

It can be observed that the measured zero temperature coefficient of S_I is present at about 20 ℃, while it appears at 30 ℃ in the simulation. This is due to the zero temperature coefficient of S_I usually fluctuating within the room temperature range for the actual Hall devices. So, we use a typical value of 30 ℃ in the simulation. On the whole, the simulation and experimental results achieves consistency when Hall sensor is liberated from packaging stress[11]. Finally, the model simulations of the current related sensitivity for different implantation widths are compared, as shown in Fig. 7. It can be obviously observed that the current related sensitivity is greatly improved with a reduction in implantation width. This is because the lateral diffusion effect results in an obvious decrease in the N-well doping concentration. For a large Hall device with 40 μm implantation width, the model's simulation is in very good agreement with the measured results. However, when the N-well implantation width is reduced to 0.8 μm, the error becomes a bit larger[12]. This is because the N-well lateral diffusion effect is over estimated. The N-well doping level is higher than the actual value so that the simulated S_I is obviously higher than the tested result. Over all, a good match between the simulation and experiments is obtained for the small Hall devices when the N-well implantation width is higher than 2.4 μm.

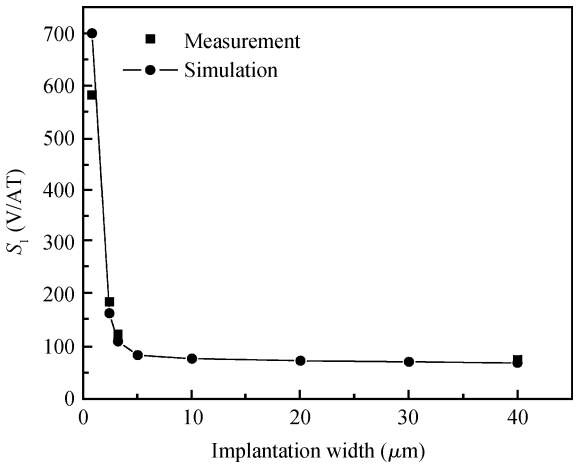

Fig. 7. Comparisons between the simulations and measurements of the current related sensitivity for different N-well implantation widths.

4. Conclusions

A simplified compact simulation model for miniaturized CMOS-integrated Hall devices has been developed. The model only consists of a passive network, including eight non-linear resistors and four current-controlled voltage sources. Except for two physical stress-related effects (piezo-resistance and piezo-Hall effects) induced packaging, the model not only takes into account the non-linear conductivity, geometrical effect, and temperature drift, but also considers the lateral diffusion and junction field effect for the miniaturized Hall devices. The model has been written in Verilog-A hardware description language and only needs ten key technological and physical parameters. The used parameters can be easily obtained from device measurements or foundry technology files. The model does not need to use JFET model and can be directly performed in standard SPICE-like EDA tools such as Cadence Spectre. To prove the correctness and accuracy of the simplified model, the model simulation was performed using AMS CXQ 0.8 μm CMOS technology parameters. The simulation results are in good agreement with the classic experimental results[11, 12]. Therefore, the simplified model is very suitable for the circuit design of Hall magnetic micro-system chips.

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