A 14-bit 80 MS/s CMOS ADC with 84.8 dB SFDR and 72 dB SNDR

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Abstract: This paper presents a design of 14-bit 80 Msample/s pipelined ADC implemented in 0.35 μm CMOS. A charge-sharing correction is proposed to remove the signal-dependent charge-injection, together with a low-jitter clock circuit, guaranteeing the high dynamic performance for the ADC. A scheme of capacitor-switching and a symmetrical layout technique minimizes capacitor mismatch, ensuring the overall linearity. The measured results show that the calibration-free ADC achieves an effective number of bits of 11.6-bit, spurious free dynamic range (SFDR) of 84.8 dB, signal-to-noise-and-distortion ratio (SNDR) of 72 dB, differential nonlinearity of $+0.63/-0.6$ LSB and integrated nonlinearity of $+1.3/-0.9$ LSB at 36.7 MHz input and maintains over 75 dB SFDR and 59 dB SNDR up to 200 MHz.

Key words: CMOS; charge-sharing correction; symmetrical layout and calibration-free
DOI: 10.1088/1674-4926/33/2/025012 **EEACC:** 1265H; 1280

1. Introduction

For modern communication systems such as wireless receivers, ultrasound applications are the main driving force behind the improvement of high-resolution and high-speed ADC. In particular, the improvement of an IF sampling system requires that the ADC not only has a higher sampling rate and over 12-bit resolution, but also other high dynamic performance, in terms of signal-to-noise-and-distortion ratio (SNDR), spurious free dynamic range (SFDR) and input bandwidth, with low power dissipation. As the resolution reaches 14-bit, it is very difficult to design high-speed ADCs that maintain the required linearity over a large bandwidth maintaining over 80 dB SFDR and 70 dB SNDR. A great deal of work has been done for such research. The on-chip buffered ADCs can get over 14-bit accuracy and 100 dB SFDR at over 100 Msample/s for 100 MHz input[1−4]. However, the input bipolar buffers will dissipate a great deal of power and cannot be implemented in a CMOS process. CMOS technology offers many advantages for ADC design, including low cost, low power consumption, etc. The CMOS switch-capacitor pipeline is the most widely used structure to realize high-speed high-resolution and low power ADCs. However, it suffers from limited amplifier gain and bandwidth, MOS device charge injection and capacitor mismatch. So design of such an ADC presents many tradeoffs and challenges.

This paper presents a calibration-free 14-bit 80 Msample/s pipelined ADC fabricated in 0.35 μm CMOS process, by using a charge-sharing correction (CSC) technique, the nonlinearity due to signal-dependent charge-injection and the load to the previous stage is greatly minimized. The capacitor-switching technique and symmetrical layout for capacitor arrays is adopted which reduces the capacitor mismatch a great deal. A low-jitter clock circuit is added to maintain the ADC performance at high frequencies with high SNDR. A dynamic biasing scheme and scaling technique helps to reduce the total power consumption. The measured results show that the ADC achieves 72 dB SNDR, 84.8 dB SFDR at 36.7 MHz input and maintains 59 dB SNDR, 75 dB SFDR up to 200 MHz input. At 80 Msps, the ADC consumes 303 mW power under 3.3 V supply.

2. Architecture

The ADC structure used in this work is shown in Fig. 1. It consists of a front-end sample-and-hold amplifier (SHA) followed by pipelined switched-capacitor ADC, which includes a 4-bit first stage following by eight 1.5-bit stages, and a final 3-bit flash. Each pipeline consists of a flash ADC and a multiplying DAC (MDAC). The use of multi-bits for the first stage provides an optimal power and speed budget in high resolution ADC[5, 6], and relaxes the linearity and matching requirement down the subsequent stages. So the bias currents and capacitors of these stages are scaled down by certain ratio[7]. The first two stages utilize a capacitor switching technique[8] to average out the mismatch error of capacitors. On-chip trimming can adjust bias point for op-amp and reference currents to control the gain and offset errors. The differential reference is externally decoupled and is on-chip buffered to provide a stable reference for the ADC. A low-jitter short path clock circuit is presented later which contributes a little on-chip clock jitter.

3. Circuit design and implementation

3.1. Sample-and-hold amplifier (SHA)

Flip-around architecture is utilized for the SHA for its unique advantages[5] over charge-redistribution one. A bootstrapped circuit is used to linearize the input switch. Usually the input switch is made large to minimize its on-resistance, which

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Received 21 July 2011, revised manuscript received 30 August 2011

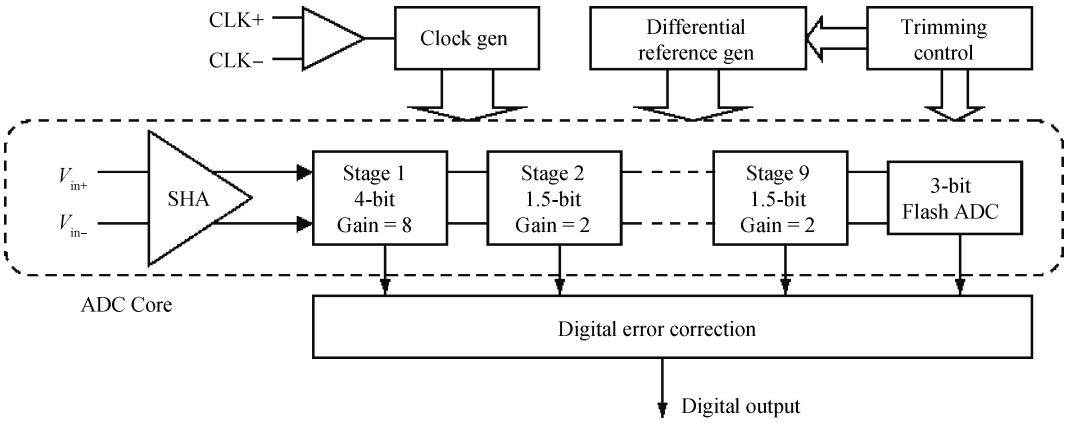

Fig. 1. ADC Architecture.

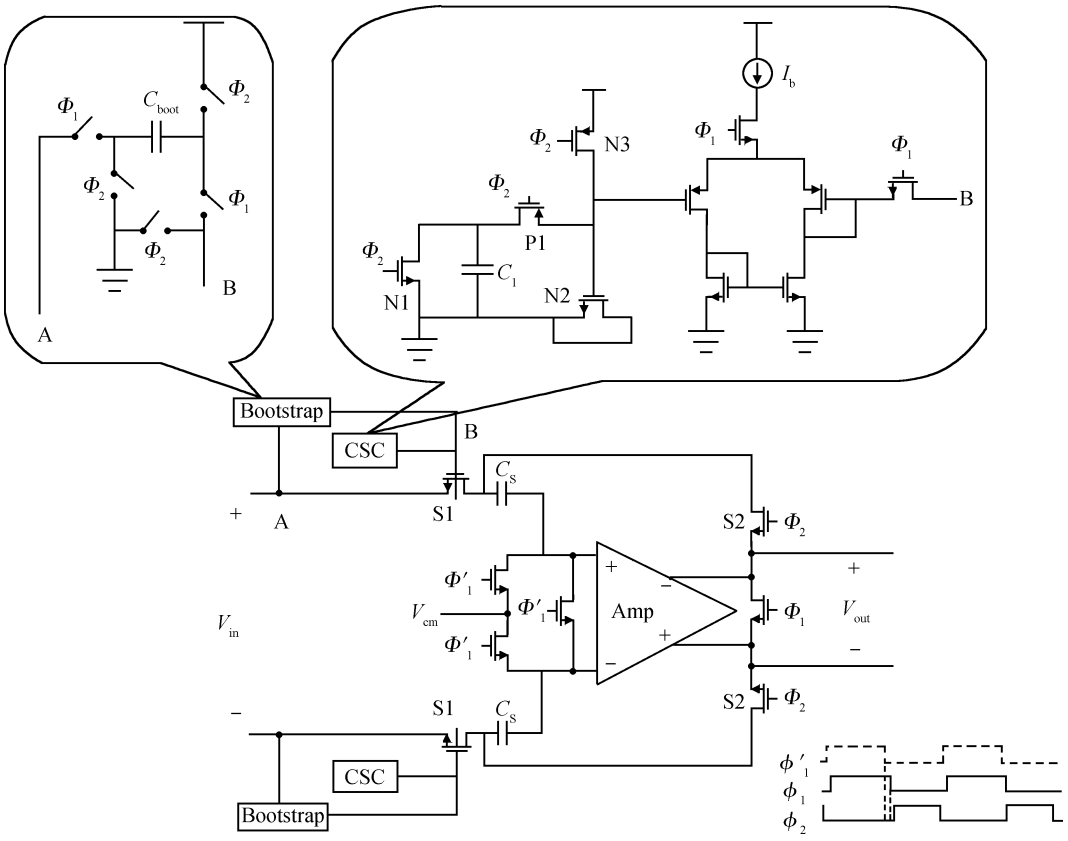

Fig. 2. Flip-around sample/hold (S/H) with CSC.

also shares the charge on the bootstrapping capacitor. In order to reduce the charge loss, sometimes a very large bootstrapping capacitor is used. However, as the capacitor is increased, the allowable operating frequency is lower and the external driving requirement becomes higher. In this work, a CSC circuit is added to effectively solve above problem. As shown in Fig. 2, during the hold phase (Φ_1 low, Φ_2 high), the bootstrapped capacitor C_{boot} is charged to V_{DD}, the input switch S1 is open, the C_1 (same size as C_{boot}) of CSC is discharged to ground and N2 (dummy switch of input sampling switch S1), which has the same size as S1, is charged to V_{DD} and the high-speed unity buffer is disabled. During the sample phase (Φ_1 high, Φ_2 low), the dummy transistor N2 is shorted to C_1 so that the voltage at the gate of N2 is just the equivalent charge loss, which mimics the charge-sharing between C_{boot} and gate capacitance of S1. This equivalent voltage is buffered and connects to gate of input switch S1 (node B), effectively compensating the charge loss due to the charge-sharing.

To further prove this theory, it can be seen that if CSC is not added, at hold phase, the charge on C_{boot} is V_{DD} C_{boot}; at sample phase, the charge on C_{gs1} (the gate–source capacitance of S1) and C_{boot} is $V_x(C_{gs1}+C_{boot})$, as the charge keeps constant, V_{DD} C_{boot} = $V_x(C_{gs1}+C_{boot})$, so the bootstrapping voltage loss (ΔV) due to the charge-sharing is

$$\Delta V = V_{DD} - V_x = V_{DD}\frac{C_{gs1}}{C_{gs1}+C_{boot}}. \quad (1)$$

In CSC, at hold phase, the charge on C_{N2} (the gate–source

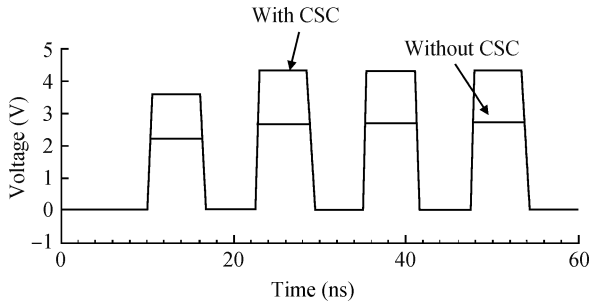

Fig. 3. Simulated bootstrapped gate voltage.

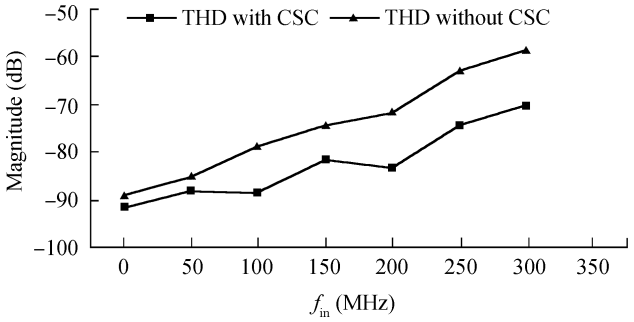

Fig. 4. THD of S/H circuit with and without CSC.

capacitance of N2) is $V_{DD}C_{N2}$; at sample phase, the charge on C_1 and C_{N2} is $V_y(C_1 + C_{N2})$, for $V_{DD}C_{N2} = V_y(C_1 + C_{N2})$, so

$$V_y = V_{DD}\frac{C_{N2}}{C_{N2} + C_1}. \quad (2)$$

As $C_{N2} = C_{gs1}$, $C_1 = C_{boot}$, obviously $V_y = \Delta V$ that the voltage at the gate of N2 equals the voltage loss due to the charge-sharing.

Figure 3 shows that by using the proposed CSC, the charge loss is almost completely compensated and the input dependent charge-injection is completely removed. In addition, the total harmonic distortion (THD) of the S/H circuit with CSC is much lower than without CSC, as shown in Fig. 4, especially at frequency higher than 100 MHz.

For a 14-bit 80 Msps ADC design, the S/H amplifier should have over 110 dB DC gain and 1 GHz unity-gain bandwidth in practical case[9]. Usually a gain-enhanced folded-cascode amplifier is used to meet these stringent requirements[10]. The bandwidth of the overall amplifier is determined by G_m/C_L, and G_m is proportional to the aspect ratio of the input pair. Usually the size of the input pair is very large in order to get a large bandwidth, but it will introduce a large parasitic capacitance to the folding node and consume a lot of power. In order to solve this problem, a symmetrical amplifier is adopted in this work so that a current mirror is utilized instead of folding, as shown in Fig. 5. The mirror ratio determines the amplifier bandwidth[11].

A single-ended current input of a gain-enhanced amplifier is used so as to keep the layout on the signal side clean[12]. As the current of input branch is not fixed, this amplifier can help the main amplifier slew more quickly acting as a push-pull function. In addition, a capacitor C_k is placed with appropriate value at the output of gain-enhanced amplifier to push its unity-gain frequency to the right place to minimize the doublet

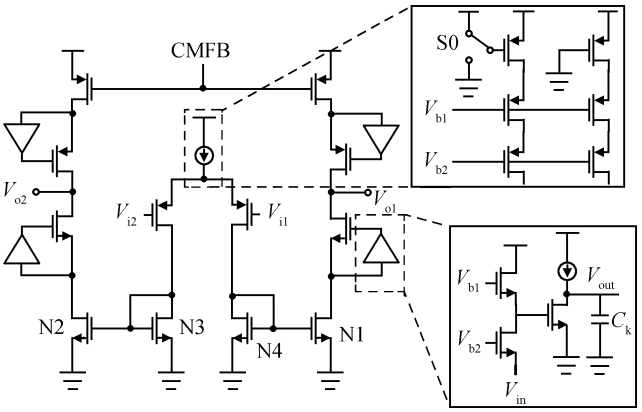

Fig. 5. Proposed amplifier for SHA.

effect[13].

The amplifier is the most power-hungry unit in an ADC. In this work, the dynamic switching bias[14] is adopted to reduce the amplifier power dissipation. At the sampling phase, switch S0 connects to power supply and at hold phase, connects to ground. The control clock for S0 is a little ahead with respect to normal sample/hold clock, preventing transient current affecting the normal operation. The simulation result shows that there is 20% power saving for the entire ADC when dynamic switching is enabled.

3.2. 4-bit first stage

The main source of non-linearity in this ADC structure comes from the capacitor mismatch of the first pipeline stage, which consists of a 4-bit sub-ADC and an MDAC with gain of 8. As shown in Fig. 6, the first stage contains an 18-capacitor array, a switching network, a sub-DAC and a two-stage gain-boosted amplifier for the MDAC and a sub-ADC.

In this work, the poly-insulator-poly capacitor is used and the MDAC capacitors are placed as a common-centroid formation. The typical value of unit capacitance is 0.85 fF/μm^2, which forms a 4.96 pF capacitor of the first stage to minimize KT/C thermal noise. The mismatch of the capacitor pair is proportional to the reciprocal of its area; the matching parameter of capacitor is defined as: $ac = \sqrt{WL}\sigma(\frac{\Delta C}{C})$ (ac is the matching parameter). The random deviation provided by the process is 0.09 which is theoretically enough for 14-bit linearity. However, in practice, the mismatch parameter may vary out of specification due to process variation. To ensure matching accuracy, a switching network similar to Ref. [8] is added. At each sampling phase there are two of 18 capacitors connected as feedback capacitors and the other 16 capacitors connect to V_{in}, V_{ref} and V_{DAC}, as determined by the 4-bit sub-ADC output, so that the capacitor mismatch error is averaged out. According to Ref. [8], when the capacitor switching is used, the transfer curve error due to capacitor is $\frac{1}{2}(\frac{1}{2}\varepsilon_i - \frac{1}{2}\varepsilon_j)$, ε_i and ε_j ($i = 0$ to 7 or 9 to 16; $j = 8$ or 17) is the variation of the unit capacitance. There is about 1-bit improvement of differential nonlinearity compared to normal MDAC operation without using the capacitor switching technique. The large number of switches contributes a large amount of capacitance to the SHA, so the bootstrapping with CSC technique is also adopted here to minimize this loading effect and remove the signal-dependent

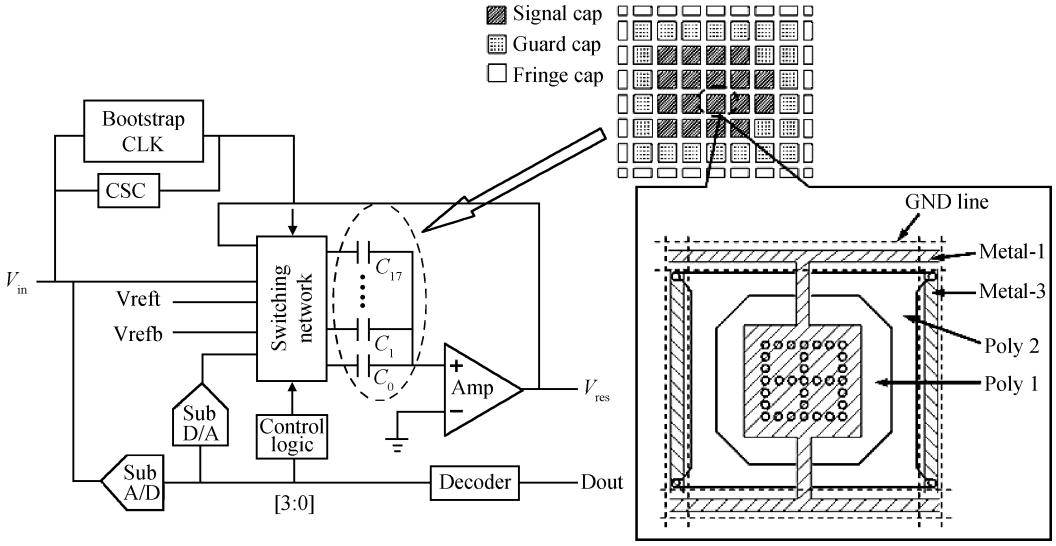

Fig. 6. Pipeline stage 1 in this work.

charge-injection.

The capacitor switching is utilized in second and third 1.5-bit pipeline stage, in which the 2-bit flash output code controls the switching logic for a 4-capacitor array.

A layout technique for reducing the capacitor mismatch is utilized. All the signal capacitors are surrounded by guard capacitors so that each capacitor will see the same parasitic condition. The fringe capacitors are placed along the peripheral line for the etching errors. Each signal line is shielded and covered by ground line, being isolated from the environment influence. The contact arrays uniformly locate at the top of poly1 to reduce the connecting resistance. As a result, the parasitic for each signal capacitor is almost the same and capacitor mismatch is greatly reduced.

The first pipeline stage should settle to 14-bit accuracy within half of operating period, as the sampling frequency increases, the allowable op-amp settling time is reduced, which requires an MDAC amplifier with a large DC gain and unity bandwidth. To meet this stringent requirement, a two-stage Miller compensated gain-boosting amplifier is used. The large DC gain (124 dB) of the op-amp in this work helps relax the MDAC capacitor matching requirement[15].

3.3. Clock jitter

The signal-to-noise ratio (SNR) will be significantly degraded by the jitter, which mainly comes from the external clock source and the internal clock path. The clocks will add periodical and random jitter to the ADC, and usually this jitter is much larger than the signal noise. So at a given input frequency, the SNR can be defined by

$$\mathrm{SNR} = -20\log_{10}(2\pi f_{\mathrm{input}} t_j). \tag{3}$$

It is obvious that a high-speed ADC is very sensitive to the quality of the clock input. According to Eq. (3), if the total jitter of ADC is 200 fs, at 100 MHz input frequency, the SNR is about 72 dB. The low-jitter source with a proper band-pass filtering can contribute jitter of 30 fs[16]. Referring to Ref. [3], the maximum jitter of ADC is restrained by

$$t_j(\mathrm{ADC}) = \sqrt{t_j^2 - t_j^2(\mathrm{clocksource})}. \tag{4}$$

From above equation, the maximum jitter provides by ADC shall be less than 197 fs.

Except by using a clean clock source, the reasonable way to minimize jitter is to utilize layout isolation, shielding and a decoupling technique. In addition, the jitter from on-chip clock path is

$$t_j = \frac{V_{\mathrm{CLK\_jitter}}}{\mathrm{d}V_{\mathrm{CLK}}/\mathrm{d}t}. \tag{5}$$

So the clock jitter is inversely proportional to the clock signal slope and the slope can be increased by the clock buffer. The total delay of clock path is proportional to the clock jitter[17]. In this work, the differential clock input is used to cancel the common-mode noise and a duty cycle stabilizer with short delay controls the clock edge, which is followed by a balanced clock distribution circuit.

As shown in Fig. 7, the buffer followed by a differential-to-single ended amplifier (D-to-S) includes a PMOS input pair which can accommodate a wide input range. The NMOS cross-coupled and diode-connected pair increases the gain so as to increase the clock slope. The DCS consisting of a Schmitt trigger, a low-pass filter and flip-flops, provides the stable 50% duty cycle clock to minimize unwanted spurs and harmonics, allowing the duty cycle of input clock varying between 30% and 70%. Certain dummy inverters are added to the clock distribution circuit to balance the capacitance load so that to reduce the clock skew in each pipeline stage. Simulation results show that the clock jitter is estimated to be less than 120 fs.

4. Measured results

The ADC is fabricated in a 0.35 μm 2-poly 4-metal CMOS process and packaged in 32-lead ceramic LCC. The die area is 5.9 mm^2, containing the pipeline ADC core, clock and reference generation, etc, as shown in Fig. 8. In the test setup, the clock signal comes from a low-jitter crystal-controlled oscillator and is narrowly band-passed to provide an 80 MHz clock

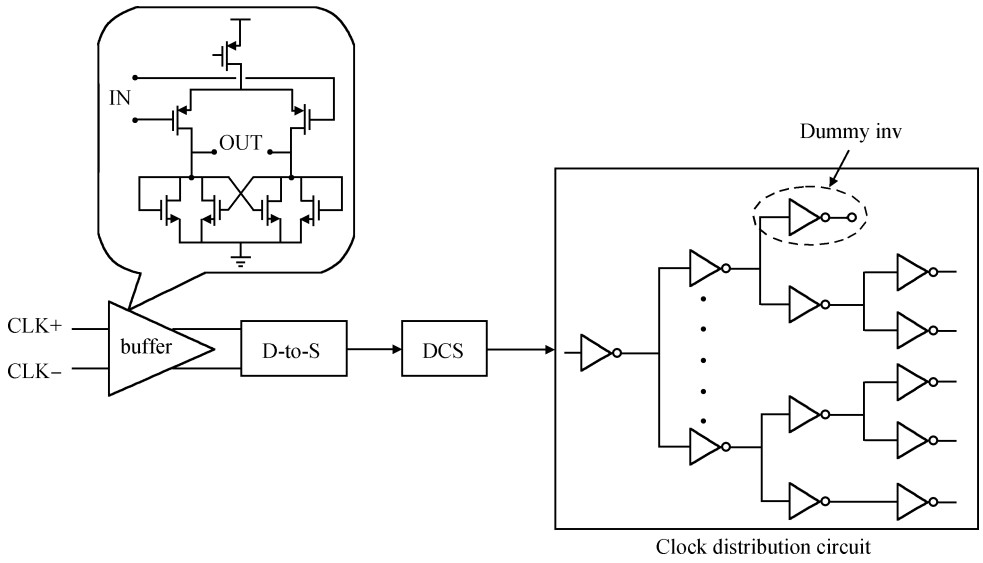

Fig. 7. Clock generation circuit.

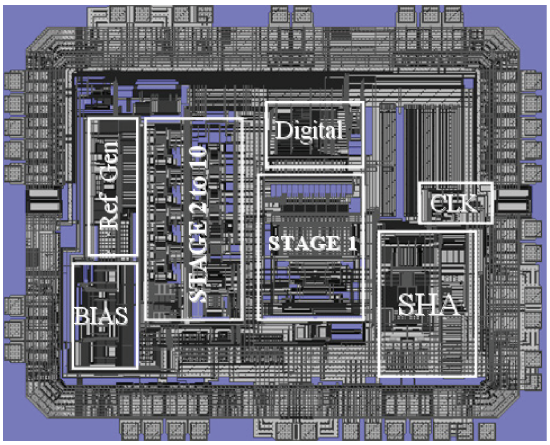

Fig. 8. Die photograph.

Table 1. ADC performance summary.

Parameter	Value
Resolution/Sampling rate	14 bit/80 Msps
DNL (LSB)	$+0.63/-0.6$
INL (LSB)	$+1.3/-0.9$
SFDR (dB)	84.8 @ $F_{\text{in}} = 36.7$ MHz 75.1 @ $F_{\text{in}} = 200$ MHz
SNDR	72 @ $F_{\text{in}} = 36.7$ MHz 59.2 @ $F_{\text{in}} = 200$ MHz
Power supply (V)/Input range (Vp-p)	3.3/2.2
Power dissipation (mW)	303
Technology	0.35 μm 2P4M CMOS

with less than 40 fs jitter. The clock source supply is isolated from other parts on the board and all the supplies are heavily decoupled. The ADC is driven differentially through a high-frequency transformer, which helps maintain the ADC performance in under-sampling case.

Figure 9 shows that the DNL is $+0.83/-0.78$ LSB, INL is $+7.1/-6.3$ LSB without capacitor switching and reduces to $+0.48/-0.7$ LSB and $+2.8/-1.6$ LSB, respectively, with capacitor switching enabled. For a 36.7 MHz input, the ADC achieves 72 dB SNDR, 84.8 dB SFDR and 11.6-bit ENOB at sampling rate of 80 Msps (Fig. 10). Figure 11 indicates the measured results of SFDR and SNDR characteristics with CSC enabled and disabled, which proves the availability of CSC technique. The SNDR and SFDR maintain over 75 dB and 59 dB respectively up to input frequency of 200 MHz. Under 3.3 V power supply, the ADC dissipates 303 mW. The performance is summarized in Table 1.

5. Conclusion

This paper presents the design of a 14-bit 80 Msps switch-capacitor pipelined ADC fabricated in 0.35 μm 2P4M CMOS technology under 3.3 V power supply. By using the CSC technique, the signal-dependent charge-injection is removed. A technique of capacitor-switching and a symmetrical layout of signal capacitor arrays is adopted to minimize capacitor mismatch, and a low-jitter clock circuit is utilized to increase the SNDR significantly. The ADC consumes 303 mW power at 80 Msps under 3.3 V supply, which achieves $+0.63/-0.6$ DNL and $+1.3/-0.9$ INL with 84.8 dB SFDR and 72 dB SNDR at 36.7 MHz input and maintains high dynamic performance up to 200 MHz.

References

[1] Moreland C, Murden F, Elliott M. A 14-bit 100-Msample/s subranging ADC. IEEE J Solid-State Circuits, 2000, 35: 1791
[2] Payne R, Corsi M, Kaylor S. A 16-bit 100 to 160 MS/s SiGe BiCMOS pipelined ADC with 100 dBFS SFDR. IEEE J Solid-State Circuits, 2010, 45: 294
[3] Ali A, Dillon C, Sneed R. A 14-bit 125 MS/s IF/RF sampling pipelined ADC with 100 dB SFDR and 50 fs jitter. IEEE J Solid-State Circuits, 2006, 41: 1846
[4] Ali A, Morgan A, Dillon C. A 16 b 250 MS/s IF-sampling pipelined A/D converter with background calibration. IEEE J Solid-State Circuits, 2010, 45: 292
[5] Yang W, Kelly D, Mehr I, et al. A 3-V 340 mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input.

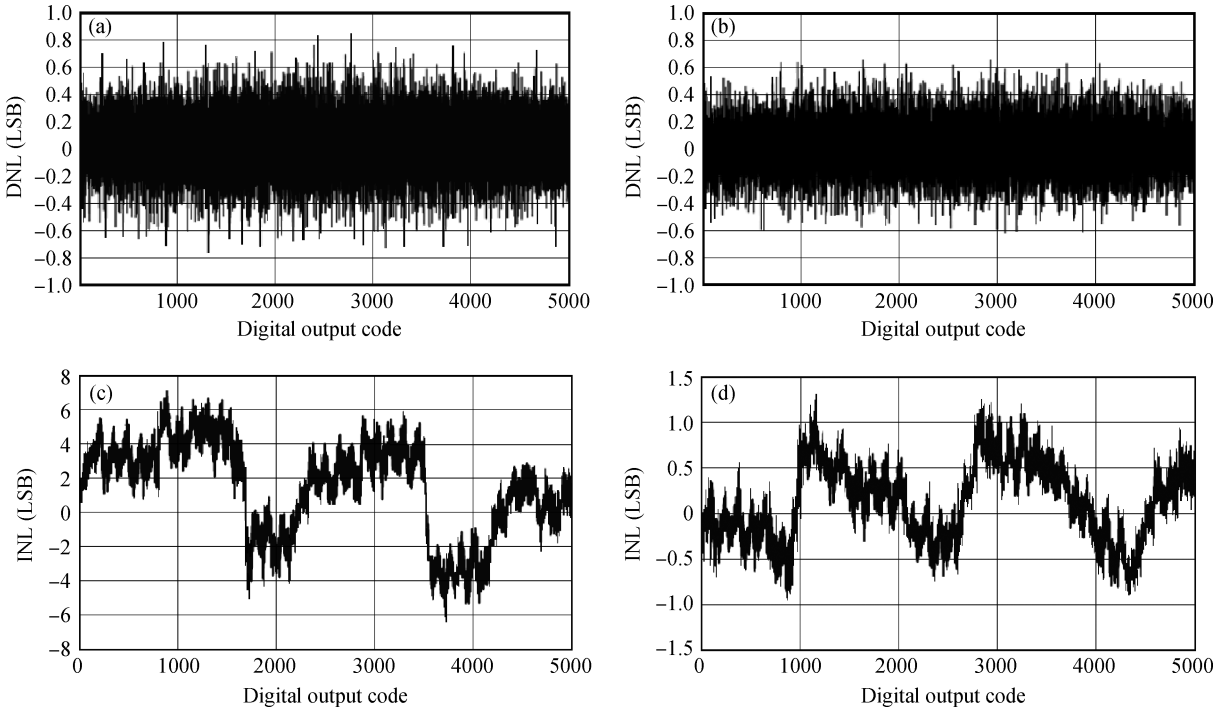

Fig. 9. Measured DNL & INL. (a), (c) Without CSC. (b), (d) With CSC.

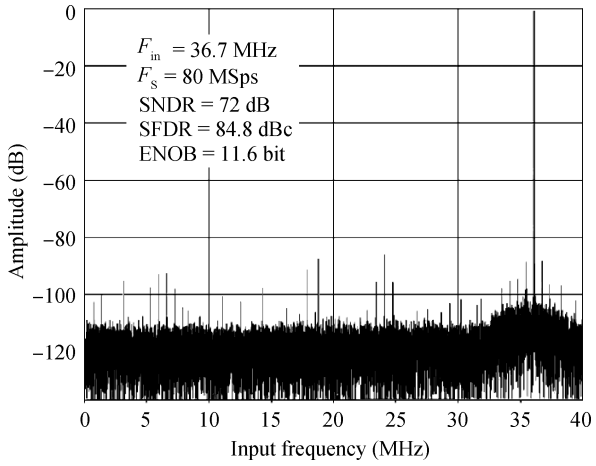

Fig. 10. Measured FFT spectrum.

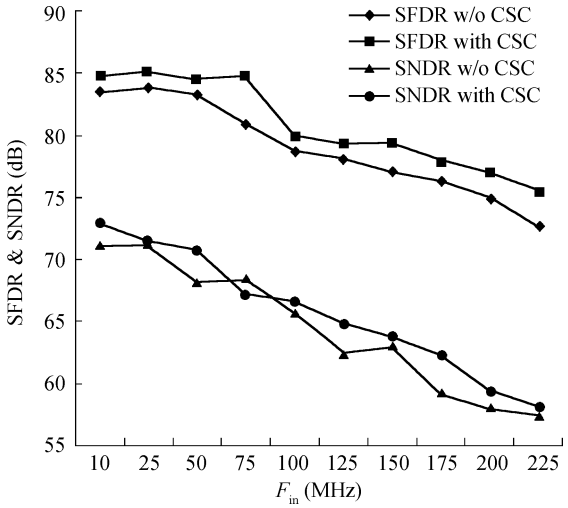

Fig. 11. SNDR & SFDR versus input frequency at 80 Msps.

IEEE J Solid-State Circuits, 2001, 36: 1931
[6] Singer L, Ho S, Timko M, et al. A 12-b 65-Msample/s CMOS ADC with 82-dB SFDR at 120 MHz. ISSCC Dig Tech Papers, 2000, 1: 38
[7] Chiu Y, Gray P, Nikolic B. A 14-b 12-MS/s CMOS pipelined ADC with over 100-dB SFDR. IEEE J Solid-State Circuits, 2004, 39(12): 2139
[8] You S, Lee K, Choi H, et al. A 3.3 V 14-bit 10 MSPS calibration-free CMOS pipelined A/D converter. ISCAS, 2000, 1: 435
[9] Baker R J. CMOS: mixed-signal circuit design. New York: John Wiley & Sons, 2004
[10] Bult K, Geelen G. A fast-settling CMOS op amp for SC circuits with 90-dB DC gain. IEEE J Solid-State Circuits, 1990, 25: 1379
[11] Sansen W. Analog design essential. Dordrecht: Springer, 2006
[12] Sasidhar N, Kook Y, Takeuchi S, et al. A low power pipelined ADC using capacitor and opamp sharing technique with a scheme to cancel the effect of signal dependent kickback. IEEE J Solid-State Circuits, 2009, 44: 2392
[13] Bult K, Geelen G. The CMOS gain-boosting technique. Analog Integrated Circuits and Signal Processing, 1991, 1: 119
[14] Ahuja B, Hoffman E. Dynamic biasing technique for low power pipelined analog to digital converters. USA Patent, No. 6462695, 2002
[15] Liu M, Ou W, Su T, et al. A 1.5 V 12-bit 16 MSPS CMOS pipelined ADC with 68 dB dynamic range. Analog Integrated Circuits and Signal Processing, 2004, 41: 269
[16] Zanchi A, Tsay F. A 16-bit 65-MS/s 3.3-V pipeline ADC core in SiGe BiCMOS with 78-dB SNR and 180-fs jitter. IEEE J Solid-State Circuits, 2005, 40: 1225
[17] Waltari M, Sumanen L, Korhonen T, et al. A self-calibrated pipeline ADC with 200 MHz IF-sampling frontend. Analog Integrated Circuits and Signal Processing, 2003, 37: 201