Design for manufacturability of a VDSM standard cell library*

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Abstract: This paper presents a method of designing a 65 nm DFM standard cell library. By reducing the amount of the library largely, the process of optical proximity correction (OPC) becomes more efficient and the need for large storage is reduced. This library is more manufacture-friendly as each cell has been optimized according to the DFM rule and optical simulation. The area penalty is minor compared with traditional library, and the timing, as well as power has a good performance. Furthermore, this library has passed the test from the Technology Design Department of Foundry. The result shows this DFM standard cell library has advantages that improve the yield.

Key words: design for manufacturability; reduced standard cell library; layout optimization; optical simulation; yield

DOI: 10.1088/1674-4926/33/2/025015 **EEACC:** 2570

1. Introduction

In the nano-era, the technology of design for manufacturability (DFM) is especially important. The consideration of process variation becomes an indispensable factor for designers. DFM is concerned with the process influences on the yield of chips, relating to two key processes of lithography and chemical mechanical planarization (CMP) in manufacturing. At a 65 nm process, various RETs have been applied to mask manufacturing.

Substantial previous work has been done in the area of DFM-friendly standard cell libraries. Heineken *et al.*[1] proposed generating yield optimized cells and using them in synthesis. This approach has since been refined by several others. DFM considerations from a key part of the standard cell methodology was described by Aitken[2]. However, all of the previous work has two issues: a design flow including DFM optimization and the balance between DFM and performance has not been proposed. Furthermore, the traditional standard cell library has many cell categories, which will take too much time to optimize layout and the data size is huge when manufactured. The efficiency of production is directly influenced. It has become the bottleneck of mask manufacture.

This paper proposes a new method which can make the process of OPC more convenient. To achieve this goal, a 65 nm DFM standard cell library has been constructed according to the design rule supplied by the foundry and the requirements of the performance. The 65 nm DFM standard cell library can realize all logics of traditional standard cell library. The size of the library has been largely reduced through logic combination of the basic cells, which will make the process of OPC become more efficient and the need for large storage is reduced. The OPC-based physical design takes the manufacture factors into account in the design phase and DFM design rule optimization can avoid the structure of hotspot efficaciously. Moreover, this library is more manufacture-friendly as every cell has been optimized by optical simulation. Consequently, the process of OPC can be implemented efficaciously and the chip performance will be improved. Not is only the storage of the data reduced significantly, but the yield is enhanced greatly.

2. Reduced standard cell library

It is not necessary to use every cell in a library to realize the logic function and the performance of the circuit will not visibly decrease[3]. For decreasing the difficulty of manufacturing, it is better to use a small type of logic cell to realize the circuit function in a 65 nm process node. A certain way is proposed to choose the standard cells to achieve this target.

First, when choosing the most basic cells, such as inverter, buffer, primitive gates, compound gates, operate cells and sequence cells, try to traverse all complicated logic by appropriately combining these cells. Second, as a standard cell library for use, it has to completely take into account front and back design requests. So some special cells must exist, such as delay cells, pull cells, fillers, cap fillers, nwell/substrate ties and antenna cells, in order to realize the basic function of the cell library. Third, the multi-input cells are realized by logic decomposition. For an example, a 4-input logic can be realized by two 2-input logics or one 3-input logic and one 1-input logic. These multi-input cells contribute to the area used in cell library, but the gate delay is in proportion to the square of input number. So a multi-input logic is harmful for timing, and logic decomposition such as that above is effective, which will not cause much area dissipation. Fourth, a high drive cell is realized by drive decomposition. In order to resolve the problem of drive ability and to not increase the number of cell categories, the following method has been used: $\times 4$, $\times 8$ and $\times 16$ are designed alone for the inverter and the buffer, which is made for releasing the nervous timing. For other high drive logics, the

* Project supported by the National Major Specialized Program of China (Nos. 2008ZX01035-001-07, 2009ZX02023-4-2).
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Received 22 July 2011, revised manuscript received 5 September 2011

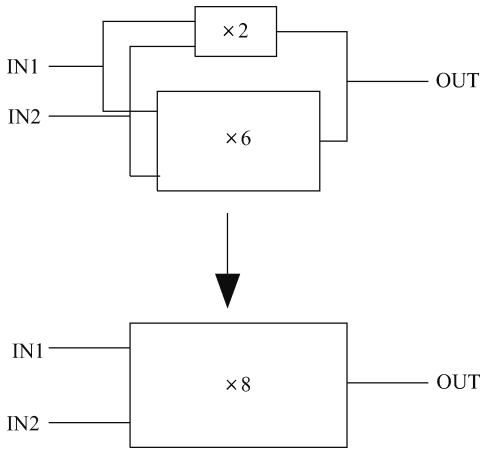
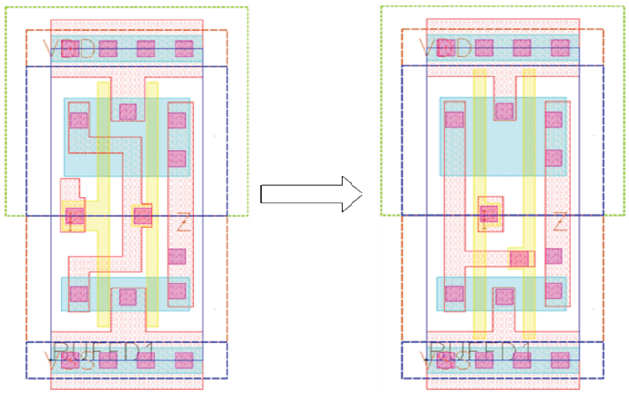
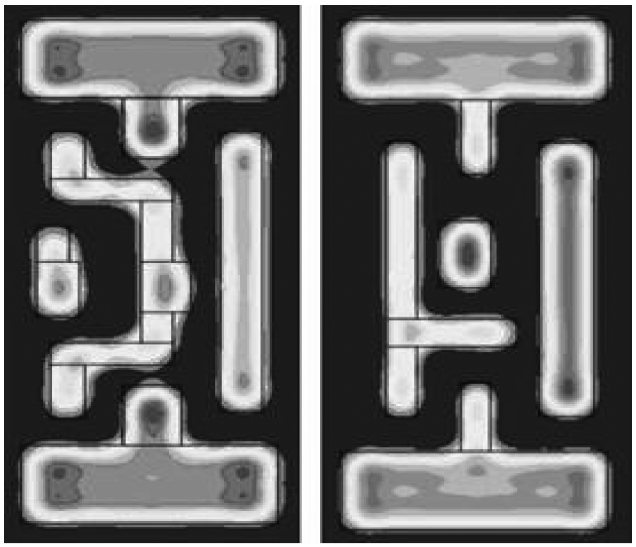


Fig. 1. A parallel cell realization example.



(a) Pre-opt layout (b) Post-opt layout

Fig. 2. Layout of buffer cell.



(a) Pre-opt (EPE: 2809) (b) Post-opt (EPE: 2521)

Fig. 3. Metal of buffer after optical simulation.

principle is followed: do not increase cell categories. We realize them by multiple existing logics, as Figure 1 shows.

Some additional delay will be brought in by using this method, but the output transition time will be greatly improved. The gate delay is connected with the input transition time and the total output net capacitance. The look up table in the library model file (.lib), which includes gate delay information is made just through the input transition time and output load. So it should be decided by using a synthesis tool whether to use multiple existing logics.

After a great deal of practice, it is proven that the circuit performance after synthesis will not lose beyond 2% if the category of the standard cell is reasonably chosen and the cell size is reasonably designed[4]. Furthermore the cell is elaborately designed and has advantages in the accuracy and stability of its timing. The designer also can add cells according to the special use of the library.

As for cellwise OPC, the data we need to keep is a primitive database containing different OPC versions of the standard cells[5]. This reduced standard cell library decreases the number of layouts greatly, which will make manufacturing brief and favorable to OPC by decreasing the data size. Therefore, production efficiency will be greatly improved.

3. Layout optimization through DFM rules

The layout is the basis of mask manufacture and the target of wafer graphics, and it is the core of resolving the DFM problem. A better design for the layout of a standard cell can reduce some problems that are encountered during lithography or CMP but are hard to fix. At the same time it can reduce the data size, which will increase at OPC stage. DFM-friendly design rules are created based on learning from prior silicon data and/or technology CAD simulations. Typically these are not captured by the SPICE transistor and extraction models[6]. The layout has been designed according to the DFM and DRC rule in order to satisfy the requirements of manufacturing. The DFM-friendly rules fall into several major categories:

(1) Improved printability. These include line end rules, regularity requirements, diffusion shape near gate rules, contact overlap rules, etc[7].

(2) Reduced mask complexity. These include rules about "jogs", or small changes in dimensions, structures that could confuse line end algorithms, and space needed for phase shift mask features[8].

(3) Reduced critical area. These include relaxed spacing, increased line thickness, etc.

(4) CMP rules. These include density fill, as well as layer relationship rules.

The layout of buffer before optimization (pre-opt) is shown in Fig. 2(a), and Figure 2(b) shows the one after optimization (post-opt) according to DFM-friendly rule. The DFM-friendly design rules summarized above are for using the RET conveniently. Some rules have been written into the recommended DFM rules in the foundry.

Based on these DFM-friendly design rules and SMIC 65 nm design rules, the DFM standard cell library has been developed through the Virtuoso platform of Cadence. With the foundation of its achievement of the traditional standard cell library, the RET, which makes the DFM standard cell library, has high reliability and accuracy.

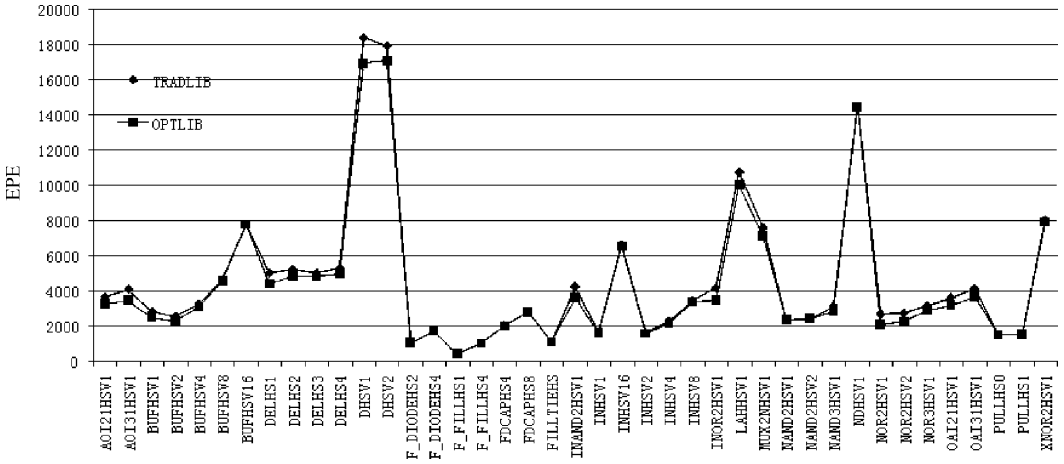


Fig. 4. Contrast of all standard cells' EPE.

4. Optical simulation for cells

All traditional and DFM optimization cells have been simulated by using the DFMT-IME, which is an optical simulation tool developed by EDACAS. The manufacturing has been checked through edge placement error (EPE), which represents the quality of lithography from the result of optical simulation.

The buffer metal after optical simulation is shown in Fig. 3. It can be observed that the EPE has been reduced to about 10% and many virtual attach nodes have disappeared after DFM optimization. Clearly the manufacturing process has been significantly improved.

The contrast of all cells is plotted in Fig. 4, showing the EPE between the traditional standard cell library (TRADLIB) and the DFM standard cell library (OPTLIB).The EPE of some special cell*s* is equal because the structure of these cells is simple and has no room for layout optimization, such as in fillers and diodes. For the EPE of other cells, OPTLIB is smaller than TRADLIB, which proves that our DFM standard cell library has higher quality after lithography.

The design flow of standard cell library including the optical simulation stage is shown in Fig. 5. The cell can be optimized in time and deal with the problems which will be encountered during manufacturing.

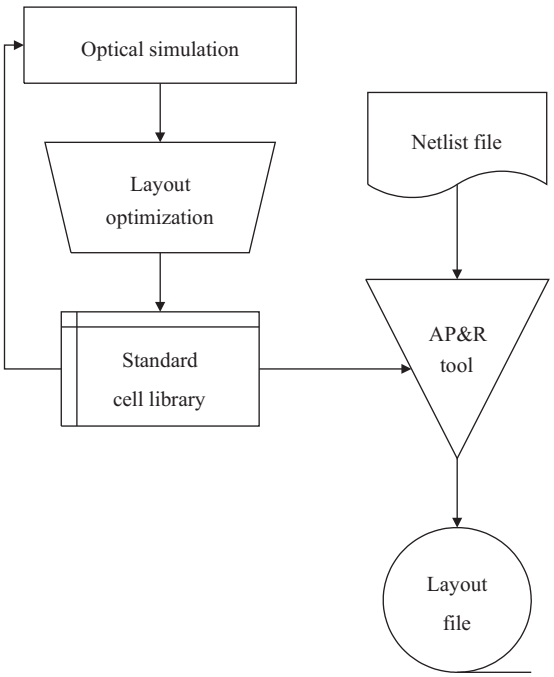


Fig. 5. Design flow of standard cell library which includes the optical simulation stage.

5. Performance and manufacturing verification

5.1. Performance verification

The synthesis library model file of the cell library (lib) contains information about cell delay, area and power, so the performance verification is equal to verify the synthesis library model file.

Three cell libraries are used as the target library for the design compiler (DC). OPTLIB is the 65 nm DFM standard cell synthesis library, TRADLIB is the 65 nm traditional standard cell synthesis library and TRADLIB_SELECT is the traditional synthesis library which only contains the same cells as OPTLIB. Then the 16 benchmark circuits selected from ISCAS85 and ISCAS89 have been synthesized according to different constraints. The performance of the DFM standard cell library developed in this project is verified from three aspects: timing, area and power.

The power is compared when the timing constraint is nervous. After synthesis for all benchmarks, the power reported by DC is plotted in Fig. 6. It can be observed that the circuits synthesized by the OPTLIB have lowest power.

The curves in Fig. 7 are the timing after synthesis for all benchmarks when the area is nervous. It obviously shows that the timing of OPTLIB is best among the three libraries.

Finally the area is compared when the timing is nervous. The result is plotted in Fig. 8. It obviously shows that the OPTLIB is better than TRADLIB_SELECT, but has less than 5% increase in area compared to TRADLIB. This loss in area can be accepted completely. As synthesized blocks in standard cells are only a part of the VLSI and memory, I/O, clock system and handcrafted data paths occupy the major portion of the

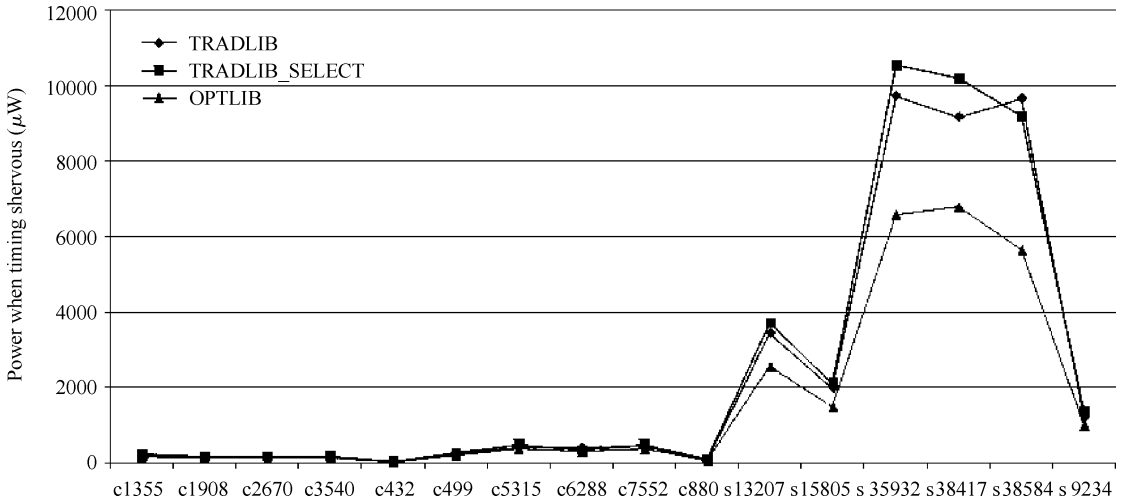


Fig. 6. Power when timing is nervous.

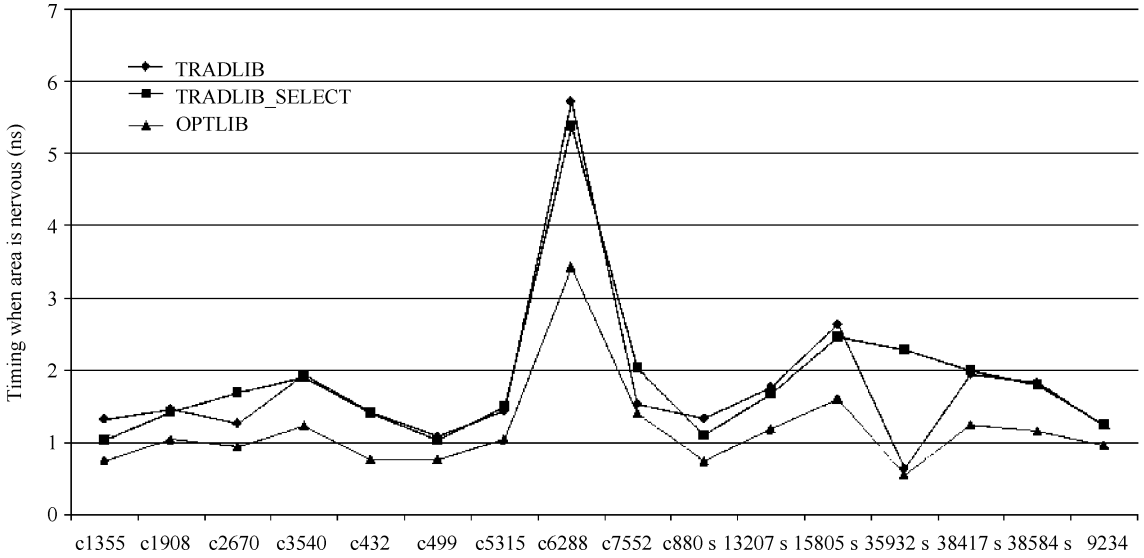


Fig. 7. Timing when area is nervous.

area and power in most VLSI design. The delay is important, because the critical path in a synthesized block may determine the clock frequency of the total chip, even though it is not major area-wise.

It can be proven from the above description and the synthesis result that the 65 nm DFM standard cell library has better performance compared with traditional standard cell library.

5.2. Manufacturing verification in foundry

The foundry always tests design-variability-index (DVI) and process-variability-index (PVI) to evaluate the manufacturing of a design. The DVI and PVI can be expressed as follows:

The DVI score indicates how likely it is that the variations in printing will negatively impact yield. It represents the proportion of the area under investigation that is problematic[9]. This index is best used by design teams to locate and assign priority to errors for correction. The LFD tool calculates the DVI as follows:

$$\mathrm{DVI} = \sum \frac{\mathrm{AREA(LFDerrors)}}{\mathrm{AREA(window)}}. \quad (1)$$

The PVI score indicates the degree to which printing is impacted by changes in the process[10]. It represents the ratio of PV-band layer data to target layer data. It is calculated as follows:

$$\mathrm{PVI} = \sum \frac{\mathrm{AREA(pvband(layer))}}{\mathrm{AREA(layer)}}. \quad (2)$$

The designer can get unreasonable position for lithography easily by taking advantage of the LFD (litho-friendly-design) kit provided by the foundry.

Currently the DFM standard cell library has passed the manufacturing of 65 nm process test from the Technology Design Department of the Foundry. The results of the test have been summarized below.

(1) The DVI of the DFM standard cell library is zero, which is tested by a manufacturing tool in the foundry.

(2) The PVI of the DFM standard cell library has been reduced by 10% regardless of whether the process is normal or

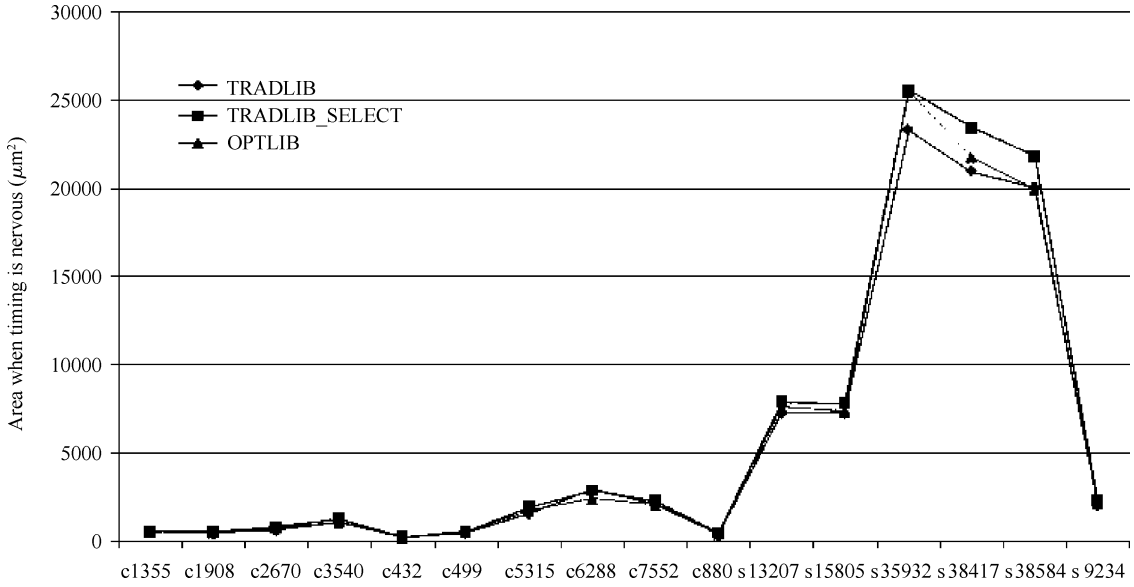


Fig. 8. Area when timing is nervous.

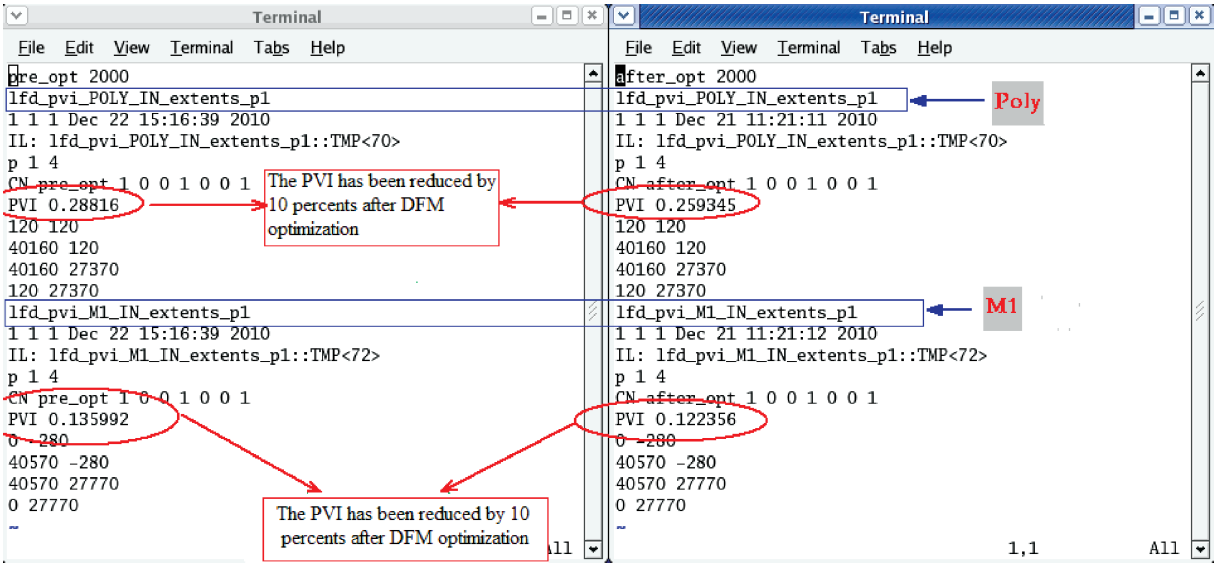


Fig. 9. Result of the PVI test for standard cells.

has process variations.

The result of the PVI test for the standard cells from the Technology Design Department of the Foundry is shown in Fig. 9. The DVI is zero which indicates that the design is LFD clean, and the lower PVI represents that the design has less unreasonable region for lithography. The result shows that the DFM standard cell library is advantageous to improve yield.

6. Conclusion

The design method which is proposed by this paper can help a designer to find out if a layout has some latent problems in manufacturing, and then edit the layout and fix them in time. It is a big advantage to improve the quality of IC design. Furthermore it brings advantage to OPC at the manufacture stage because of the smaller data size and a series of measures for layout optimization. The DFM standard cell library leads to a less than 5% increase in area compared with traditional standard cell library, and its timing, as well as power has a good performance. Furthermore, the library has passed the test from the Technology Design Department of the Foundry. The results shows high competence of the 65 nm DFM standard cell library compared to traditional libraries, of which the process-variability-index has been reduced nearly by 10%, and the design-variability-index is zero. The design method has definite value and is significant for reducing a designers' workload, shortening the design cycle as well as improving the chip yield.

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