A 65-nm low-noise low-cost ΣΔ modulator for audio applications*

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Abstract: This paper introduces a low-noise low-cost ΣΔ modulator for digital audio analog-to-digital conversion. By adopting a low-noise large-output swing operation amplifier, not only is the flicker noise greatly inhibited, but also the power consumption is reduced. Also the area cost is relatively small. The modulator was implemented in a SMIC standard 65-nm CMOS process. Measurement results show it can achieve 96 dB peak signal-to-noise plus distortion ratio (SNDR) and 105 dB dynamic range (DR) over the 22.05-kHz audio band and occupies 0.16 mm^2. The power consumption of the proposed modulator is 4.9 mW from a 2.5 V power supply, which is suitable for high-performance, low-cost audio codec applications.

Key words: ΣΔ modulator; low-noise; low-cost; analog-to-digital converter

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1. Introduction

With the rapid development of China's multi-media digital audio-video SOC chip, the industry itself has urgent demands of an independent CMOS based, high-performance, low-power and low-cost analog-to-digital converter (ADC). ΣΔ modulation provides an efficient method of signal conversion to achieve high resolution without high-accuracy analog building blocks. High-order single-loop and multi-bit quantizer ΣΔ architectures can realize sufficient low quantization noise, but they have poor linearity and take up a relatively large area[1, 2].

In this paper, a 2.5 V 4.9 mW 96 dB SNDR 2-1 cascaded ΣΔ modulator is implemented in 65-nm CMOS technology for audio applications. By adopting a low-noise large-output swing operation amplifier, the noise level can be attenuated to –130 dB and, in addition, it can use GND (ground) and VDD (power supply) as feedback voltages instead of v_{ref+} and v_{ref-} in most single-bit quantification cascaded ΣΔ modulators[3]. The power consumption can be greatly reduced, eliminating two feedback voltage buffers which are usually asked to be integrated in chip for convenience in industry.

2. Modulator architecture

The system architecture of the proposed ΣΔ modulator is shown in Fig. 1. To achieve an overall dynamic range of above 100 dB, a 3 order modulator with an oversample ratio of 128 is adopted. The reasons for choosing 2-1 cascaded architecture are as follows: firstly, cascading first and second order modulators eliminate the stability problems associated with high order single loop ones. Thus a higher input overload level is approached, which is suitable for rail-to-rail input modulators; secondly, baseband spectral tones are largely suppressed in cascaded modulators, which is desirable in high performance audio applications; thirdly, it is less sensitive to component mismatch[3, 4]. Non-idealities such as kT/C noise, amplifier slew rate and saturation voltage are considered in integrator 1. Figure 2 shows its Matlab model. Models of integrator 2 and integrator 3 are similar to integrator 1 except for the slew rate considerations since they are not usually limiting.

A single-bit quantizer is chosen for its high linearity, but it requires a larger output swing of the operation amplifier in first integrator. Figure 3 is the probability density functions of each integrator output voltage range (normalized by the power supply), which shows that the integrator 1 output voltage could probably reach 0.75, at which the operational transconductance amplifier (OTA) must have sufficient DC voltage gain as well as gain linearity, otherwise it will cause serious distortion.

Another reason for using the structure shown in Fig. 1 is that we can use small sampling and integration capacitors. This greatly affects the modulator's area cost since it's capacitors are dominant. In our design, 2 pF sampling capacitors are adopted. Simulation results show this structure can achieve 105.3 dB peak SNDR.

3. Circuit design

3.1. Circuit topology

Fully differential CMOS implementation of the modulator schematic is shown in Fig. 4. It consists of three switched-capacitor integrators and two comparators. All the building blocks are designed in an SMIC 65-nm CMOS mixed-signal process and work at 2.5 V supply. The reference voltages are selected as 2.5 and 0 V, which are conventionally v_{ref+} and v_{ref-} in most 2-1 cascaded single-bit quantification ΣΔ modulators. While v_{ref+} and v_{ref-} are usually generated by voltage references connected with buffers in chip for convenience. Considering the modulator's setup time, these two feedback

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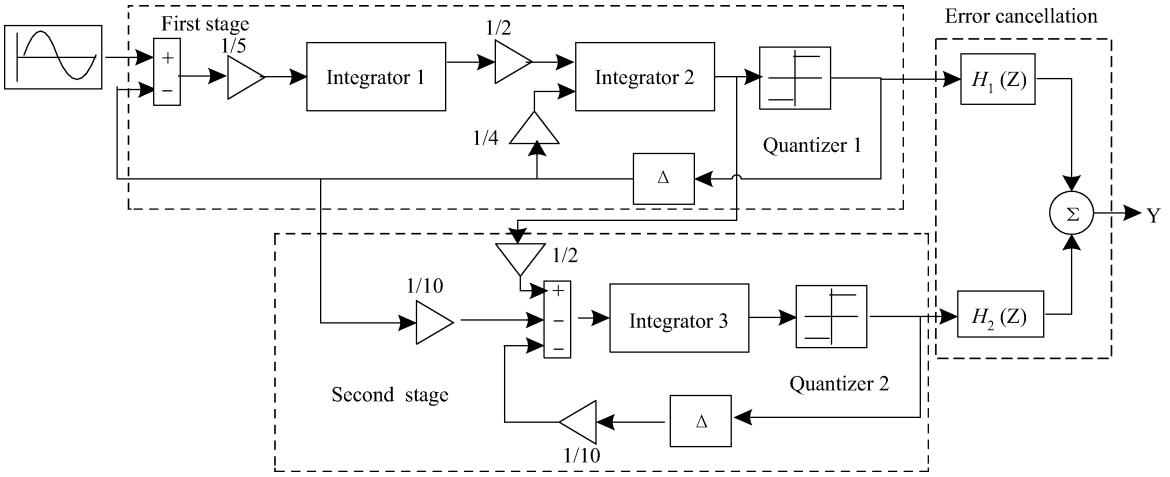

Fig. 1. Matlab block diagram of a 2-1 cascaded modulator.

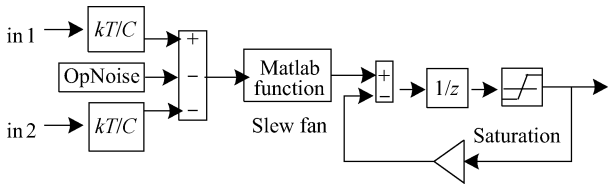

Fig. 2. Matlab model of the first integrator.

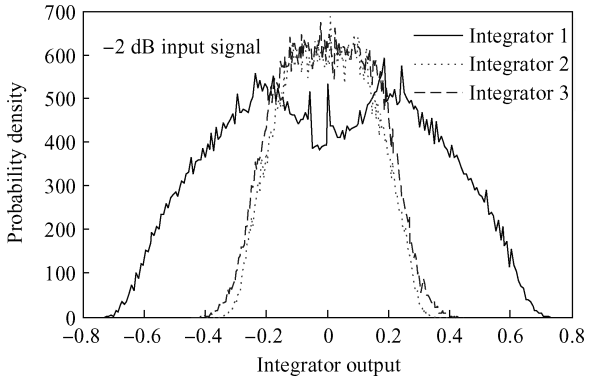

Fig. 3. Probability density functions integrator output.

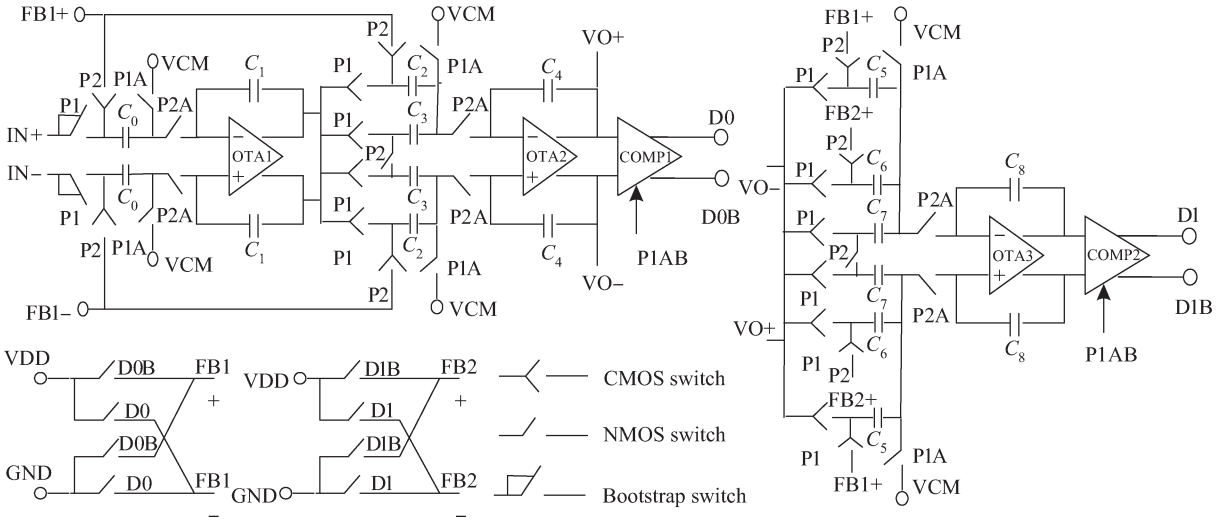

Fig. 4. Fully differential 2-1 cascaded single-bit ΣΔ modulator implemented with SC circuits.

voltage buffers should have strong driving capacity and that means a heavy current. So a large part of power consumption can be reduced by eliminating them. In addition, it also enlarges the modulator's input range to rail-to-rail. However, it requires an OTA with a large output swing, as Figure 3 shows.

The switched-capacitor integrators are controlled by two-phase, non-overlapping clocks, P1 and P2, advanced falling edge clocks, P1A and P2A, and a complement of P1AB, in order to suppress the channel charge injection, as Figure 5 shows. To enhance the linearity of the modulator, bootstrap switches are adopted in the first integrator, while CMOS or NMOS switches are used in others. C0, C2, C5, C6 are shared both in the integrate loop and the feedback loop for the purpose of reducing area cost [4, 5].

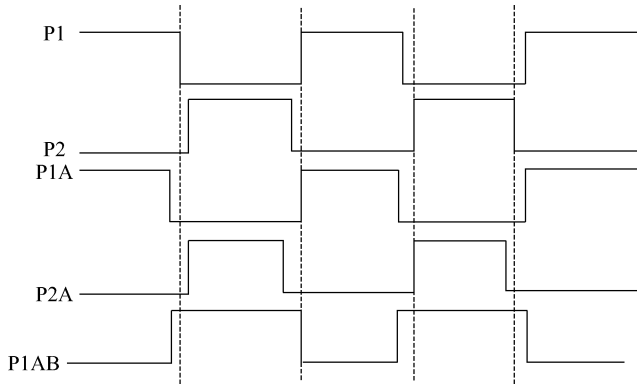

Fig. 5. Timing diagram of the clocks.

3.2. OTA

The OTA used in the integrators is the most critical block in a cascaded modulator. A class AB amplifier is usually used for their superior slew rate, but its noise performance is poor and the output swing is relatively limited with a cascade output stage for gain demand as shown in Fig. 3. A two-stage telescopic OTA is adopted for its high voltage gain, low power consumption and, most importantly, low noise. Figure 6 shows the details of the OTA circuit. A cascode is used in the first stage to get a high voltage gain, while the second stage uses a single NMOS with an active load to ensure a large output swing. A Miller capacitor introduces the first pole between two stages, and the output pole becomes the second one. With a compensatory resistor, the RHP (right half plane) zero can be cancelled. Therefore the OTA is stable. M14–M20 form a CMFB (common mode feedback) circuit. In this structure, the common mode and differential mode input stages share current mirrors and output loads. This not only reduces power consumption, but also equalizes the AC characteristic of these two paths. Moreover, once the differential loop is stable, the common loop is stable[6, 7].

Under the worst temperature and process corner conditions, simulation results show the proposed OTA in the first integrator achieves 87-dB DC gain, 80-MHz bandwidth, 65° phase margin with 1.06 μV inband input-referred noise, consuming 2.7 mW under 2.5 V power supply. Figure 7 shows its no-linear gain effect at different output range, and Figure 8 describes its frequency response. The OTAs in the second and third integrators are scaled versions of the first OTA. Due to the relaxed requirements of DC gain, bandwidth and capacitor load, the OTAs in the second and third integrators dissipate 0.8 mW, respectively.

3.3. Bootstrap switch

The linearity of sampling switches is very important to the modulator, which influences the harmonic distortion and intermodulation. Common CMOS switches cannot satisfy high linearity demand. Bootstrap switches are adopted in the first integrator in this design, as Figure 4 shows. The details of the bootstrap switch circuit are shown in Fig. 9. The switch is controlled by clock CLK. When CLK is low, M1 is off, making the switch off. The voltage on capacitor CP is pull up to VDD at the same time. As CLK becomes high, M8 is on and the voltage between gate and drain of M1 remains VDD, irrespective of input voltage. M5, M9 are used to ensure the reliability of the circuit. In 65-nm design, parasitic capacitance is relatively small compared to 0.18-μm or 0.13-μm, so CP is inclined to be smaller, reducing the chip area. Simulation results prove that the harmonic distortion of this switch is 50 dB less than a CMOS switch[8].

Table 1. Modulator performance summary.

Specification	Value
Power supply	2.5 V
Oversampling ratio	128
Bandwidth	22.05 kHz
Sampling rate	5.645 MHz
Power consumption	4.9 mW
SNDR	96 dB
Dynamic range	105 dB
Area	0.16 mm^2
FOM	2.15 pJ/step
Technology	65 nm

Table 2. Modulator performance comparison.

Parameter	Ref. [4]	Ref. [9]	Ref. [10]	This work
Technology (μm)	0.18	0.065	0.065	0.065
Supply (V)/ Power (mW)	3.3/6.9	3.3/0.9	1.2/3.3	2.5/4.9
Bandwidth (kHz)	22.05	15	100	22.05
SNDR (dB)	90	75	84	96
FOM (pJ/step)	5.4	6.5	1.27	2.15

4. Experimental results

The $\Sigma\Delta$ modulator proposed is implemented in a SMIC 65-nm CMOS mixed-signal process with metal–oxide–metal capacitors. The die layout is shown in Fig. 10. It occupies a core area of 0.39×0.41 mm^2.

The differential input sinusoidal signal is provided by APx525 audio analyzer and the 18 bit output digital codes are captured by Tektla6202 logic analyzer. A 6 MHz crystal oscillator is adopted for the clock signal, while the power supplies are generated by high efficient linear regulator LM1117. A 524288-point FFT of the output spectrum for a –3 dBFS, 1.53 kHz sinusoidal input is shown in Fig. 11. The spectrum demonstrates a flat noise floor free of spectrum tones since thermal noise limited. The peak-SNDR reaches 96 dB as shown in Fig. 11. An input level of 0 dBFS corresponds to a 5 V peak-to-peak sinusoidal signal. The DR is obtained through curve extension when the input is lower than 67 dB for the limitation of the signal generator. The dynamic range of the modulator achieves 105 dB as Figure 12 indicates. The power consumption of the modulator is 4.9 mW. Table 1 shows the modulator performance summary. Table 2 shows a comparison between recently published audio $\Sigma\Delta$ modulators[9, 10]. Reference [10] achieved 1.27 pJ/step FOM mostly due to its bandwidth contribution, while the proposed modulator achieved a FOM of 2.15 pJ/step.

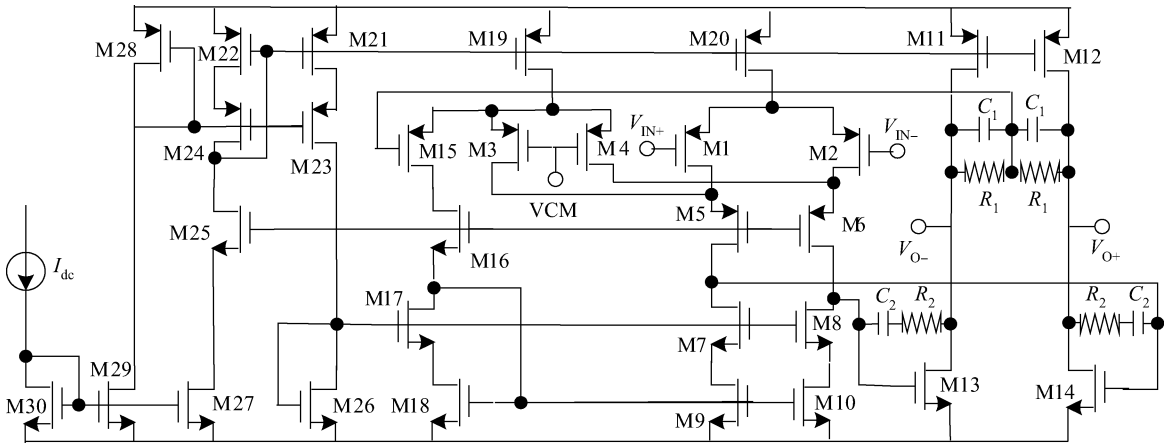

Fig. 6. Fully differential two-stage telescopic OTA with CMFB.

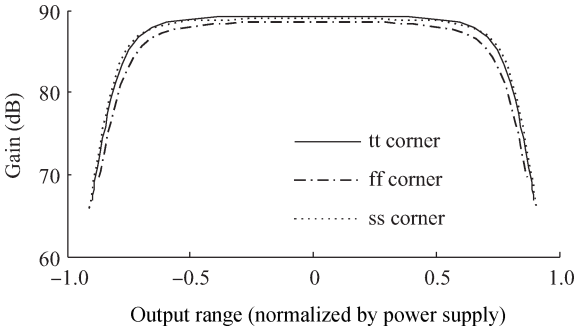

Fig. 7. No-linear gain effect of the OTA.

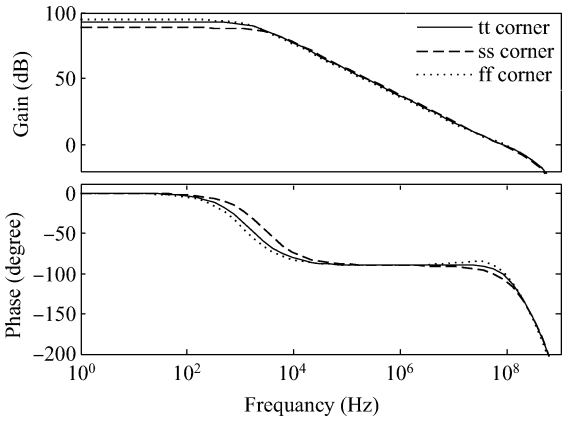

Fig. 8. Frequency response of the OTA.

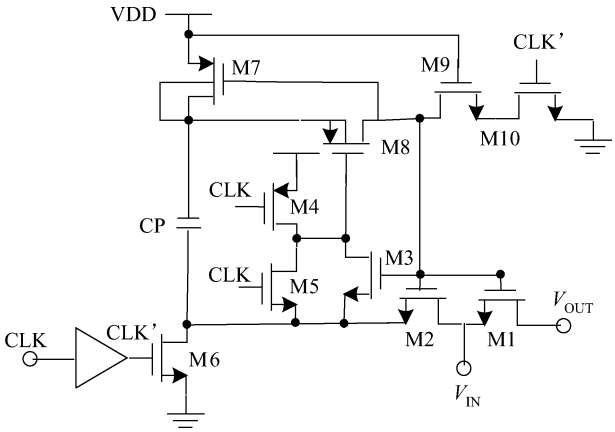

Fig. 9. Bootstrap switch.

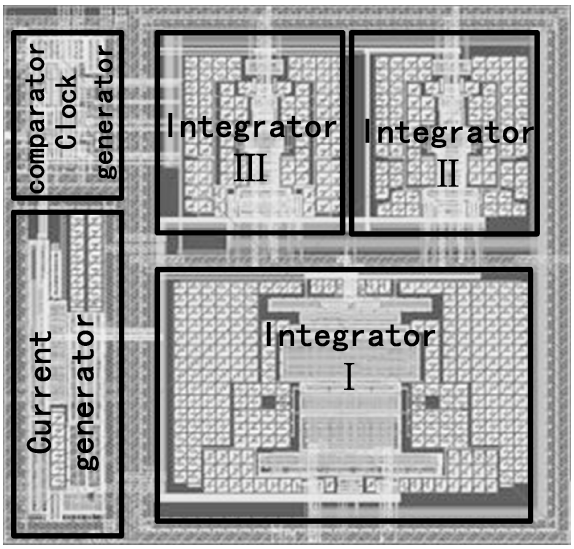

Fig. 10. Layout of the modulator.

5. Conclusion

A low noise, low cost ΣΔ modulator is proposed. With single-bit quantification and high linearity bootstrap switches, the modulator gets a high SNDR. Using low noise large output swing OTAs, not only can noise be greatly inhibited, but also the power consumption is reduced. In addition, its area cost is quite competitive. The modulator is designed in a SMIC 65-nm CMOS mixed-signal process. The measurement result shows that a 96-dB peak-SNDR and 105-dB peak-DR is achieved and the power consumption is 4.9 mW, and the FOM is 2.15 pJ/step.

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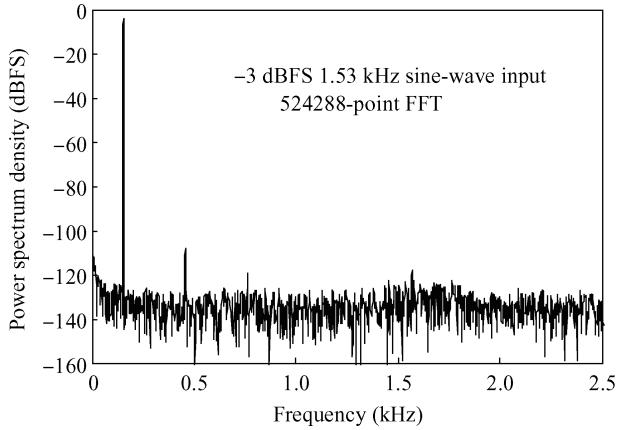

Fig. 11. Measured output spectrum of the modulator.

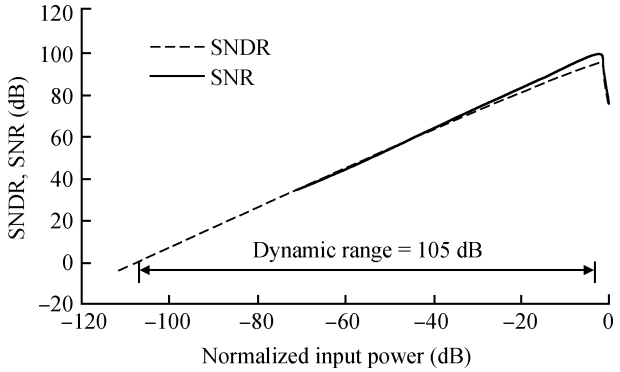

Fig. 12. Measured SNR and SNDR versus input signal power.

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