An offset cancellation technique in a switched-capacitor comparator for SAR ADCs*

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Abstract: An offset cancellation technique for a SAR (successive approximation register) ADC switched-capacitor comparator is described. The comparator is designed with a pre-amplifying and regenerative latching structure and realized in 0.18 μm CMOS. With the first stage preamplifier offset cancellation and low offset regenerative latching approach, the equivalent offset of the comparator is reduced to < 0.55 mV. By using the pre-amplifying and regenerative latching comparison mode the comparator exhibits low power dissipation. Under a 1.8 V power supply, with a 200 kS/s ADC sampling rate and 3 MHz clock frequency, a 13-bit comparison resolution is reached and less than 0.09 mW power dissipation is consumed. The superiority of this comparator is discussed and proved by the post-simulation and application to a 10 bit 200 kS/s touch screen SAR A/D converter.

Key words: A/D converter; switched-capacitor comparator; preamplifier; regenerative latch; low power; low offset

DOI: 10.1088/1674-4926/33/1/015011 **EEACC:** 2570D; 1285

1. Introduction

As the pivotal building blocks of SoC's (system-on-chip), A/D converters have been widely used in HDTV (high definition TV), wireless sensor nodes, touch screen controllers and other applications. SAR (successive approximation register) A/D converters are especially popular due to their simple architecture, small area and ease of integration with other IC blocks[1−4]. The comparator is an essential part of a SAR ADC and the design of a low power, low offset and high resolution comparator is very significant for SAR ADC realization. Though many CMOS comparators have been described in previous works, there are very few papers that focus on a switched-capacitor comparator based on SAR ADC operation. In Ref. [3], by using a self-timed comparator the power dissipation of a 12-bit fully- differential SAR ADC is reduced, but the operation and the offset cancellation of the comparator are not described. In Ref. [4], many structures of SAR ADC are discussed and a 10-bit low power SAR ADC is realized with an R–C hybrid structure, but the design of the comparator is not mentioned. In Ref. [5], two offset cancellation techniques are proposed for comparator design but these two techniques are not completely compatible with SAR ADC operation so additional logic control circuits are needed to guarantee the correct operation, increasing the complexity of the whole ADC design.

In this paper, a switched-capacitor comparator that is suitable to SAR ADC is described in detail. The operation, power dissipation and offset cancellation of the comparator are discussed based on SAR ADC operation. This comparator is especially compatible with the operation of charge redistribution, R–C and C–R hybrid SAR ADC, so no additional logic control signals need to be added. A 10 bit 200 kS/s SAR ADC with this comparator has been realized in 0.18 μm CMOS, and the simulation and measurement results can prove the applicability of this comparator to SAR A/D converters.

2. Structure of the proposed comparator

The typical structure of SAR A/D converter is shown in Fig. 1. As a key part of SAR ADC, the comparator is used to compare the sampled value of the input signal and the sub-references generated by the D/A network. It directly affects the performance of the converter, such as the offset, resolution, and power.

In this paper, a pseudo differential switched-capacitor comparator for SAR ADC is proposed as shown in Fig. 2. Not only is the sample-and-hold function of SAR ADC combined in this structure, but the input offset is dramatically reduced by the first stage preamplifier offset cancellation. The whole comparator is designed with a "pre-amplify + regenerative latching" approach, which improves the comparison speed through the combination of the negative exponential response of the pre-amplifier and the positive exponential response of the latch. The pre-amplifiers are used to amplify the differential

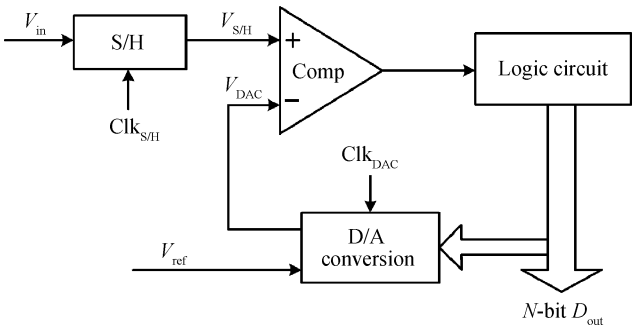

Fig. 1. A typical structure of SAR A/D converter.

* Project supported by the National Natural Science Foundation of China (Nos. 60725415, 60971066).
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Received 25 July 2011, revised manuscript received 8 October 2011

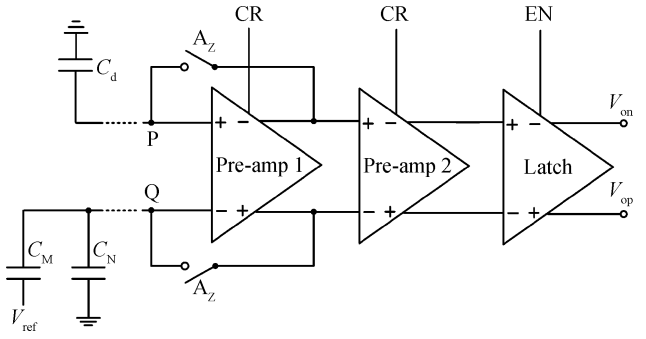

Fig. 2. Diagram of the comparator proposed.

input while the latch boosts the output of the preamplifier up to a desired output level. In the sampling phase, the entire capacitor array (C_M and C_N) is utilized to sample the input signal with the first pre-amplifier auto-zeroed. Then, $V_P = V_Q = V_{CM}$, where V_{CM} represents a common-mode voltage. By the end of the sampling phase, the information of the input signal can be stored at the input ports of the comparator with switches A_z turned off. In the comparison mode, based on the comparator output, the output of the D/A converter is controlled by the digital logic to approximate the sampled input successively. The capacitors C_M and C_N in Fig. 2 represent the total capacitors that connected to the reference V_{ref} and ground. C_d is used for reducing the input offset caused by the charge injection and clock feed-through of the auto-zero switches A_z.

3. Design of the switched-capacitor comparator

Based on the introduction of the comparator's application to SAR ADC, its architecture and operation in Section 2, the comparison approach, inherent offset cancellation compatible with SAR ADC operation, power and speed optimization will be described in this section.

3.1. "Pre-amplify + regenerative latching" approach

In this comparator, the comparison is finished with two pre-amplifiers followed by a regenerative latch. The two pre-amplifiers have a same structure as shown in Fig. 3. The cross-coupled positive feedback realized with M3 and M4 is used to increase the gain of the pre-amplifier, which can be seen from the expression:

$$A_{\text{pre-amp}} = \frac{g_{m1,2}}{g_{m5,6}} \frac{1}{1 - g_{m3,4}/g_{m5,6}}. \quad (1)$$

The second component in the right-hand of Eq. (1) represents the enhancement coefficient caused by the cross-coupled positive feedback. For a constant gain-bandwidth product, the increase of the gain can degrade the bandwidth of the comparator. Since SAR ADCs are usually used in low to medium speed applications, the pre-amplifiers are usually designed to be with a higher gain to reduce the total input offset of the comparator[6]. The tail current of the pre-amplifiers is a critical design variable for the comparator[7]. It is important to find an optimal compromise between a small bias current for low power dissipation and a large value to minimize noise and maximize the comparison rate. With the above consideration, the current

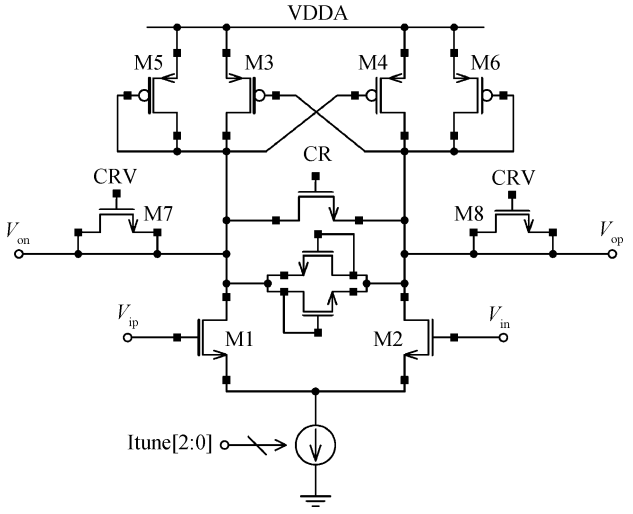

Fig. 3. Pre-amplifier of the comparator.

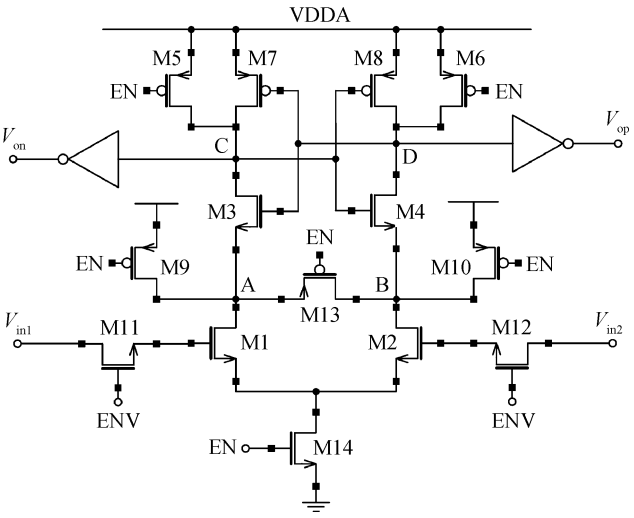

Fig. 4. Regenerative latch of the comparator.

of the comparator is designed to be tunable with the control of Itune[2:0]. In Fig. 3, the two MOSFETs connected between the differential outputs are used as clamped transistors to limit the output span. The signal CR is a recovery signal for reducing the settling time of the comparator, and the transistors M7 and M8 are used to cancel the charge injection caused by the recovery operation.

The regenerative latch of the comparator is shown in Fig. 4. When EN = "0" and ENV = "1", the internal nodes A–D are pre-charged to "1" with M5–M6 and M9–M13 turned on. Then, M14 is turned off and no static current flows from the power to the ground. When EN turns to "1", M5–M6 and M9–M13 turn off while M14 turns on. Then, M1 and M2 will convert the differential input voltages (V_{in1} and V_{in2}) to differential currents, making the internal nodes A and B to discharge with two different speeds. If $V_{in1} > V_{in2}$, the voltage of node A will decrease at higher speed. With the increase of V_{DA}, M3 turns on when $V_{DA} > V_{th3}$, making the voltages of nodes C and D not equal any more. The voltage of node C will decrease rapidly. Therefore, the outputs V_{on} and V_{op} of the regenerative latch will be "1" and "0" respectively. In Fig. 4, M9–M10 and M13 are used to

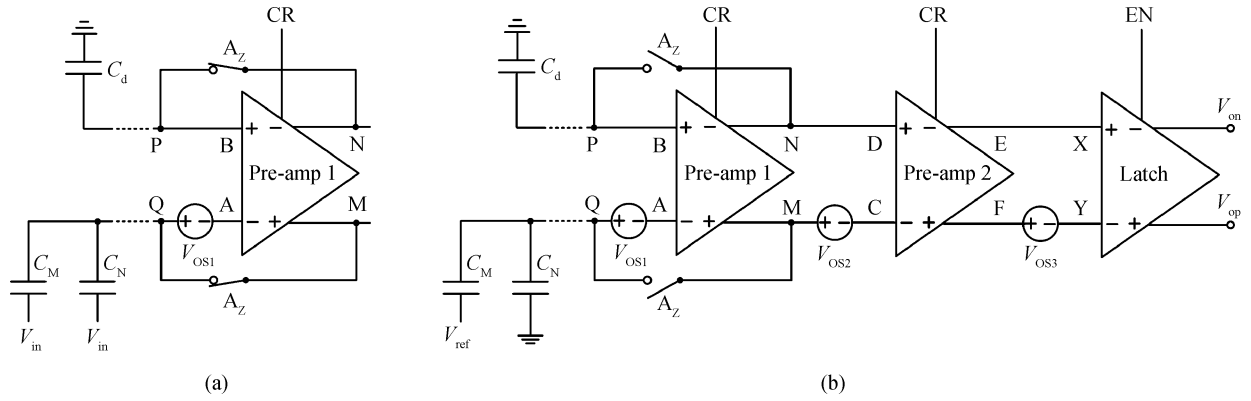

Fig. 5. Offset cancellation of the proposed comparator. (a) Sampling phase. (b) Approximation phase.

guarantee the nodes A and B to be at the same voltage level at the pre-charge phase, which reduces the input offset caused by the cross-coupled transistors M3–M4 and M7–M8. M11 and M12 are used to reduce the kickback noise of the regenerative latch.

3.2. Inherent offset cancellation compatible with SAR ADC operation

In SAR A/D converter, the input offset voltage of the comparator can directly affect the DC and AC performance of the converter[8]. As for this proposed pseudo differential switched-capacitor comparator, its inherent offset cancellation is fully compatible with the operation of SAR ADC, reducing the circuit complexity. The operation of the offset cancellation of this comparator is shown in Fig. 5.

In Fig. 5, $C_{\rm M}$ and $C_{\rm N}$ form the capacitor array of the D/A network in SAR ADC. Taking a "5 MSBs + 5 LSBs" C–R hybrid structure as an example, the total capacitance of the 5-bit capacitor array $C_{\rm T}$ ($C_{\rm T} = C_{\rm M} + C_{\rm N}$) equals $32C_0$. The dummy capacitor array $C_{\rm d}$ is used for reducing the input offset caused by the charge injection and clock feed-through of the auto-zero switches A_z. With $C_{\rm d}$ directly connected to ground, the capacitor array of the converter and the dummy array form a pseudo differential structure.

Based on the operation described in Section 2, in the sampling phase, the comparator is auto-zeroed with A_z turned on, as shown in Fig. 5(a). We can get: $-A_1(V_{\rm B}-V_{\rm A}) = V_{\rm N}-V_{\rm M} = V_{\rm P}-V_{\rm Q}$. Here, A_1 represents the gain of the first pre-amplifier. With $V_{\rm B} = V_{\rm P} = V_{\rm CM}$ and $V_{\rm A} = V_{\rm Q} - V_{\rm OS1}$, we get: $-A_1(V_{\rm P} - V_{\rm Q} + V_{\rm OS1}) = V_{\rm P} - V_{\rm Q}$. After rearrangement, we have:

$$V_{\rm Q} = V_{\rm P} + \frac{A_1 V_{\rm OS1}}{A_1 + 1} = V_{\rm CM} + \frac{A_1 V_{\rm OS1}}{A_1 + 1}. \tag{2}$$

By the end of the approximation phase as shown in Fig. 5(b), $V_{\rm X}$ should be equal to $V_{\rm Y}$. Taking the offset of the second stage pre-amplifier $V_{\rm OS2}$ and the latch offset $V_{\rm OS3}$ into consideration, at the nodes P and Q we have $V'_{\rm P} = V_{\rm CM}$ and:

$$V'_{\rm Q} = V_{\rm CM} + V_{\rm OS1} + \frac{V_{\rm OS2}}{A_1} + \frac{V_{\rm OS3}}{A_1 A_2}. \tag{3}$$

Based on the charge conservation at node Q in the sampling and approximation phase, we have:

$$\left(V_{\rm Q} - V_{\rm in}\right) C_{\rm T} = \left(V'_{\rm Q} - V_{\rm ref}\right) C_{\rm M} + V'_{\rm Q} C_{\rm N}. \tag{4}$$

Substituting Eqs. (2) and (3) into Eq. (4), we can get:

$$V_{\rm in} = \frac{V_{\rm ref} C_{\rm M}}{C_{\rm T}} - \left(\frac{V_{\rm OS1}}{A_1 + 1} + \frac{V_{\rm OS2}}{A_1} + \frac{V_{\rm OS3}}{A_1 A_2}\right). \tag{5}$$

Then, the equivalent input offset $V_{\rm OS}$ of the comparator can be calculated as below:

$$V_{\rm OS} = \frac{V_{\rm OS1}}{A_1 + 1} + \frac{V_{\rm OS2}}{A_1} + \frac{V_{\rm OS3}}{A_1 A_2}. \tag{6}$$

It is obvious from Eq. (6) that the offset of the first stage pre-amplifier is divided by $A_1 + 1$, and the equivalent input offset of the comparator is dramatically reduced. This advantage is compatible with the operation of the SAR ADC and is achieved without any additional circuit complexity.

4. Design results and discussion

The switched-capacitor comparator proposed in this paper is designed based on a 0.18 μm CMOS 1.8 V device model. Under the condition of typical SAR ADC application, the design results of the comparator show that it realizes high resolution and low offset with low power dissipation and a small area.

4.1. Simulation results

With the "pre-amplify + regenerative latching" comparison approach, this comparator achieves high resolution at a proper speed with low power. The pre-amplifiers are used to amplify a small signal to a larger level, which can turn on the latch. The latch boosts this amplified value up to a full span. The gain of the first and the second pre-amplifiers (A1 and A2) are designed to be about 35.2 and 16 respectively. Under a 1.8 V supply and 3 MHz comparison speed, the minimum input value that can be recognized by the comparator is less than 0.22 mV, reaching a resolution of about 13-bit. The power dissipation is about 86 μW. The post-simulation result of the current can be shown in Fig. 6. The average current is about 48 μA.

A constant comparator offset will appear as a static shift in the overall transfer characteristic of the ADC. If a mismatch exists between the input transistors M1 and M2, then their effect on the pre-amplifier's offset can be assumed to be an offset voltage $V_{\rm OS1,2}$ connected between the gate of M1 and the input

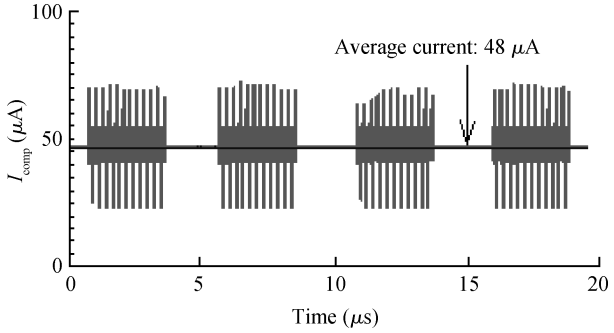

Fig. 6. Post-simulation result of the comparator current.

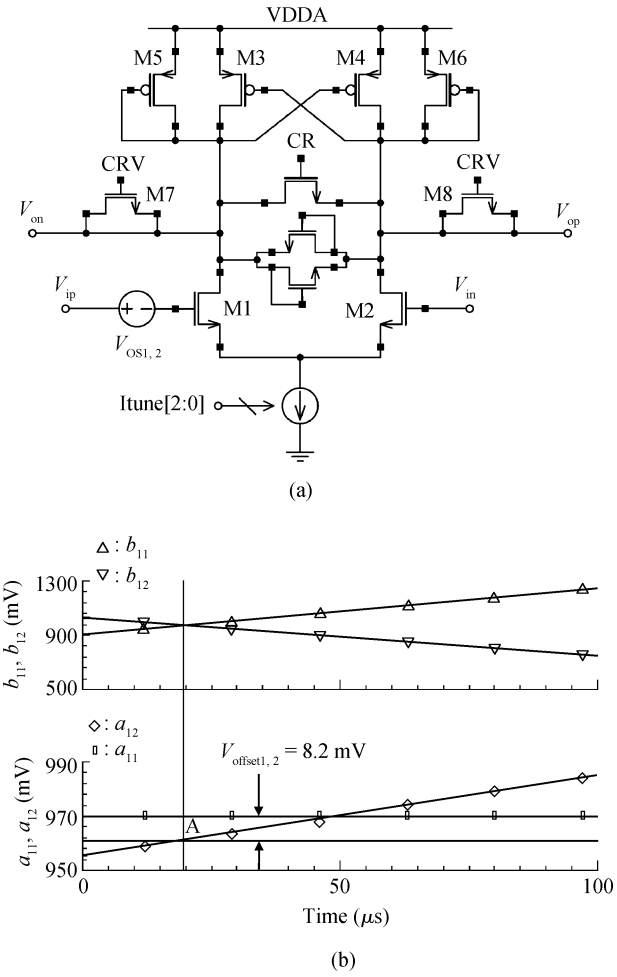

Fig. 7. Post-simulation of the pre-amplifier's offset. (a) Simulation circuit. (b) Simulation result.

signal, as shown in Fig. 7(a). From Ref. [5], $V_{OS1,2}$ is calculated as bellow:

$$V_{OS1,2} = \Delta V_{TH1,2} + \frac{1}{2}\left(\frac{\Delta W_{1,2}}{W_{1,2}} - \frac{\Delta L_{1,2}}{L_{1,2}}\right) V_{dsat1,2}. \quad (7)$$

Here, $\Delta V_{TH1,2}$ is the standard deviation of the mismatch between M1 and M2 in threshold voltage. $\Delta W_{1,2}$ and $\Delta L_{1,2}$ are the standard deviation of the mismatch between M1 and M2 in size. $V_{dsat1,2}$ is the initial overdrive voltage of M1 and M2. Based on the mismatch model of the 0.18 μm CMOS, $V_{OS1,2}$ is calculated to be 8.2 mV from Eq. (7). By adding

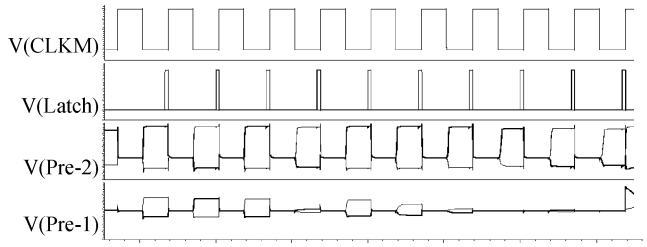

Fig. 8. Post-simulation result of the comparator for SAR A/D converter.

this DC voltage source $V_{OS1,2}$ as shown in Fig. 7(a), a post-simulation is made. The simulation result is shown in Fig. 7(b). When $V_{op} = V_{on}$, the difference between V_{ip} and V_{in} is the pre-amplifier's offset caused by the mismatch between M1 and M2. In Fig. 7(b), b_{11} and b_{12} represent V_{on} and V_{op}, and a_{11} and a_{12} represent V_{ip} and V_{in}, respectively. With this method, the pre-amplifier's offset caused by the mismatch between M1 and M2, M3 and M4, M5 and M6 can be found. Here, we represent them as $V_{offset1,2}$, $V_{offset3,4}$, and $V_{offset5,6}$, respectively. $V_{offset1,2}$ = 8.2 mV, $V_{offset3,4}$ = 0.83 mV, and $V_{offset5,6}$ = 1.2 mV. The equivalent input offset of the first pre-amplifier can be expressed as:

$$V_{OS1} = \sqrt{V_{offset1,2}^2 + V_{offset3,4}^2 + V_{offset5,6}^2}. \quad (8)$$

Based on the simulation and calculation method, the offset of pre-amp 1, pre-amp 2 and the latch are found. Here, we represent them as V_{OS1}, V_{OS2}, and V_{OS3}, respectively, and we get V_{OS1} = 8.33 mV, V_{OS2} = 9.8 mV and V_{OS3} = 20.7 mV. Substituting V_{OS1}, V_{OS2}, V_{OS3}, A_1 and A_2 into Eq. (6), we find the offset of the comparator to be 0.55 mV, which is about 0.31 LSB under 1.8 V power supply for a 10-bit ADC.

Under a condition of 200 kS/s A/D conversion rate and 3 MHz clock frequency, the post-simulation result of the entire comparator is shown in Fig. 8. The production of a code needs 15 clock cycles, in which the first 5 cycles are used for sampling and the others for generating the 10-bit output. In this comparator design, the latching process can be finished in 1/13 clock period, making enough time (12/13 clock period) for the internal D/A conversion and pre-amplification. The regenerative latch works at high speed and consumes no static power, making the compromise between power and speed easy.

4.2. Measurement results

This high performance pseudo differential switched-capacitor comparator is realized in 0.18 μm CMOS, and has been successfully utilized in a 10-bit 200 kS/s touch screen SAR A/D converter[9], as shown in Fig. 9. The area of the whole converter is 333 × 250 μm^2, where the comparator occupies an area of about 173 × 30 μm^2.

As for the resolution, this ADC using the proposed comparator has an ENOB of 9.15 with a 91 kHz input signal sampled at 200 kS/s. Figure 10 shows an 8000 point DFT spectrum for a 91 kHz single-ended sinusoidal input signal. This measurement result has proved the applicability of the proposed comparator to SAR ADC. The ADC's imperfection in the AC performance is mainly caused by the switches in the internal

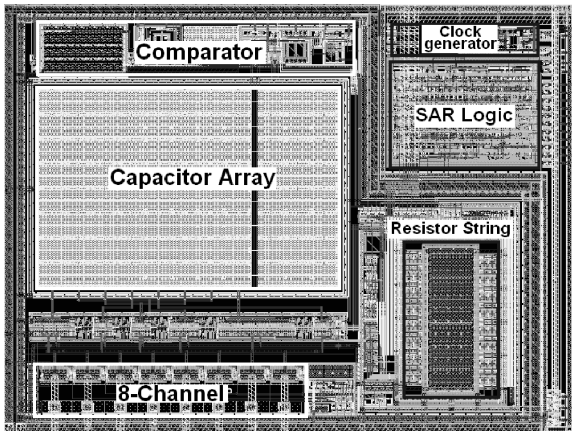

Fig. 9. A 10-bit SAR ADC with the proposed comparator.

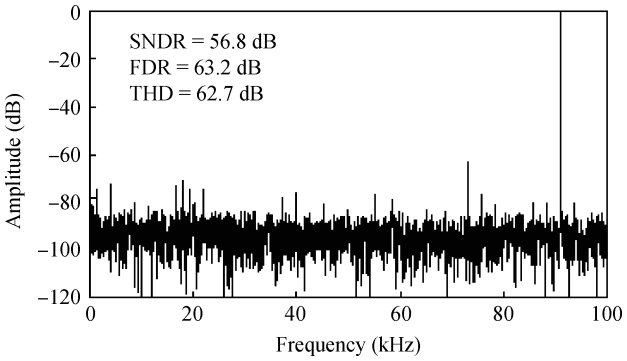

Fig. 10. DFT with 91 kHz input of the ADC with the proposed comparator.

D/A network, rather than the proposed comparator. As for the DC performance, the offset of the 10-bit ADC is measured to be less than 0.4 LSB, which is mainly caused by the mismatch of the D/A network and the offset of the proposed comparator. This 0.4 LSB ADC offset proves the low-offset merit of the proposed comparator. Since the power supply of the proposed comparator is common-used in the whole converter, the comparator's power is not measured independently. But the 10-bit ADC consumes 136 μW, which is very similar to the post-simulation result. It can be inferred that this silicon proved comparator does not vary too much in power dissipation.

4.3. Comparison with previous works

The analysis, simulation and measurement results show that this proposed comparator displays high performance. Low power and relatively high resolution are realized in a small area. Without adding any circuit complexity, low offset is realized with its inherent offset cancellation compatible with SAR ADC operation.

In Ref. [3], a self-timed comparator is proposed to reduce the power dissipation. Compared to this approach, the comparator proposed in this paper is also low power, and is even simpler in structure and logic control. And the FoM (figure-of-merit) of the ADC with the proposed comparator is less than 1.2 pJ/conversion step, which is better than the 4.83 pJ/conversion step of the ADC in Ref. [3]. In Ref. [5], two offset cancellation techniques IOS and OOS are proposed. But additional time should be given for the offset storage phase and an additional control logic circuit is needed in both of them. But the comparator proposed in this paper is completely compatible with SAR ADC operation. No additional control signal is needed.

5. Conclusion

A 0.18 μm CMOS pseudo-differential switched-capacitor comparator is realized for a SAR ADC design in this paper. The "pre-amplify + regenerative latching" comparison mode is utilized to reduce the power dissipation of the comparator. By using the first stage preamplifier offset cancellation and low offset regenerative latching approach, the comparator's equivalent input offset is reduced. Under the condition of 1.8 V power supply, 200 kS/s ADC sampling rate and 3 MHz clock frequency, the comparator features 13 bit resolution. The input offset is no more than 0.55 mV and the power dissipation is less than 0.09 mW. This low power, low offset and high resolution comparator is compatible with SAR ADC operation and has been successfully applied to a 200 kS/s touch screen SAR ADC IP core.

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