A feedforward compensation design in critical conduction mode boost power factor correction for low-power low total harmonic distortion*

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Abstract: For low-power low total harmonic distortion (THD), based on the CSMC 0.5 μm BCD process, a novel boost power factor correction (PFC) converter in critical conduction mode is discussed and analyzed. Feedforward compensation design is introduced in order to increase the PWM duty cycle and supply more conversion energy near the input voltage zero-crossing points, thus regulating the inductor current of the PFC converter and compensating the system loop gain change with ac line voltage. Both theoretical and practical results reveal that the proposed PFC converter with feedforward compensation cell has better power factor and THD performance, and is suitable for low-power low THD design applications. The experimental THD of the boost PFC converter is 4.5%, the start-up current is 54 μA, the stable operating current is 3.85 mA, the power factor is 0.998 and the efficiency is 95.2%.

Key words: CRM; boost PFC; low-power; THD; feedforward compensation
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1. Introduction

A boost power factor correction (PFC) converter operating in critical conduction mode (CRM) is a very popular topology for the front-end converter of many low-power electronics systems[1−3]. Compared with discontinuous conduction mode (DCM) or continuous conduction mode (CCM) boost converters, a CRM boost converter has lower power losses for the turn-on with zero-voltage switching and operates in varying frequency mode, which eliminates diode reverse recovery losses, with a smaller peak inductor current, lower turn-off switching and conduction losses[2]. However, as a function of the input line voltage and loads, the varying frequency mode could lead to excessive system losses for the power switch, inductor and core circuits, and eventually bring about a lower power factor (PF) and higher total harmonic distortion (THD). The most effective measure to avoid the drawback of the CRM boost PFC converter above is to limit the switching frequency by fixing the turn-on time. But this could result in input line current distortion, especially near the input voltage zero-crossing called valley switching (VS), which is mainly due to the resonance between the parasitic capacitances of the switch and the freewheeling diode with the boost inductor. Therefore it is necessary to develop new techniques to eliminate the effects of resonance.

This paper presents a novel feedforward compensation design for the CRM boost PFC converter, for the purpose of compensating the system loop gain change with ac line voltage, with a better PF and THD performance. Based on the CSMC 0.5 μm BCD process, the proposed PFC converter has been verified, and both simulation and testing results have revealed that the CRM boost PFC converter has significantly reduced the harmonic current and restrained the nonlinearity phenomenon and the frequency limits of the system. It is suitable for electronic equipment with strict standby power and harmonic regulations, such as ballasts, notebook adapters, and LCDs.

2. System description

The topology of the CRM boost PFC converter is shown in Fig. 1. The system is made up of two control loops, the internal voltage loop and the external current loop. In the voltage loop, the analog multiplier is the key module that could achieve multiplication of the sampling input line voltage V_i and the feedback control voltage V_c generated by the error amplifier with frequency compensation block, thereby compelling the input current to be sinusoidal and in phase with the input voltage[4,5] and completing power factor correction function. To eliminate distortions as far as possible, a self-starting timer is introduced[6]. Because the switching frequency T_s is much smaller than the frequency of the AC input line voltage T_l, the output voltage V_{out} can be considered as a constant during one switching period[7]. The state equation of the CRM boost PFC can be expressed as

$$\begin{cases} \dfrac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}t} = -\dfrac{v_{\mathrm{out}}}{R_{\mathrm{load}}C_{\mathrm{o}}} + \dfrac{(1-d)i_{\mathrm{L}}}{C_{\mathrm{o}}}, \\ \dfrac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t} = -\dfrac{(1-d)v_{\mathrm{out}}}{L} + \dfrac{v_{\mathrm{in}}}{L}, \end{cases} \tag{1}$$

where

$$v_{\mathrm{in}}(t) = \sqrt{2}V_{\mathrm{in,\,rms}}\sin(2\pi f_l t). \tag{2}$$

The stable working condition for PFC is depicted as $|i_{n+1}/i_n| < 1$, that is, the system must converge. Assuming

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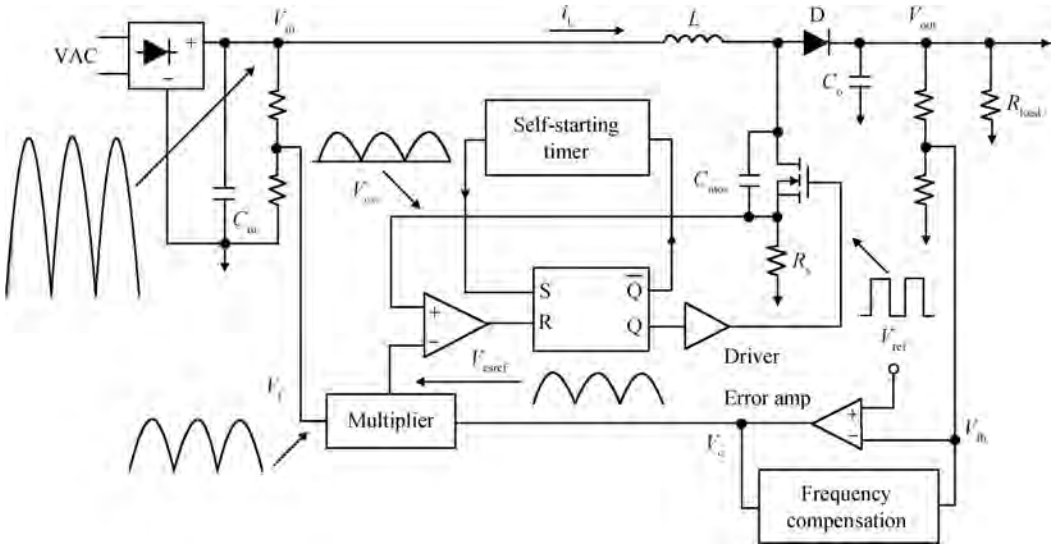

Fig. 1. CRM boost PFC topology.

that i_n and i_{n+1} are the input currents, respectively, at $t = nT_s$ and $(n + 1)T_s$, then

$$\begin{cases} \dfrac{i_{\text{csref}} - i_{n+1}}{(1-d)T_s} = \dfrac{v_{\text{out}} - v_{\text{in}}}{L}, \\ \dfrac{i_{\text{csref}} - i_n}{dT_s} = \dfrac{v_{\text{in}}}{L}. \end{cases} \tag{3}$$

Equation (3) can be given as

$$i_{n+1} = \left(1 - \frac{v_{\text{out}}}{v_{\text{in}}}\right) i_n + \frac{i_{\text{csref}} v_{\text{out}}}{v_{\text{in}}} - \frac{(v_{\text{out}} - v_{\text{in}})T_s}{L}. \tag{4}$$

Simplifying and eliminating the current items, the stability criterion of the system is

$$i_{\text{csref}} \leqslant \frac{v_{\text{in}}}{R_{\text{load}}} \left[\frac{R_{\text{load}} T_s d}{2L} + \frac{1}{(1-d)^2} \right], \tag{5}$$

where

$$d(t) = k_1 V_i (V_{\text{ref}} - v_{\text{out}}) - k_2 i_L, \tag{6}$$

where k_1 and k_2 are the gains of the voltage loop and current loop, respectively. The smaller the gain, the more stable the system. But the loop gain cannot be infinite to avoid a poor dynamic response. In practical application, an appropriate loop gain could enhance the system stability and reduce the noise both from the ac input and the converter itself. As shown in Eqs. (5) and (6), at VS the AC line voltage V_{in} and the sampling voltage V_i reach the min, and the duty cycle d decreases, as does the reference current i_{csref}, which increases the switching frequency and finally the system power. At the same time, this will bring about a delay in turn-on switching because of the parasitic capacitances resonating with the inductor. During this delay time, the stored charge of the C_{mos} (the MOSFET output capacitance) is discharged and transferred into a small filter capacitor C_{IN} with a negative current across the inductor i_L. The switching waveforms are shown in Fig. 2.

As Figure 2 shows, the negative inductor current i_{neg} extends the turn-off switching time t_{off}. The switch could not turn

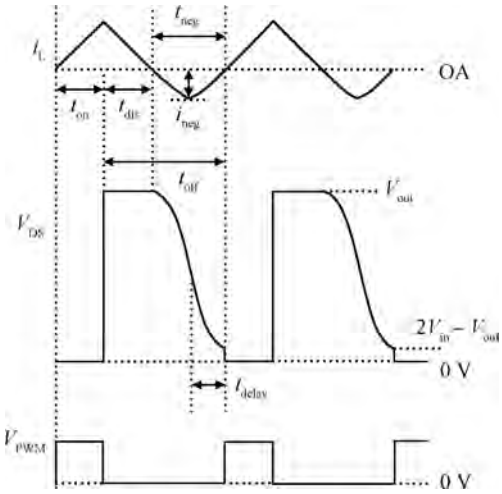

Fig. 2. Switching waveforms.

on until the current through the inductor returns to zero. During the time t_{neg}, the drain–source voltage of MOSFET V_{DS} reduces at a limited slope, which causes additional power losses. t_{neg} is proportional to $(V_{\text{out}} - V_{\text{in}})$, so at VS the parasitic capacitances cause a longer switch period with a smaller d, correspondingly, thereby resulting in the current distortions. Essentially, the distortions are caused by the instability of the system conversion energy. This instability is amplified by the high-frequency input filter capacitor, and makes the bridge rectifier diodes reverse-biased, and thus the input current deviates from the envelope of the input voltage and leads to current distortion. Therefore, as long as more conversion energy can be supplied at VS, the distortion is reduced accordingly.

3. The feedforward compensation design

As mentioned above, for better PF and THD, eliminating distortions and switching-frequency limitation is needed to provide more conversion energy for the system at VS. A specific method is increasing the conversion rate near VS to

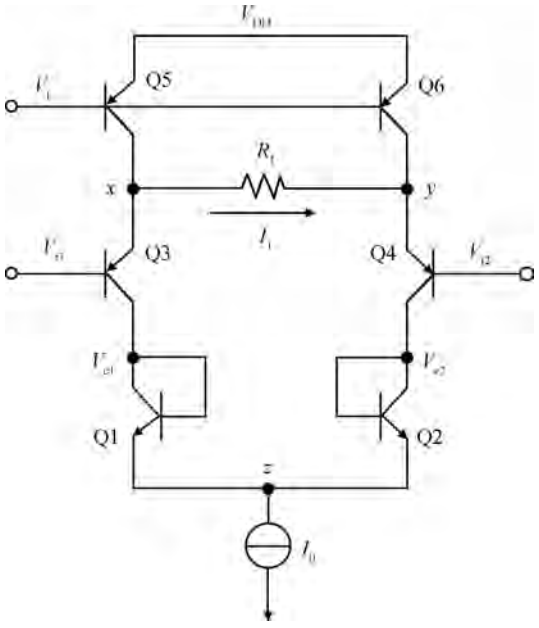

Fig. 3. A $1/V_{\rm l}^2$ feedforward compensation block.

discharge the input capacitor fully. A feedforward control compensation cell is introduced to supply the additional conversion energy at VS by increasing the duty cycle d. This is realized by embedding the $1/V_{\rm l}^2$ generating circuit (where $V_{\rm l}$ is proportional to the input line voltage) into the voltage control loop to make the multiplier output signal $V_{\rm csref}$ inversely proportional to the square of the input line voltage, that is, inversely proportional to the conversion energy, thus suppressing distortions. The $1/V_{\rm l}^2$ feedforward control cell could regulate the current reference of the system and compensate the system loop gain change with AC line voltage. The circuit topology is depicted in Fig. 3.

Supposing all the transistors matched, the current through transistors Q5 and Q6 is equal, there is

$$I_{\rm c5} = I_{\rm c6} = I_{\rm c3} + I_1 = I_{\rm c4} - I_1 = I_{\rm s} \exp \frac{V_{\rm DD} - V_{\rm l}}{V_{\rm T}} = \frac{I_0}{2}, \tag{7}$$

where $I_{\rm c3} + I_{\rm c4} = I_{\rm c5} + I_{\rm c6}$, then

$$I_{\rm s} \exp \frac{V_{\rm x} - V_{\rm i1}}{V_{\rm T}} + I_{\rm s} \exp \frac{V_{\rm y} - V_{\rm i2}}{V_{\rm T}} = 2I_{\rm s} \exp \frac{V_{\rm DD} - V_{\rm l}}{V_{\rm T}}. \tag{8}$$

For $V_{\rm i} = V_{\rm i1} - V_{\rm i2}$, $R_1 I_1 = V_x - V_y$, and from Eq. (7) it can be gotten,

$$I_{\rm c4} - I_{\rm c3} = 2\frac{V_x - V_y}{R_1} = I_{\rm s}\left(\exp \frac{V_y - V_{\rm i2}}{V_{\rm T}} - \exp \frac{V_x - V_{\rm i1}}{V_{\rm T}}\right). \tag{9}$$

Combining with Eqs. (8) and (9) gives

$$\frac{\exp \dfrac{V_y - V_{\rm i2}}{V_{\rm T}} - \exp \dfrac{V_x - V_{\rm i1}}{V_{\rm T}}}{\exp \dfrac{V_y - V_{\rm i2}}{V_{\rm T}} + \exp \dfrac{V_x - V_{\rm i1}}{V_{\rm T}}} = \frac{2\dfrac{V_x - V_y}{R_1 I_{\rm s}}}{\exp\left(\dfrac{V_{\rm DD} - V_{\rm l}}{V_{\rm T}}\right)^2} \approx \frac{(V_{\rm i1} - V_{\rm i2}) - (V_x - V_y)}{2V_{\rm T}}. \tag{10}$$

Simplify the formulas above, then

$$V_x - V_y = \frac{V_{\rm i1} - V_{\rm i2}}{1 + \dfrac{4V_{\rm T}}{I_{\rm s}R_1} \exp\left[-\left(\dfrac{V_{\rm DD} - V_{\rm l}}{V_{\rm T}}\right)^2\right]}. \tag{11}$$

As shown in Fig. 3, $I_{\rm c3} = I_{\rm c1}$ and $I_{\rm c4} = I_{\rm c2}$, so

$$\frac{\exp \dfrac{V_{\rm o1} - V_z}{V_{\rm T}}}{\exp \dfrac{V_{\rm o2} - V_z}{V_{\rm T}}} = \frac{\exp \dfrac{V_x - V_{\rm i1}}{V_{\rm T}}}{\exp \dfrac{V_y - V_{\rm i2}}{V_{\rm T}}}. \tag{12}$$

That is

$$\exp \frac{V_{\rm o1} - V_{\rm o2}}{V_{\rm T}} = \exp \frac{V_x - V_y - V_{\rm i1} + V_{\rm i2}}{V_{\rm T}}. \tag{13}$$

So

$$V_{\rm o1} - V_{\rm o2} = (V_x - V_y) - (V_{\rm i1} - V_{\rm i2}). \tag{14}$$

Substitute Eq. (11) into Eq. (14),

$$V_{\rm o1} - V_{\rm o2} \approx -\frac{4V_{\rm T}(V_{\rm i1} - V_{\rm i2})}{I_{\rm s}R_1\left(\dfrac{V_{\rm DD} - V_{\rm l}}{V_{\rm T}}\right)^2 + I_{\rm s}R_1 + 4V_{\rm T}}. \tag{15}$$

Obviously, the output signal $V_{\rm o1} - V_{\rm o2}$ is a function of $1/V_{\rm l}^2$ and $V_{\rm i}$, which is used as one of the input signals of the multiplier. Thus, the feedforward voltage $V_{\rm l}$ has been injected into the current reference to compensate the system loop gain and reduce the current distortion.

The analog multiplier topology with the $1/V_{\rm l}^2$ feedforward compensation cell is shown in Fig. 4. It is a typical four-quadrant Gilbert cell which uses the cascading differential pair to expand the input voltage range at the cost of the voltage redundancy[8]. The Q15 is used as a β-help transistor to improve the accuracy of the current mirror Q13–Q14. The output current $I_{\rm out}$ flows through the Wilson current mirror and produces $I_{\rm csref}$, which is used as the current reference of the PFC converter. The Wilson current mirror utilizes the negative feedback principle to further improve the temperature stability of the mirror output signal, and increases the dynamic output resistance and load capacity.

It can be seen that Gilbert completes the multiplication of two analog voltage signals $V_{\rm c}$ and $V_{\rm o1} - V_{\rm o2}$. Both could change from positive to negative continuously. The output current reference is

$$I_{\rm csref} = \frac{1 - \exp \dfrac{V_{\rm c}}{V_{\rm T}}}{1 + \exp \dfrac{V_{\rm c}}{V_{\rm T}}} I_{\rm c11} + \frac{\exp \dfrac{V_{\rm c}}{V_{\rm T}} - 1}{\exp \dfrac{V_{\rm c}}{V_{\rm T}} + 1} I_{\rm c12} \approx -\frac{V_{\rm c} I_{\rm c11}}{2V_{\rm T}} + \frac{V_{\rm c} I_{\rm c12}}{2V_{\rm T}}, \tag{16}$$

where $I_{\rm c11} = \frac{I_0}{1+\exp(V_{\rm o}/V_{\rm T})}$, $I_{\rm c12} = \frac{I_0 \exp(V_{\rm o}/V_{\rm T})}{1+\exp(V_{\rm o}/V_{\rm T})}$, $V_{\rm o} = V_{\rm o1} - V_{\rm o2}$, simplify Eq. (16),

$$I_{\rm csref} \approx \frac{V_{\rm c} I_0}{2V_{\rm T}} \frac{\exp(V_{\rm o}/V_{\rm T}) - 1}{\exp(V_{\rm o}/V_{\rm T}) + 1} = \frac{V_{\rm c} V_{\rm o} I_0}{4V_{\rm T}^2}. \tag{17}$$

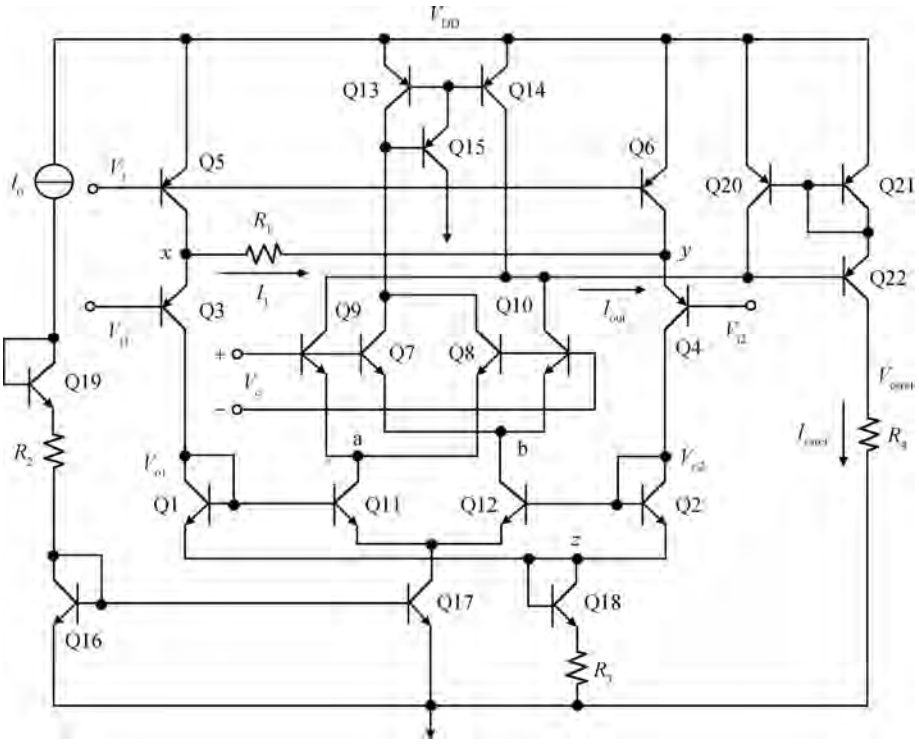

Fig. 4. Analog multiplier with a $1/V_1^2$ feedforward compensation cell.

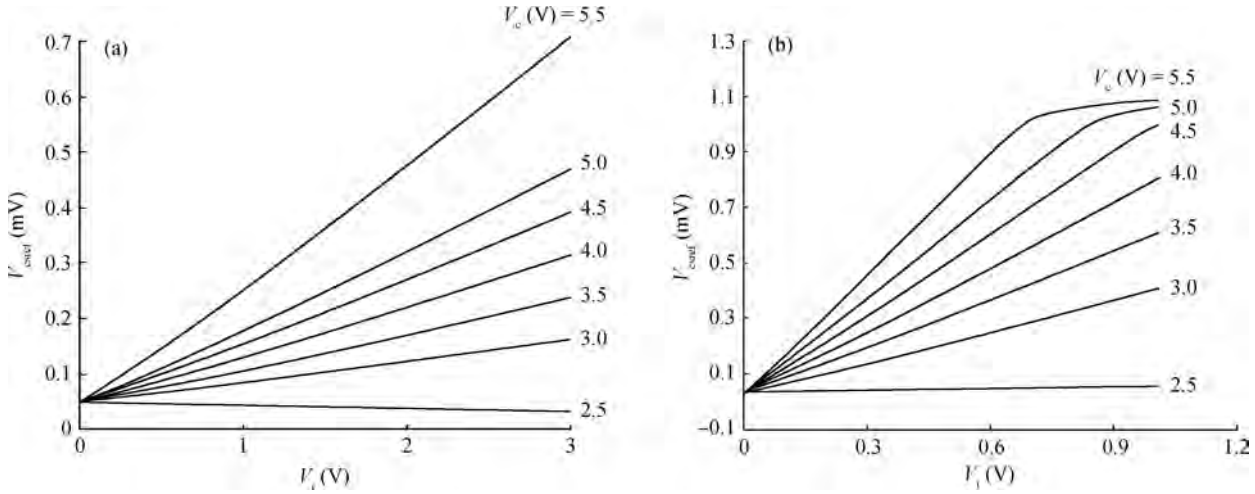

Fig. 5. DC characteristics of the analog multiplier. (a) $V_1 = 3$ V. (b) $V_1 = 1$ V.

Substitute Eq. (15) into Eq. (17), and the reference voltage for the inductor current is

$$V_{\text{csref}} = -\frac{R_4 I_0 V_{\text{T}} V_{\text{c}} V_{\text{i}}}{I_{\text{s}} R_1 (V_{\text{DD}} - V_1)^2 + I_{\text{s}} R_1 V_{\text{T}}^2 + 4V_{\text{T}}^3}. \quad (18)$$

As shown in Eq. (18), the Gilbert cell with the $1/V_1^2$ feedforward compensation cell realizes the multiplication among the feedback control voltage V_{c} generated by the error amplifier, the sampling line voltage V_{i}, and $1/V_1^2$. V_1 is sampled from the ac input line voltage, and has a different amplitude with V_{i}. It compensates the conversion energy needed at VS.

4. Results and discussion

Based on the CSMC 0.5 μm BCD process, a CRM boost PFC converter with a $1/V_1^2$ feedforward compensation cell is simulated and verified. Figure 5 shows the DC characteristic curves of the analog multiplier at bias current $I_0 = 0.66$ μA with the difference feedforward voltage V_1. As shown in Fig. 5(a), when $V_1 = 3$ V the sampling input line voltage V_{i} changes in the range of 0–3 V, and the feedback control voltage V_{c} varies from 2.5 to 5.5 V. Accordingly, the multiplier output signal V_{csref} has a good linearity in the range 0.05–0.7 V. Figure 5(b) shows the dc characteristic at $V_1 = 1$ V. When V_{i} changes in the range 0–1 V, V_{csref} has a swing range of 0.06–1 V. Visibly, with the decrease in V_1, the output swing of the analog

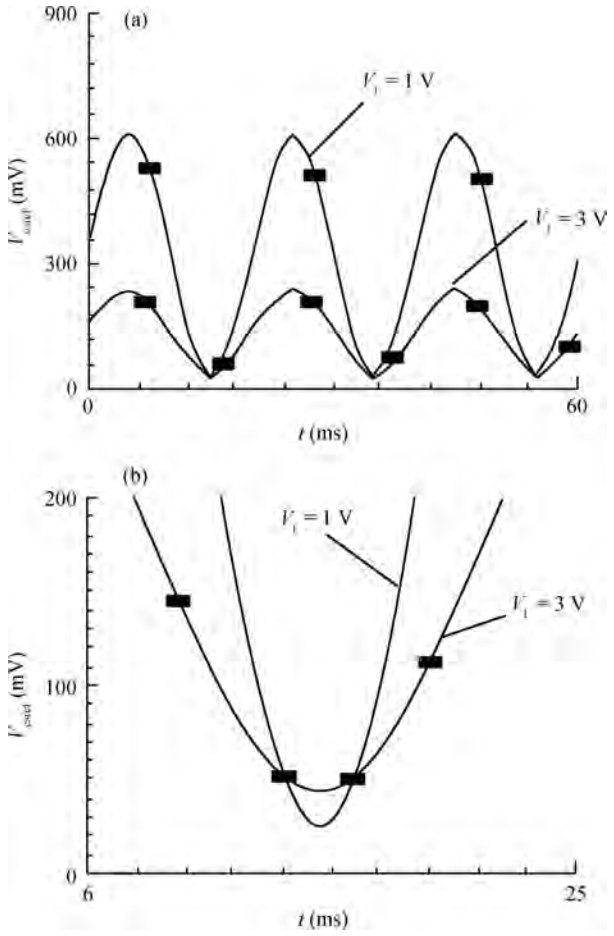

Fig. 6. Temporal characteristic of the analog multiplier: (a) full waveforms and (b) at VS.

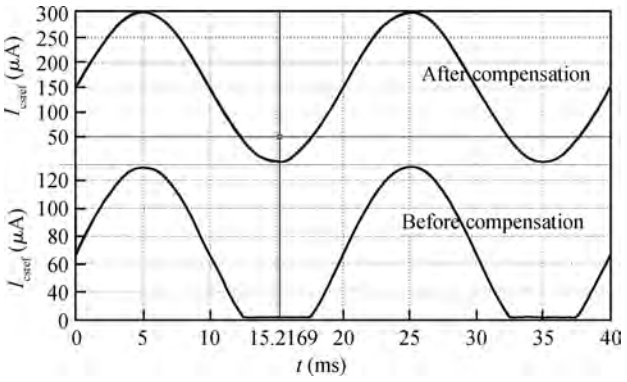

Fig. 7. Output current of the analog multiplier.

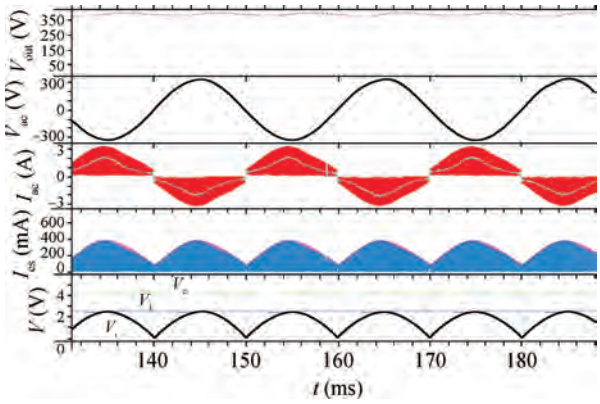

Fig. 8. The simulation waveforms of the CRM boost PFC converter.

multiplier is enhanced. As it is known that V_{csref} is used to compare with the sampling input current to determine the switch duty cycle d, so V_{csref} with a wider swing will extend d. While a larger d could compensate the attenuation of d caused by the parasitic capacitances resonating with the inductor, as described in Section 2. Therefore, more conversion energy is provided at VS, that is, the feedforward compensation cell introduces $1/V_l^2$ to compensate the system loop gain and conversion energy, thereby suppressing the harmonic distortion and improving the system performance. The simulated max slope of V_{csref} following V_i is 2.26. It is worth noting that the lower V_c is, the better the linearity is. This is because with the increase in V_c, transistors Q7–Q10 gradually enter the linear work region, and the output current of the analog multiplier reaches the maximum value, so the output reference voltage swing is limited.

The temporal simulated results further validate the compensation function of V_l, as shown in Fig. 6. It can be seen that from Fig. 6(a), the amplitude of the output reference voltage V_{csref} is 250 mV at the feedforward voltage $V_l = 3$ V, and the amplitude of V_{csref} rises to 600 mV at $V_l = 1$ V. As shown in Fig. 6(b), at VS the minimum value of V_{csref} is 25 mV, and compared with the value at $V_l = 3$ V, V_{csref} drops about 15 mV. So a lower V_l enlarges the output swing of V_{csref} significantly.

The output current I_{csref} of the analog multiplier is given in Fig. 7. Obviously, before compensation the output swing of I_{csref} was only 0–120 μA, and furthermore I_{csref} has distortion at the valleys. After compensation, I_{csref} could obtain an output swing of 0–300 μA, eliminate the distortion phenomenon and supply more conversion energy near the input voltage zero-crossing points.

Figure 8 shows the waveforms of the input current I_{ac} waves following the input voltage V_{ac} at 50 Hz 220 V_{AC}, as well as other control signals in the PFC converter. The output voltage of PFC V_{out} is 392.8 V. The input signals of the analog multiplier, V_l, V_c and V_i, compel the sampling current I_{cs} to present a sinusoidal wave in the same frequency and phase with the rectified input voltage. At the junction of each half ac line cycle, the input current kept a continuous value greater than zero and the current distortions were limited efficiently. This is attributed to the fact that the $1/V_l^2$ feedforward compensation cell adjusts the reference voltage in time and provides more conversion energy at VS, thereby increasing PF and decreasing THD.

At 50 Hz 220 V_{AC} the output power is 36 W. The measured waveforms of the CRM boost PFC converter are shown in Fig. 9. Considering the maximum input current, relevant thermal parameters, fast recovery problem, and so on, STP8NM50 (5 A/500 V) is chosen as the power switch, C_{IN} as 0.22 μF/400 V and C_o as 56 μF/400 V. Before compensation, the rectified line current can automatically follow the sinusoidal line voltage, but all the sampling voltages V_{cs} and inductor currents I_L have obvious distortions at the input voltage zero-crossing points. After feedforward compensation, the system

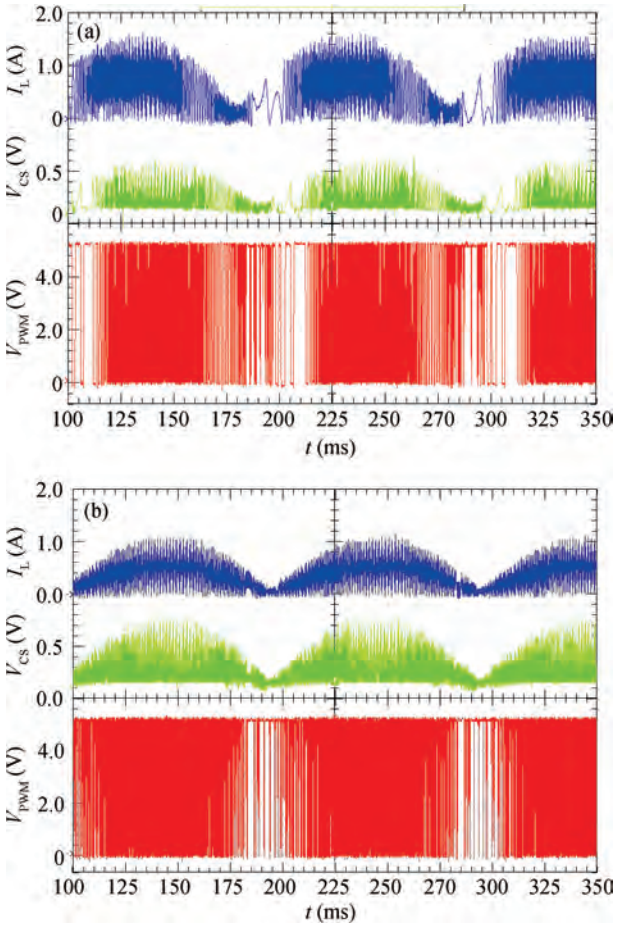

Fig. 9. The measured waveforms of the CRM boost PFC converter: (a) before and (b) after compensation.

Table 1. Comparison of the different boost PFC converters.

Parameter	Efficiency	PF	THD (%)	P_o (W)
Ref. [2]	—	0.9949	10.1	130
Ref. [3]	0.945	0.995	3.8	50
Ref. [5]	—	0.98	5.22	—
Ref. [6]	0.973	0.988	3.8	—
Ref. [9]	0.947	0.996	5	50
Ref. [10]	—	0.9797	14.9	—
This work	0.952	0.998	4.5	36

could eliminate distortions and switching-frequency limitations with a lower input current THD. At full load and $V_{cc} = 12$ V, $V_{fb} = 2$ V and $V_i = 2$ V, the measured THD of the boost PFC converter is 4.5% from the digital power meter WT230, the power factor is 0.998, the start-up current is 54 μA, the stable operating current is 3.85 mA from the multimeter VICTOR VC9806, and the efficiency is 95.2% from the ac power source EXTECH6805 and the active load ITECH IT8511. A conclusion can be achieved that the PFC converter presented in this paper meets the requirements of low-power low THD design.

Table 1 shows the parameter characteristics of several boost PFC converters. The difference working mode, the output power P_o, the process, and the variable loads will all affect the performance of the converters. Comparatively, the CRM boost PFC converter in this work has a better compromise among THD, PF, efficiency and P_o, and all these parameter indicators meet the demands for low-power, low THD and high PF.

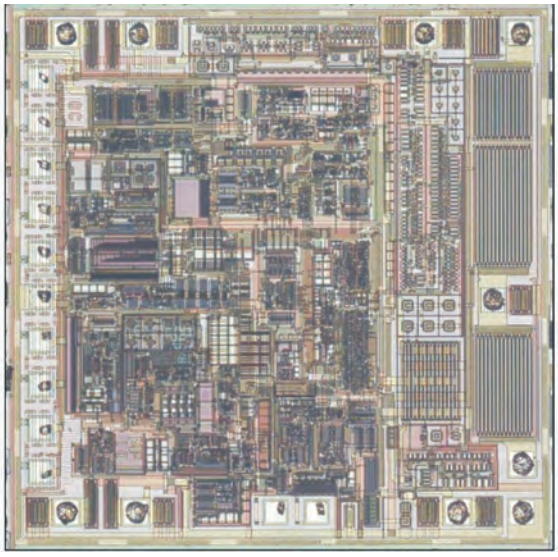

Fig. 10. Layout of the CRM boost PFC converter.

Based on the CSMC 0.5 μm BCD process, the layout of the CRM boost PFC converter is realized. To prevent crosstalk noise in the voltage feedback loop and current sampling loop, protection ring and dummy devices have been added around the critical paths as isolation. To reduce static imbalance and dynamic offset voltage, cross-empty lead technology has been used in the differential cells, such as the error amplifier. The output stage layout applies symmetry design to reduce the dynamic error. The active die area is 1.62×1.70 mm^2, as shown in Fig. 10.

5. Conclusions

A novel $1/V_l^2$ feedforward compensation cell for reducing the power and THD of the CRM boost PFC converter was presented. The feedforward control voltage V_l could enlarge the PWM duty cycle and compensate the conversion energy needed by the system at VS, thereby eliminating the current distortion effectively. Based on the CSMC 0.5 μm BCD process, the CRM boost PFC converter was analyzed and verified. Both simulation and testing results revealed that the system significantly reduced the harmonic current and restrained the nonlinearity phenomenon and the frequency limits of the system. The proposed PFC converter with feedforward compensation cell is suitable for low-power low THD design applications.

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