On-chip frequency compensation with a dual signal path operational transconductance amplifier for a voltage mode control DC/DC converter*

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Abstract: A novel on-chip frequency compensation circuit for a voltage-mode control DC/DC converter is presented. By employing an RC network in the two signal paths of an operational transconductance amplifier (OTA), the proposed circuit generates two zeros to realize high closed-loop stability. Meanwhile, full on-chip integration is also achieved due to its simple structure. Hence, the number of off-chip components and the board space is greatly reduced. The structure of the dual signal path OTA is also optimized to help get a better transition response. Implemented in a 0.5 μm CMOS process, the voltage mode control DC/DC converter with the proposed frequency compensation circuit exhibits good stability. The test results show that both load and line regulations are less than 0.3%, and the output voltage can be recovered within 15 μs for a 400 mA load step. Moreover, the compensation components area is less than 2% of the die's area and the board space is also reduced by 11%. The efficiency of the whole chip can be up to 95%.

Key words: DC/DC convertor; voltage mode control; on-chip frequency compensation; stability
DOI: 10.1088/1674-4926/33/4/045006 **EEACC:** 2560P; 2570A

1. Introduction

In recent years, battery-powered portable devices such as cellular phones, personal digital assistants and other palm-sized devices have been in great demand[1−3]. Due to high power conversion efficiency, DC/DC converters are widely used in these devices to reduce the standby power and maximize the battery run-time[4]. Compared to current-mode control schemes, voltage-mode control schemes have the advantage of a less complicated control circuit, lower noise sensitivity and potentially higher power efficiency for the absence of accurate and fast current sensing and processing. Hence, they are a popular choice in DC/DC converters. In voltage-mode control DC/DC converters, the stability requirement is becoming more stringent as the supply range extends and the board space decreases.

In most cases, conventional approaches could compensate the voltage-mode control DC/DC converter. By introducing an extra zero generated by the equivalent series resistance (ESR) of the output capacitor, the converters with a type II compensation can obtain a sufficient phase margin. The problem with the type II compensation method is that the ESR of a capacitor varies with temperature and is not properly specified in many cases[5]. Moreover, if a large ESR value is adopted to generate the low-frequency zero, it results in large board space and output voltage ripple. The type III compensation which eliminates the need for ESR zero to solve the problem of system stability is hence the choice in many systems. However, a complex compensation circuit and more off-chip components are difficult to avoid.

A novel on-chip frequency compensation circuit based on a dual signal path operational transconductance amplifier (OTA) is therefore proposed in this paper. This method can maintain system stability independent of the ESR of the output capacitor. Meanwhile, fewer components and a simplified and fully integrated compensation circuit could also be achieved. Details of the transistor level circuit are provided and the enhanced slew rate of the OTA also improves the dynamic response of the converter.

2. A review of the voltage-mode control scheme

The structure of the PWM buck converter with voltage-mode control is shown in Fig. 1. The system can be divided into three parts: the feedback network, the compensation and the modulator[6, 7]. The feedback network consists of two resistors that are used to set different output voltages. The compensation is composed of an error amplifier and compensation components. The compensation circuit is used to provide enough phase margin so as to realize system stability. The modulator consists of a PWM comparator, a control and driver block, and an output filter.

The major characteristic of the voltage-mode control scheme is that there is a single voltage feedback path with pulse-width modulation performed by comparing the voltage error signal with a constant ramp waveform. As mentioned above, this feedback control scheme has many advantages to its current-mode control counterparts, especially in a high-frequency DC/DC converter. However, it also brings three ma-

* Project supported by the National Natural Science Foundation of China (No. 60876023) and the Fundamental Research Funds for the Central Universities, China (No. K50511020031).
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Received 28 July 2011, revised manuscript received 26 November 2011

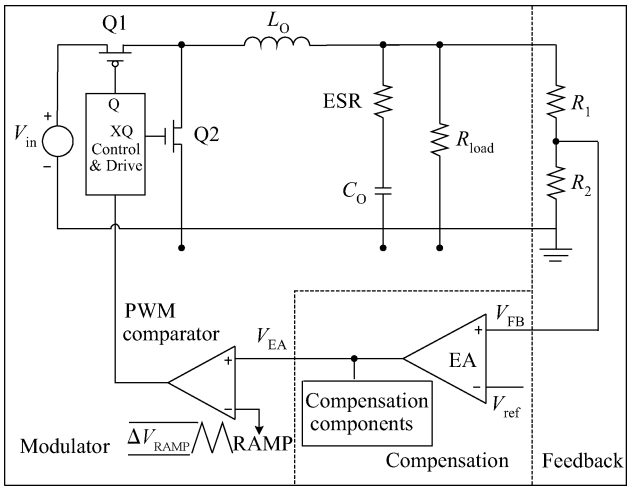

Fig. 1. Structure of the voltage-mode control buck DC/DC convertor.

jor difficulties[8]. First, compensation in voltage-mode control schemes is more complicated by the fact that the loop gain varies with input voltage. Second, the output filter adds two poles to the control loop, requiring an added zero in the compensation. Moreover, any change in line or load must first be sensed as an output change and then corrected by the feedback loop. This usually means slow responses.

For the first drawback, the input-voltage feed-forward is an effective method, which makes the converter gain independent of the input voltage. To counteract the effect of the output filter, type II or type III compensation is usually employed in the voltage-mode control DC/DC converter. However, for the consideration of limited board space, ceramic capacitors with small ESR are widely used. As a result, the ESR zero in the loop gain is pushed to a higher frequency, so that type II compensation may not be enough to maintain adequate stability in the control loop. The type III compensation generates an added low-frequency zero instead of the ESR zero. Nonetheless, the off-chip compensation components of type III compensation often prove to be an obstacle for further squeezing the size of the power regulator. Thus a novel fully integrated compensation methodology that can generate the necessary zeros yet occupy a smaller area is proposed in this paper. Moreover, the slew rate is also improved to optimize the transition response.

3. The proposed frequency compensation circuit

3.1. Stability analysis

The simplified loop model of the voltage-mode control DC/DC converter adopting the proposed frequency compensation circuit is shown in Fig. 2. The loop can be divided into three stages.

(1) Modulator. As shown in Fig. 2, the input of the modulator is the output of compensation V_{EA}. The transfer function of the modulator is composed of two parts and the G_{MOD} is the gain from V_{EA} to the SW node, which is equal to:

$$G_{MOD} = \frac{V_{IN}}{\Delta V_{RAMP}}, \tag{1}$$

where V_{IN} is the supply voltage and ΔV_{RAMP} is the peak-to-peak ramp voltage. Then the transfer function of the modulator can be expressed as:

$$H_1(s) = G_{MOD}\frac{1 + s\cdot \mathrm{ESR}\cdot C_O}{1 + s\cdot \mathrm{ESR}\cdot C_O + s^2 L_O C_O} = \frac{V_{IN}}{\Delta V_{RAMP}}\frac{1 + s\cdot \mathrm{ESR}\cdot C_O}{1 + s\cdot \mathrm{ESR}\cdot C_O + s^2 L_O C_O}. \tag{2}$$

Equation (2) shows the double pole generated by the output filter, which greatly degrades the system stability[8, 9].

(2) Feedback. The feedback network is composed simply of resistors, which are used to set different output voltages. Since there are no capacitors in the feedback network, this stage has no effect on the phase margin. Its transfer function is equal to:

$$H_2(s) = \frac{R_2}{R_1 + R_2}. \tag{3}$$

(3) Compensation. As shown in Fig. 2, the proposed frequency compensation circuit is composed of an OTA and the compensation components R_3, R_4, C_1 and C_2. Since the OTA has two signal paths, the superposition method is used here. Figure 3 shows the equivalent small signal circuit of the proposed frequency compensation. G_{m1} and G_{m2} represent the transconductance of the first and second signal paths of the error amplifier, respectively. R_{out} is the resistance at the output of the first signal path.

To analyze the first signal path, the second signal path is disconnected. The equivalent small signal circuit is shown in Fig. 3(a). The transfer function of the first signal path is equal to:

$$\begin{aligned} H_{3\_1}(s) &= G_{m1}(Z_1||Z_2)\frac{R_4 + 1/sC_2}{Z_2} \\ &= G_{m1}R_{out}(1 + sR_4C_2) \\ &\quad \times \left\{s^2 R_{out}(R_3 + R_4)C_1C_2 + s[R_{out}(C_1 + C_2) \right. \\ &\quad \left. + R_3C_2 + R_4C_2] + 1\right\}^{-1}. \end{aligned} \tag{4}$$

For $C_1 \gg C_2$,

$$H_{3\_1}(s) \approx G_{m1}R_{out}\times \frac{1 + sR_4C_2}{s^2 R_{out}(R_3 + R_4)C_1C_2 + s\left[R_{out}C_1 + (R_3 + R_4)C_2\right] + 1}. \tag{5}$$

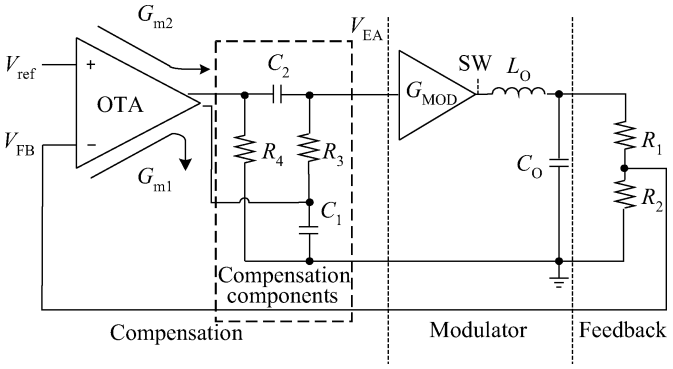

Fig. 2. The simplified loop model with proposed frequency compensation.

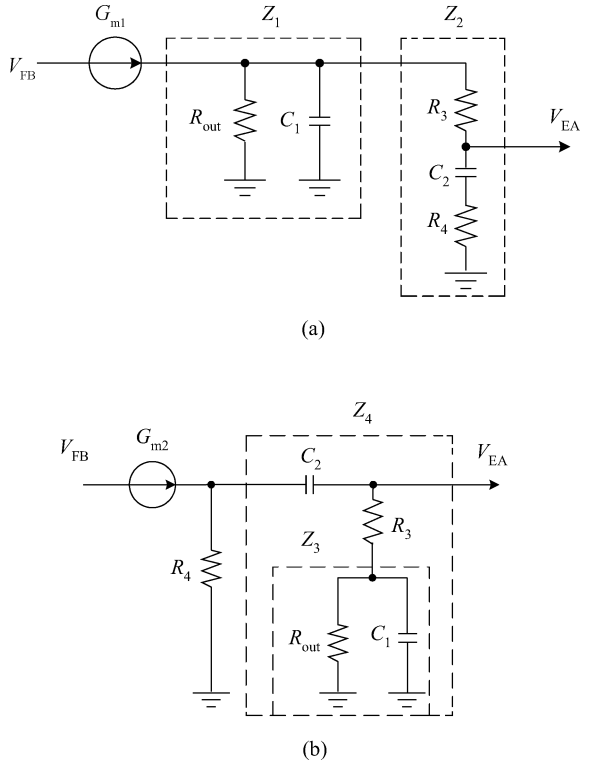

Fig. 3. Equivalent circuits of (a) the first signal path and (b) the second signal path.

For the analysis of the second signal path, the first signal path is disconnected. The equivalent small signal circuit is shown in Fig. 3(b). The transfer function of the second signal path is equal to:

$$\begin{aligned} H_{3\_2}(s) &= G_{m2}(R_4||Z_4)\frac{R_3+Z_3}{Z_4} \\ &= G_{m2}R_4C_2\times s\,(sR_3R_{out}C_1+R_{out}+R_3) \\ &\quad\times[s^2R_{out}(R_3+R_4)C_1C_2+s(R_{out}C_1+R_{out}C_2 \\ &\quad+R_3C_2+R_4C_2)+1]^{-1}. \end{aligned} \tag{6}$$

For $C_1 \gg C_2$,

$$H_{3\_2}(s) \approx G_{m2}R_4C_2\times \frac{s\,(sR_3R_{out}C_1+R_{out}+R_3)}{s^2R_{out}(R_3+R_4)C_1C_2+s\,[R_{out}C_1+(R_3+R_4)\,C_2]+1}. \tag{7}$$

From Eqs. (5) and (7), we get the transfer function of this stage as follows:

$$\begin{aligned} H_3(s) &= H_{3\_1}(s)+H_{3\_2}(s) \\ &= \{s^2G_{m2}R_{out}R_3R_4C_1C_2+sR_4C_2\,[R_{out}(G_{m1}+G_{m2}) \\ &\quad+R_3G_{m2}]+G_{m1}R_{out}\}\{s^2R_{out}(R_3+R_4)C_1C_2 \\ &\quad+s\,[R_{out}C_1+(R_3+R_4)\,C_2]+1\}^{-1}. \end{aligned} \tag{8}$$

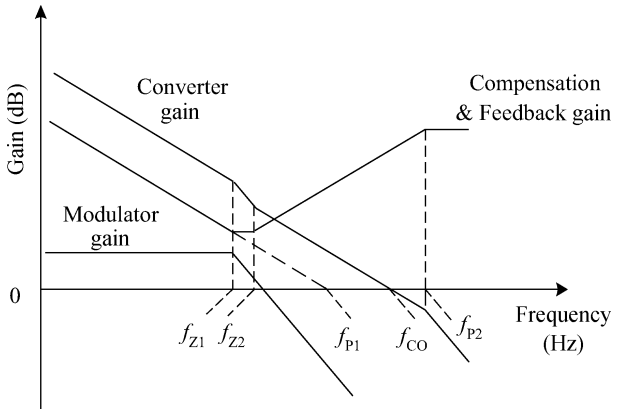

Fig. 4. A Bode gain plot of the convertor.

From Eq. (8), we can see that the proposed compensation circuit utilizes two zeros and two poles, which are expressed as:

$$Z_1 = \frac{R_{out}(G_{m1}+G_{m2})+R_3G_{m2}}{G_{m2}R_{out}R_3C_1},$$

$$Z_2 = \frac{G_{m1}R_{out}}{R_4C_2\,[R_{out}(G_{m1}+G_{m2})+R_3G_{m2}]}, \tag{9}$$

$$P_1 = \frac{1}{2\pi R_{out}C_1}, \quad P_2 = \frac{1}{2\pi(R_3+R_4)C_2}. \tag{10}$$

These two zeros, which give a phase boost of 180°, are necessary to provide enough phase margin and counteract the effects of the output filter at the double pole.

Figure 4 shows the DC/DC converter's Bode gain plot in detail. The gain curve of the converter is the sum of the curve of three stages. For the location of the two zeros determined by the integrated components, adjusting the parameters could guarantee that the converter gain rolls off at a slope of –20 dB/dec at a desired crossover frequency f_{CO}. According to the sampling theorem, in order to ensure stability, the f_{CO} must be less than half the switching frequency. In fact, to avoid the interference of the switching ripple on the output, the f_{CO} is usually placed at the 1/10 switching frequency[4]. Meanwhile, in order to reduce the output voltage ripple, a 4.7–22 μF ceramic capacitor is generally used as the output capacitor.

3.2. Circuit design

The transistor-level circuit of the proposed frequency compensation is shown in Fig. 5. The M1–M13, R_1 and R_2 comprise the OTA. The C_1, C_2, R_3 and R_4 correspond to the compensation components in Fig. 2. The first stage of the OTA consists of M3–M6, R_1 and R_2. The next stage of the OTA has two small signal paths. The first one is composed of M7–M10 and the second one is composed of M11–M13. The G_{m1}, G_{m2} and R_{out} could be expressed as:

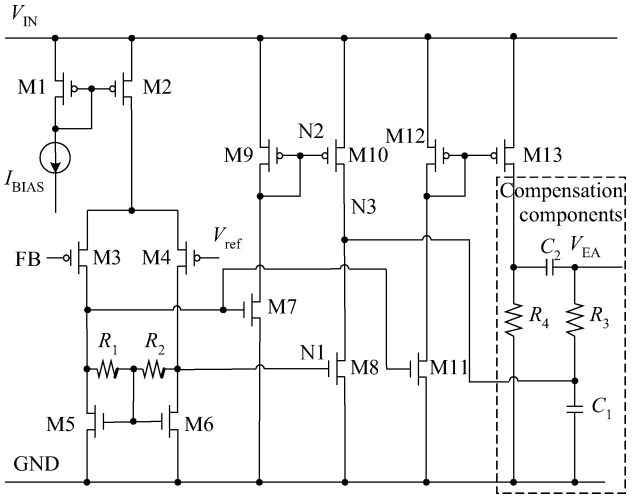

Fig. 5. A transistor-level circuit of the proposed frequency compensation.

$$G_{m1} = g_{m3}g_{m7}(r_{o5}||R_1)\frac{(W/L)_{M10}}{(W/L)_{M9}},$$

$$G_{m2} = \frac{1}{2}g_{m3}g_{m11}(r_{o5}||R_1)\frac{(W/L)_{M13}}{(W/L)_{M12}}, \quad R_{out} = r_{o8}, \quad (11)$$

in which r_{o5} and r_{o8} represent the conductive impedance of M5 and M8, respectively. They are equal to:

$$r_{o5} = \frac{2}{\lambda I_{BIAS}}, r_{o8} = \frac{2(W/L)_{M9}}{\lambda K(V_{GS7} - V_{TH7})^2(W/L)_{M7}(W/L)_{M10}}. \quad (12)$$

The transconductance g_{m3}, g_{m7}, g_{m11} can be expressed as:

$$g_{m3} = \sqrt{K(W/L)_{M3}I_{BIAS}},$$

$$g_{m7} = K(W/L)_{M7}(V_{GS7} - V_{TH7}),$$

$$g_{m11} = K(W/L)_{M11}(V_{GS7} - V_{TH11}), \quad (13)$$

where λ is the channel-length modulation coefficient and K is the transconductance coefficient. From Eqs. (9) and (10), the reduction of C_2, R_3 and R_4 could place P_2 to high frequency, but also move two zeros to high frequency. Otherwise, increasing G_{m2} and C_1 could move the zeros to the low frequency and have little effect on P_2. Equations (11)–(13) could directly guide the selection of parameters.

Additionally, the slew rate of the OTA is also optimized. Since the transient performance of the DC/DC converter is determined by the slew rate of the OTA and closed-loop bandwidth, the higher slew rate leads to better transient response. In this structure, the differential to single conversion is designed in the second stage rather than the first stage. The voltages at N1 and N2 can thus be varied during the transient condition. This enables M8 and M10 to pull and push the slew rate current simultaneously of node N3, and consequently the slew rate is enhanced.

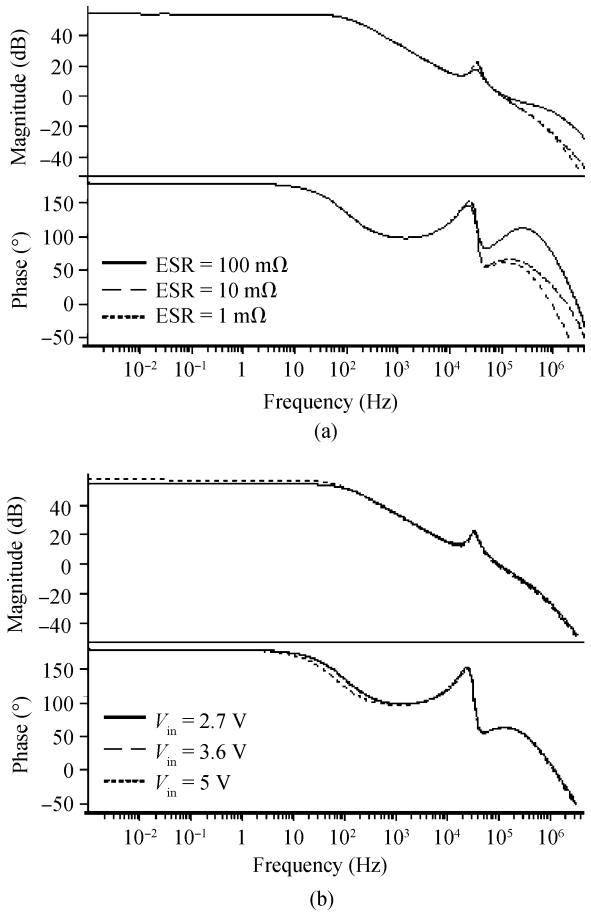

Fig. 6. (a) An open-loop AC response with different ESR values and (b) an open-loop AC response with different V_{IN} values.

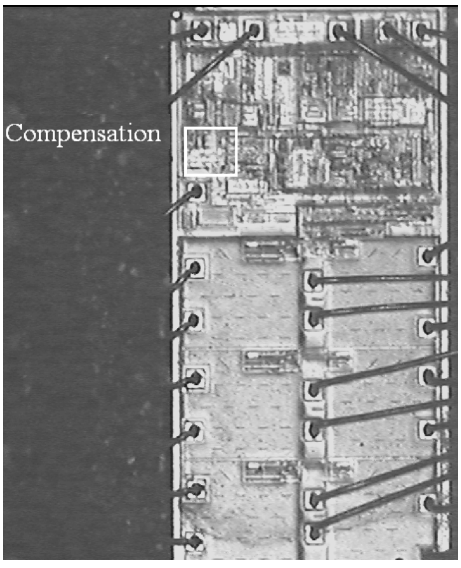

Fig. 7. A micrograph of the DC/DC converter.

4. Simulation and experimental results

4.1. Simulation results

Figure 6(a) shows the simulation results of open-loop AC response with different ESR values. When ESR = 1 mΩ, the phase margin is 61.6° and it increases with the ESR value. Fig-

Table 1. A comparison with the previously reported DC/DC converters.

Parameter	Ref. [4]	Ref. [10]	This work
Technology	CMOS 0.5 μm	CMOS 0.5 μm	CMOS 0.5 μm
Feedback control scheme	Current mode control	Voltage mode control	Voltage mode control
Supply voltage (V)	2.5–5.5	2.5–5.5	2.7–5.5
Maximum output current (mA)	600	750	600
Frequency (MHz)	1.5	1	1
Line regulation (%/V)	< 0.4	0.17	< 0.3
Load regulation (%/A)	< 0.4	1	< 0.3
Load step recovering time (μs/100mA)	< 2	< 3.5	< 2.5

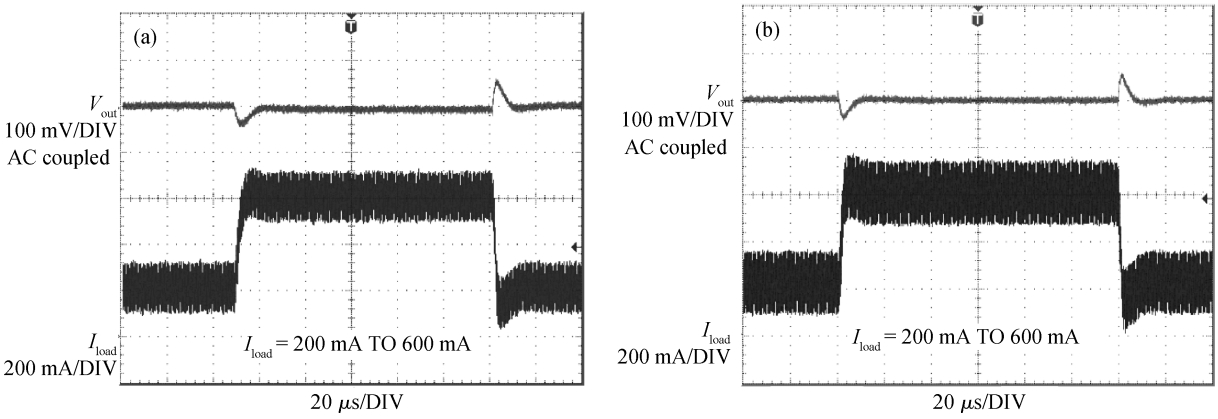

Fig. 8. (a) $V_{IN} = 3.6$ V, $V_{OUT} = 1.8$ V. (b) $V_{IN} = 5$ V, $V_{OUT} = 1.8$ V.

ure 6(b) shows the simulation results for V_{IN} voltage at 2.7, 3.6 and 5.5 V. The converter with the proposed frequency compensation achieves over 60° phase margin for all cases, and the crossover frequency is about 120 kHz, which is around 1/10 of the switching frequency.

4.2. Experimental results

Based on a 0.5 μm CMOS process, the DC/DC converter with the proposed frequency compensation circuit is designed and implemented. Figure 7 shows a die micrograph of the voltage-mode control DC/DC converter. The die area is 1818.9 $\times$ 1230 μm^2 and the compensation components area is less than 2% of this. It is packaged in a 3 $\times$ 3 TDFN-10 package and the electrical characteristics of the converter are shown in Table 1.

The chip is tested with an X7R ceramic output capacitor. The results indicate that the output is stable with no oscillation under any duty cycles and load conditions. The load regulation and line regulation are both less than 0.3% at room temperature. Figure 8 shows the results of the load transient response under conditions $V_{IN} = 3.6$ V, $V_{OUT} = 1.8$ V and $V_{IN} = 5$ V, $V_{OUT} = 1.8$ V, respectively. The load current jumped from 200 to 600 mA and the output voltage could recover within 15 μs.

The resistance of the power MOS is less than 200 mΩ, and by the internal synchronous rectification the efficiency is up to 95%. Compared with the traditional frequency compensation, the proposed frequency compensation could not only maintain the system stability without the help of ESR zero, but also save the board space efficiently by reducing two off-chip components.

5. Conclusion

An on-chip frequency compensation circuit with dual signal path OTA for a voltage-mode control DC/DC converter was introduced in this paper. Compared with the conventional method, the proposed on-chip frequency compensation circuit can generate two zeros, which are enough to counteract the effects of the output filter at the double pole and make the system have a high stability without the need for ESR zero. Moreover, the board space is reduced by 11% due to the simple structure of the proposed circuit, and the structure of OTA is optimized to help get a better transition response. A voltage-mode control Buck DC/DC convertor employing this compensation circuit was implemented in a 0.5 μm CMOS process, and the experimental results verified the proposed compensation circuit.

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