Experimental study of the anode injection efficiency reduction of 3.3-kV-class NPT-IGBTs due to backside processes*

Jiang Huaping(蒋华平)^{1,†}, Zhang Bo(张波)¹, Liu Chuang(刘闯)², Chen Wanjun(陈万军)¹, Rao Zugang(饶祖刚)², and Dong Bin(董彬)²

¹State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronics Science and Technology of China, Chengdu 610054, China

²Tianjin Zhonghuan Semiconductor Co. Ltd., Tianjin 300384, China

Abstract: The anode injection efficiency reduction of 3.3-kV-class non-punch-through insulated-gate bipolar transistors (NPT-IGBTs) due to backside processes is experimentally studied through comparing the forward blocking capabilities of the experiments and the theoretical breakdown model in this paper. Wafer lifetimes are measured by a μ -PCD method, and well designed NPT-IGBTs with a final wafer thickness of 500 μ m are fabricated. The test results show higher breakdown voltages than the theoretical breakdown model in which anode injection efficiency reduction is not considered. This indicates that anode injection efficiency reduction must be considered in the breakdown model. Furthermore, the parameters related to anode injection efficiency reduction are estimated according to the experimental data.

Key words: non-punch-through IGBT; anode injection efficiency reduction; breakdown voltage **DOI:** 10.1088/1674-4926/33/2/024003 **EEACC:** 2570

1. Introduction

Insulated-gate bipolar transistors (IGBTs) have become the major power switching device in power electronic applications as they combine both the advantages of field-effect transistors and those of bipolar junction transistors^[1]. The rapid development of high-voltage IGBTs within the $3.3^{[2]}$ to 6.5 kV^[3, 4] range in recent years has improved the system efficiency and led to much simpler drive circuits. Today high-voltage IGBT models have been the basic electronic components of power-conversion systems in railway applications^[5, 6].

The breakdown model of non-punch-through IGBTs (NPT-IGBTs), which consists of a wide-open-base p–n–p transistor driven by an integrated MOSFET, is based on the open-base p–n–p transistor^[7–9]. The breakdown voltage of the IGBT and the common-base current gain are related by a widely used empirical formula^[10]

$$V_{\rm B} = V_{\rm B0} (1 - \alpha)^{1/n}, \tag{1}$$

where $V_{\rm B0}$ and α are the breakdown voltage of J1 (shown in Fig. 1) and the common-base current gain respectively, n = 6 for n-type IGBTs. We can conclude from Eq. (1) that a decrease of the common-base current gain results in an increase of the breakdown voltage. In this paper, the forward blocking capabilities of 3.3-kV-class NPT-IGBTs are studied in detail considering the anode injection efficiency reduction. The anode injection efficiency reduction to backside processes is estimated according to experimental results.

2. Theoretical analysis

Considering that the anode injection efficiency of the NPT-IGBT in the forward blocking mode is decreased by the recombination current in the depletion region of J2, one has^[11]

$$\alpha = \frac{\sec h(x_{\rm n}/\sqrt{D_{\rm p}\tau_{\rm p}})}{1+\eta+\delta},\tag{2}$$

where $\eta = J_{dn}/J_{dp}$, $\delta = J_r/J_{dp}$, D_p and τ_p are the diffusion coefficient for holes and the minority carrier lifetime of the base respectively, ρ and R_{sq} are the resistivity of the N-drift region



Fig. 1. Schematic cross-sectional view and electric field distribution of the NPT-IGBT during forward blocking mode.

* Project supported by the Major Specialized Program of National Science and Technology, China (No. 2011ZX02706-003).

[†] Corresponding author. Email: huapingjiang2008@gmail.com

Received 29 July 2011, revised manuscript received 27 September 2011



Fig. 2. Graphic illustration of the relation of the breakdown voltage $(V_{\rm B})$ and common-base current gain (α) . Three kinds of situations, i.e., the punch-through breakdown voltage $(V_{\rm PT})$ is equal to, larger and smaller than the avalanche breakdown voltage of J1 $(V_{\rm B0})$, are shown in (a). $V_{\rm PT}$ is supposed to be smaller than $V_{\rm B0}$ for simplicity in (b).

and the sheet resistivity of the P-collector respectively; and x_n is the width of the neutral base satisfying $W = x_1 + W_D + x_n + x_d + x_2$ with the symbols wherein being illustrated in Fig. 1. The width of the depletion region of J1 (W_D) is a function of V_B and satisfies $qN_DW_D^2/(2\varepsilon_s) = V_B$, where N_D is the doping concentration of the N-drift.

It is worth noting that the backside junction (J2) is a onesided abrupt junction. The majority of the depletion region is inside the lightly doped N-drift side. When J2 is slightly forward biased during the forward blocking mode, the width of the depletion region is in the 3–6 μ m range.

As shown in Refs. [12, 13], the lifetimes near the backside collector are locally reduced by the backside processes, and therefore the anode injection efficiency can be reduced. The direct consequence of the anode injection efficiency reduction is the increase in the breakdown voltage.

It is worth noticing that both α_T and γ vary with the width of the neutral N-drift region, x_n , which is a function of V_B . So V_B is implicitly determined by Eqs. (1) and (2), both of which are graphically illustrated by clusters of curves in Fig. 2. The breakdown points are represented by the cross points of the two clusters of curves. The three curves in Fig. 2(a) denoted by A, B, and C correspond to the three different relations of avalanche breakdown voltage (V_{B0}) and punch-through breakdown voltage (V_{PT}). As illustrated in Fig. 2(b), x_n approaches 0 and α approaches $1/(1+\delta)$ which is usually smaller than unity



Fig. 3. Lifetime distribution of the 6-inch 700- μ m-thick wafer.

while V_{CE} approaches the punch-through breakdown voltage (V_{PT}) . And one can conclude that the increase of δ leads to the increase of the breakdown voltage.

3. Experiments and discussions

IGBT chips with a final wafer thickness of 500 μ m are designed and fabricated. The resistivity of the (100)oriented starting material doped by neutron transmutation is 195–199 Ω ·cm. The lifetimes, shown in Fig. 3, are tested by the μ -PCD method. The tested values are between 28.8 and 1373 μ s, and the average and median are 324.08 and 181.15 μ s respectively.

The laser mark is followed by edge termination implantation with a dosage of $3-3.8 \times 10^{12}$ cm⁻². After active etching, a low dosage of phosphorus implantation of the order of 1×10^{12} cm⁻² was selectively carried out by the splitting plan before 100 nm gate oxides were grown. A high dosage of boron implantation followed the Ohm contact etching, for better Ohm contact of the P-base and aluminum. Front side processing is completed with cathode metallization and passivation. After the topside processes, wafers were ground to a thickness of 500 μ m. P⁺-collectors with a sheet resistivity of 4.7 k Ω are then formed by Boron implantation followed by 30-min low temperature annealing^[14].

The breakdown voltages of the fabricated IGBTs with P⁺collector sheet resistivity of 4.7 k Ω are in the 3.7 to 3.8 kV range with typical breakdown curves shown in Fig. 4. The blocking capabilities of the analytical model and the simulations are shown in Fig. 5. The P+-collector sheet resistivity of the IGBTs used in the analytical calculation and the simulations is set to be 4.7 k Ω . The anode injection efficiency reduction due to the recombination current of the depletion region of the backside junction (J2) at low current density is not considered (i.e. $\delta = 0$). The results of the analytical model show good agreement with those of the simulations, according to which the experimental breakdown voltages should be in the 3.5 to 3.65 kV range. However, as is shown, the test breakdown voltages are much higher. This, combined with the relation of the breakdown voltages and the parameter δ (shown in Fig. 6), indicates that anode injection efficiency reduction must be considered in the breakdown model. It is worth pointing out that the small deviation of experimental breakdown voltages is the result of anode injection efficiency reduction.

The values of δ are estimated in detail by analytical for-



Fig. 4. Typical breakdown curves of (a) 3.7 kV and (b) 3.8 kV NTT-IGBTs with a P⁺-collector sheet resistivity of 4.7 k Ω .



Fig. 5. Comparison of the blocking capabilities of experiments, analytical model, and simulations. The P⁺-collector sheet resistivity of the IGBTs used in the simulation and analytical calculation is set to be 4.7 k Ω . The anode injection efficiency reduction is not considered (i.e. $\delta = 0$).

mulas according to the experimental results and are shown in Fig. 7. The curves rise with the increase of lifetime and show plateaus in the 30 to 1000 μ s range. The details of the para-



Fig. 6. Relation of breakdown voltage and parameter δ .



Fig. 7. Dependencies of δ on τ_p with a P⁺-collector sheet resistivity of 4.7 k Ω .

Table 1. Details of the estimation of δ .

Parameter	Value	
N_{D}	$2.2 \times 10^{13} \text{ cm}^{-3}$	
ρ	195 Ω·cm	
W	500 µm	
R_{sq}	4.7 kΩ/□	
$V_{\rm B0}$	5.3 kV	
$V_{\rm B}({\rm Avg.})$	3.76 kV	
x _n	27.2 μm	
$ au_{\mathrm{p}}$	28.8–1373 μs	
$\dot{\alpha}_{\mathrm{T}}$	> 0.976	
δ	0.09-0.1	

meters used in the estimation are shown in Table 1. It is important to notice that the breakdown voltage with P⁺-collector sheet resistivity 4.7 k Ω in Table 1 is the average of more than 40 test values.

4. Conclusions

The anode injection efficiency reduction of 3.3-kV-class NPT-IGBTs which is a result of backside processes is experimentally studied in detail. The wafer lifetimes measured by the μ -PCD method are in the 28.8 to 1373 μ s range. IGBTs

References

class NPT-IGBTs.

- Baliga B J. The future of power semiconductor device technology. Proc IEEE, 2001, 89(6): 822
- [2] Castellazzi A, Ciappa M, Fichtner W, et al. Integrated compact modelling of a planar-gate non-punch-through 3.3 kV-1200 A IGBT module for insightful analysis and realistic interpretation of the failure mechanisms. Proc ISPSD, 2007: 133
- [3] Bauer J G, Schilling O, Schaeffer C, et al. Investigations on the ruggedness limit of 6.5 kV IGBT. Proc ISPSD, 2005: 1
- [4] Bauer J G, Duetemeyer T, Falck E, et al. Investigations in 6.5 kV trench IGBT and adapted EmCon diode. Proc ISPSD, 2007: 5
- [5] Uzuka T. Trends in high-speed railways and the implications on

power electronics and power devices. Proc ISPSD, 2011: 6

- [6] Sato K, Yoshizawa M, Fukushima T. Traction systems using power electronics for Shinkansen high-speed electric multiple units. The International Power Electronics Conference, 2010: 2859
- [7] Khanna V K. Insulated gate bipolar transistor (IGBT): theory and design. John Wiley & Sons, 2003
- [8] Sze S M, Ng K K. Physics of semiconductor devices. 3rd ed. John Wiley & Sons, 2007
- [9] Taur Y, Ning T H. Fundamentals of modern VLSI devices. Cambridge University Press, 1998
- [10] Baliga B J. Fundamentals of power semiconductor devices. Springer, 2008
- [11] Chen X B, Zhang Q Z. Transistor theory and design. Beijing: Publishing House of Electronics Industry, 2006
- [12] Nakamura K, Hisamoto Y, Matsumura T, et al. The second stage of a thin wafer IGBT low loss 1200 V LPT-CSTBTTM with a backside doping optimization process. Proc ISPSD, 2006: 1
- [13] Robinson J T, Cecil O B, Shah R R. Method for removal of minute physical damage to silicon wafers by employing laser annealing. USA Patent, No.4390392, 1983
- [14] Jiang Huaping, Chen Wanjun, Liu Chuang, et al. Design and optimization of linearly graded-doping junction termination extension for 3.3-kV-class IGBTs. Journal of Semiconductors, 2011, 32(12): 124004