Influence of back-gate stress on the back-gate threshold voltage of a LOCOS-isolated SOI MOSFET*

Mei Bo(梅博), Bi Jinshun(毕津顺), Li Duoli(李多力), Liu Sinan(刘思南), and Han Zhengsheng(韩郑生)†

Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

Abstract: The performance of a LOCOS-isolated SOI MOSFET heavily depends on its back-gate characteristic, which can be affected by back-gate stress. A large voltage stress was applied to the back gate of SOI devices for at least 30 s at room temperature, which could effectively modify the back-gate threshold voltage of these devices. This modification is stable and time invariant. In order to improve the back-gate threshold voltage, positive substrate bias was applied to NMOS devices and negative substrate bias was applied to PMOS devices. These results suggest that there is a leakage path between source and drain along the silicon island edge, and the application of large back-gate bias with the source, drain and gate grounded can strongly affect this leakage path. So we draw the conclusion that the back-gate threshold voltage, which is directly related to the leakage current, can be influenced by back-gate stress.

Key words: back-gate; threshold voltage; stress; silicon-on-insulator

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1. Introduction

Silicon-on-insulator (SOI) technology has many advantages over other technologies. Its high temperature reliability, high speed, low power and radiation hardness have rapidly made SOI technology a main-stream commercial technology[1]. But there are still many disadvantages of SOI devices, such as the effect of back-gate (as is shown in Fig. 1). The low back-gate threshold voltage ($V_{\rm TB}$) of SOI MOSFET devices can degrade their performance, for example, by reducing the sub-threshold slope of the devices and increasing the off-state leakage current. Although shallow trench isolation (STI) technologies have been applied to nano-scale bulk CMOS, the local oxidation of silicon (LOCOS) technologies are still widely used in deep submicron SOI CMOS processes. For LOCOS-isolated SOI MOSFETs, we treated the back-channel transistor as the main transistor, but there is a parasitic leakage path from source to drain along the silicon island edge and it can be treated as a parasitic transistor paralleled with the main transistor[2−6]. The transfer characteristic of the back-channel is different from that of the front channel. As back-gate voltage increases, the parasitic transistor is turned on before the main transistor conducted. The main transistor turns on at a larger back-gate voltage, which is the main reason for the low back-gate threshold voltage (as is shown in Fig. 2).

Little attention has been given to this problem, and there are no domestic reports about the modification of back-gate threshold voltage by back-gate stress. Reference [7] reported that the $V_{\rm TB}$ of LOCOS isolated SOI NMOS devices can be

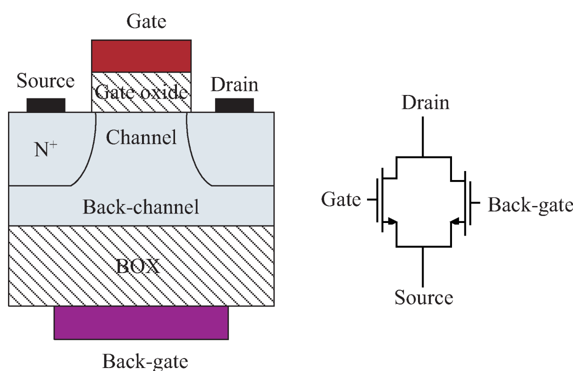

Fig. 1. Schematic diagram of back-gate transistor paralleled with the main transistor for an SOI NMOS device.

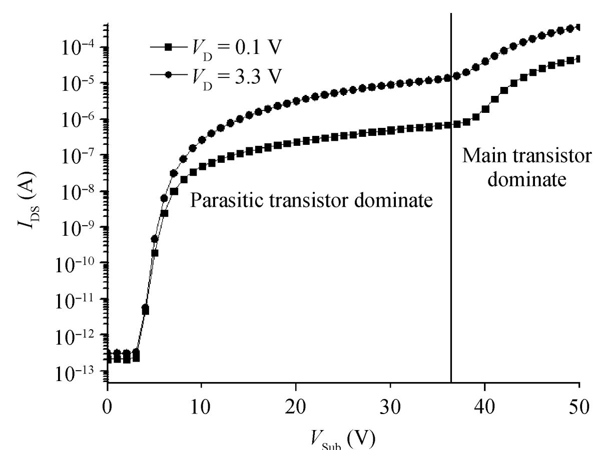

Fig. 2. Back-channel transfer characteristic of a 10/0.5 μm SOI NMOS device including kink.

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† Corresponding author. Email: zshan@ime.ac.cn

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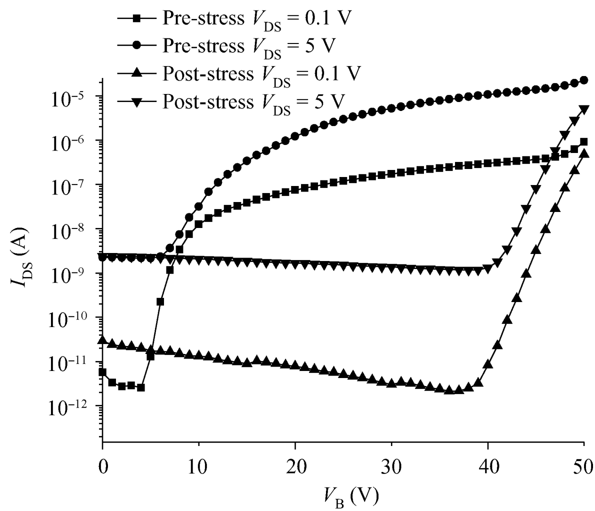


Fig. 3. Back channel transfer characteristic of an SOI NMOS device with the $W/L = 5/0.5$ before and after different back-gate stresses ($V_{GS} = 0$, $V_{DS} = 0.1$ V/$V_{DS} = 5$ V).

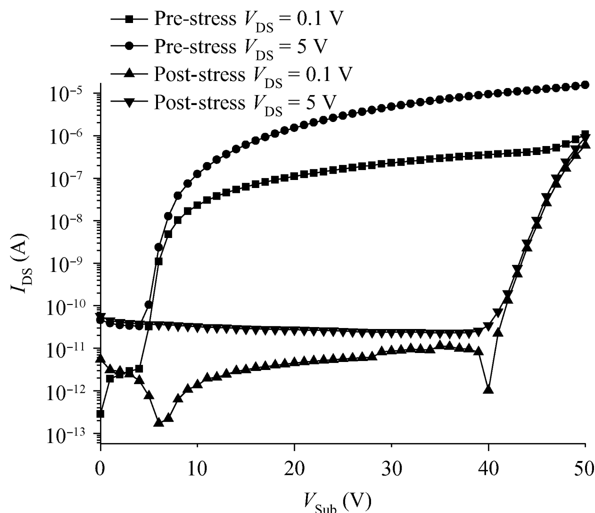


Fig. 4. Back channel transfer characteristic of an SOI NMOS device with the $W/L = 10/0.5$ before and after different back-gate stresses ($V_{GS} = 0$, $V_{DS} = 0.1$ V/$V_{DS} = 5$ V).

modified by application of a large back-gate bias with the gate, drain and source grounded at room temperature. However the V_{TB} of SOI PMOS devices were not investigated, and the principle of this effect is not given either. In this paper, a more complete and detailed experiment is proposed to explain the influence of large back-gate stress on the performance of SOI MOSFETs. A positive stress of $V_{Sub} = 120$ V was applied to the back-gate of an NMOSFET for 30 s to improve the V_{TB} of NMOSFET devices, while the negative stress of $V_{Sub} = -150$ V was applied to back-gate of a PMOSFET for 30 s to improve the V_{TB} of PMOSFET devices. All this was carried out at room temperature, and the experimental results are quite different from the PBTI (positive bias temperature instability) or NBTI (negative bias temperature instability) effect on MOSFET devices, because the modification of V_{TB} is stable and time invariant. We also investigated how back-gate stress changed the state of interface traps at the corner of BOX and bird beak

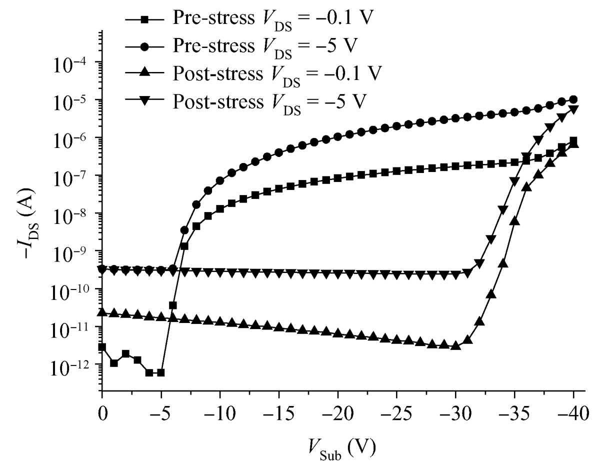


Fig. 5. Back channel transfer characteristic of an SOI PMOS device with the $W/L = 5/0.5$ before and after different back-gate stresses ($V_{GS} = 0$, $V_{DS} = -0.1$ V/$V_{DS} = -5$ V).

caused by LOCOS, which is the primary cause of improvement of back-gate threshold voltage by application of large back-gate stress.

2. Experiment

The devices were fabricated using a 0.5 μm SOI process developed by IMECAS. Both NMOS and PMOS are H-shape gate with a thickness of silicon film, gate oxide, and BOX of 200, 13 and 400 nm. They were fabricated on a UNIBOND SOI wafer, and local oxidation isolation (LOCOS) is performed to fully consume the active silicon layer in the isolation region. The channel doping concentration was 3×10^{17} cm^{-3}. The experiment results are representative of the other substrate materials (SIMOX) and other device structures.

The channel length of the devices used in this experiment is 0.5 μm, and the channel width is 10 μm and 5 μm respectively. To improve the V_{TB} of SOI NMOSFET devices, 120 V back-gate bias was stressed to the back-gate for 30 s with the gate, source and drain grounded. The main transistor characteristics were unaltered but the back-gate threshold voltage was improved, so the parasitic edge leakage had been eliminated. This was repeated for the SOI PMOSFET device, but we applied -150 V voltage bias to the back-gate for 30 s with the gate, source and drain grounded, and then the V_{TB} of the PMOSFET was also improved.

The absolute values of V_{TB} were improved for SOI NMOS and SOI PMOS devices by this method. Figures 3 and 4 show the SOI NMOS back channel transfer characteristics before and after application of the back-gate stress for two different device structures respectively, while Figures 5 and 6 show the SOI PMOS back channel transfer characteristics before and after back-gate stress for two different device structures respectively.

3. Results and discussion

One of the results in this experiment about the back-gate threshold voltage (V_{TB}) is shown in Table 1. The back-gate stress had significantly improved the V_{TB} of both NMOS and

Table 1. Back-gate threshold voltage before and after stress.

Device	V_{TB} before stress (V)	V_{TB} after stress (V)	V_{TB} after opposite stress (V)
NMOS $W/L = 5/0.5$	19	48	25
NMOS $W/L = 10/0.5$	17	50	15
PMOS $W/L = 5/0.5$	−20	−37	—
PMOS $W/L = 10/0.5$	−21	−36.5	—

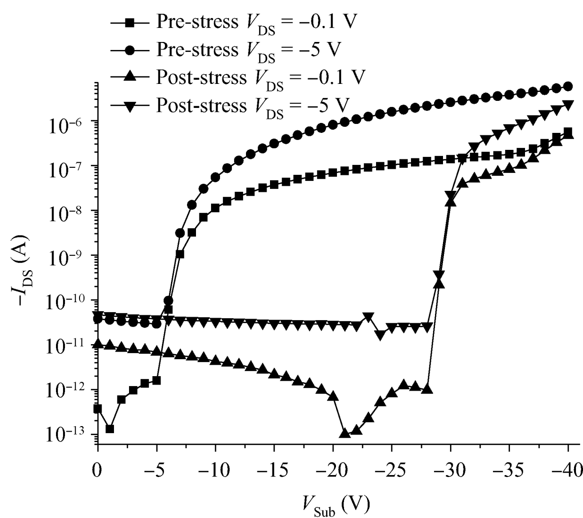


Fig. 6. Back channel transfer characteristic of an SOI PMOS device with the $W/L = 10/0.5$ before and after different back-gate stresses ($V_{GS} = 0$, $V_{DS} = -0.1$ V/$V_{DS} = -5$ V).

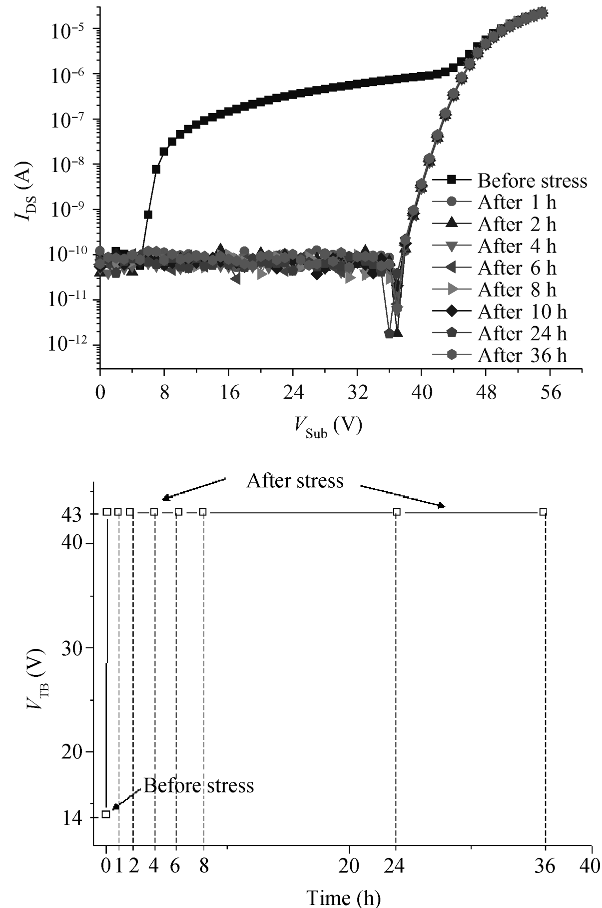


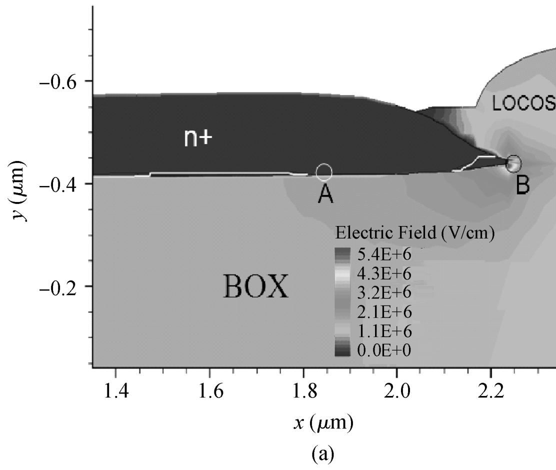
Fig. 7. Relationship of modification of V_{TB} and time. (a) Back channel transfer characteristic of $W/L = 5/0.5$ SOI NMOS devices. (b) V_{TB} of $W/L = 5/0.5$ SOI NMOS devices after stress as time goes on.

PMOS devices. We also found that the modification of V_{TB} was stable and would not change with time; the SOI NMOS device was taken as an example in Fig. 7.

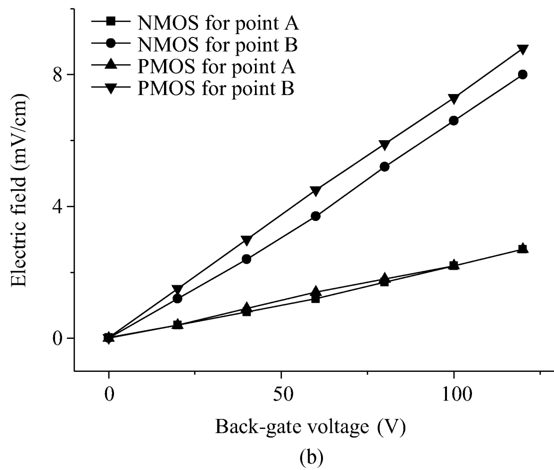
For SOI NMOSFET devices, the BOX and LOCOS introduce interfacial traps at the interface of Si/SiO_2. But these traps could be reduced or even eliminated by a process technology such as annealing in hydrogen or inert gases. In some reports, most of the interface traps were eliminated by annealing in hydrogen at low temperature (450 ℃), and the density of the interface trap can been reduced to 1×10^{10} cm^{-2}[10, 11]. But for LOCOS isolated SOI devices, some of the traps centralize at the corner of LOCOS and BOX (point B shown in Fig. 8), and those traps cannot be dispelled by annealing because of the stress produced by the volume expansion of LOCOS. So the parasitic leakage path from source to drain along the silicon island edge is induced by these traps at the corner of LOCOS and BOX, which, in this paper, we call corner traps.

All the traps are treated as an impurity energy level in the bandgap. Many researchers have tested the distribution of interfacial trap bands using various methods, and the results show there are two peak values of interfacial trap density in the bandgap[8]. One is near the top of the valence band and the other is near the bottom of the conduction band. One model, which was evidenced by experiment, attributes donor-like behavior to D_{it} (the density of interfacial traps) below E_i and acceptor-like behavior to D_{it} above E_i as shown in Fig. 9(a). Donor interface traps below E_F are occupied by electrons and hence are neutral. Those with energies $E_F < E < E_i$ are unoccupied donors and hence are positively charged. Those above E_i are unoccupied acceptors and are therefore neutral. For a different voltage bias the interface traps are occupied by electrons or not and hence are neutral, negative or positive. The energy band and electrical property of traps in the Si/SiO_2 interface is shown in Fig. 9[9]. But the corner trap band in the bandgap distribution is much more complex, there is no peak value. The corner traps in SOI NMOS always perform as donor traps and most SOI PMOS corner traps are acceptor traps. In this section we will use NMOS, for example, to explain the reasons why back-gate stress can improve the V_{TB}, but PMOS is also suitable.

The negative back-gate stress was applied to the SOI NMOS devices whose V_{TB} had been improved using positive back-gate stress. After 30 s we found that the V_{TB} of those SOI NMOS devices had been drawn back to the low values as before (see Fig. 10). (We defined V_{TB} as the voltage equal to the value of V_{Sub} when $I_{DS} = 10^{-6}$ of the back-channel transis-

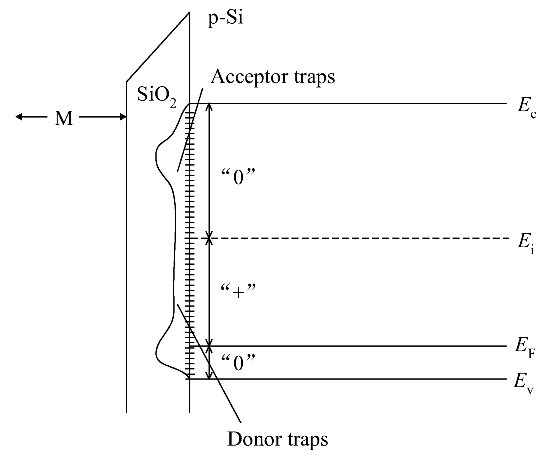


(a)

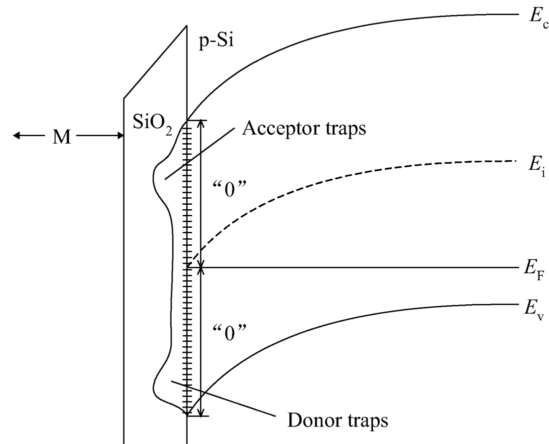


(b)

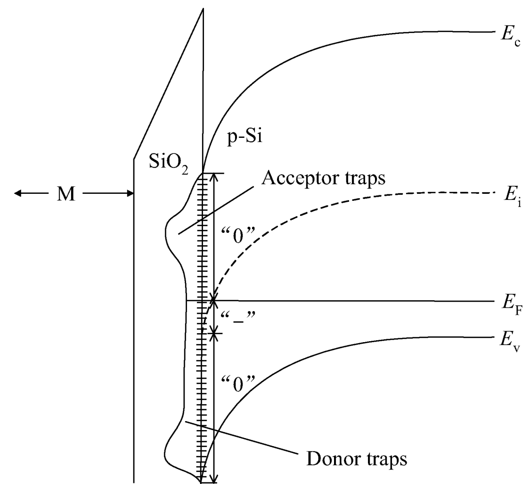
Fig. 8. Simulated electric field using ISE TCAD. (a) Simulated electric field structure schematic of SOI NMOS devices. (b) Simulated electric field as a function of back-gate bias.



(a) Interfacial trap band at flat band voltage



(b) $V_{\rm Sub} > 0$ for electron accumulation



(c) $V_{\rm Sub} \gg 0$ for the $E_{\rm F}$ get into acceptor trap band

Fig. 9. Trap energy band in SiO_2 at back channel for SOI NMOSFETs.

tor, so the $V_{\rm TB}$ and $V'_{\rm TB}$ in Fig. 10 are taking the 5/0.5 NMOS device as an example.) All the results could not be found in shallow trench isolated (STI) SOI devices in which there is no interface corner between BOX and STI. We came to the conclusion that the back-gate stress could change the state of the traps in the corner interface of BOX and LOCOS. We simulated the electric field of the back-gate characteristic using ISE TCAD. Figure 8(b) shows that the corner electric field (point B) is much larger than the interface electric field (point A).

We suspect that the density of interfacial traps in BOX is low and they do not have much influence on leakage. The traps at the corner of BOX and LOCOS are responsible for leakage, and the back-gate stress causes a large corner electric field that can change the state of corner traps. Before we applied back-gate stress to the SOI NMOS device, the donor traps were the main part of the corner traps. On a microscopic level some of the donor traps are occupied by electrons in the source region and they pass the electrons to the adjoining donor traps, which are then transported to the next one. So there is a source to drain leakage along the silicon island (see Fig. 11(a)). When we applied a 120 V bias to the back-gate and for 30 s, the energy band at the corner was changed and the Fermi energy level was moved, so the donor traps were all filled with electrons and could not transport electrons anymore (see Fig. 11(b)). So the parasitic leakage was eliminated and the $V_{\rm TB}$ of the SOI NMOS devices was improved. If we applied negative back-gate stress $V_{\rm B} = -120$ V for 30 s, some of the donor traps became empty again because the large corner electric field al-

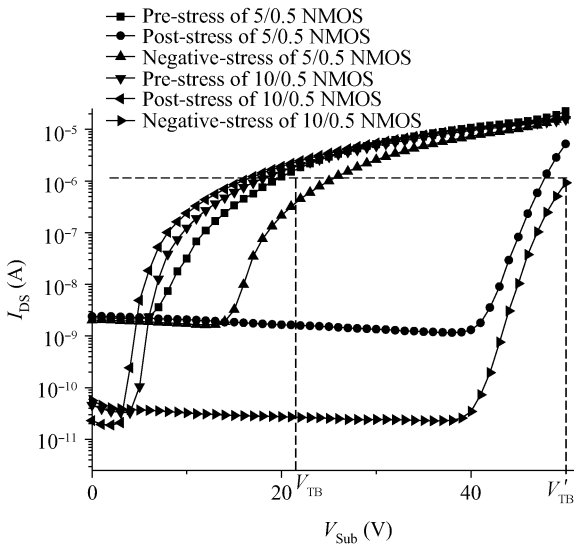


Fig. 10. Negative stress for the back channel transfer characteristic of SOI NMOS.

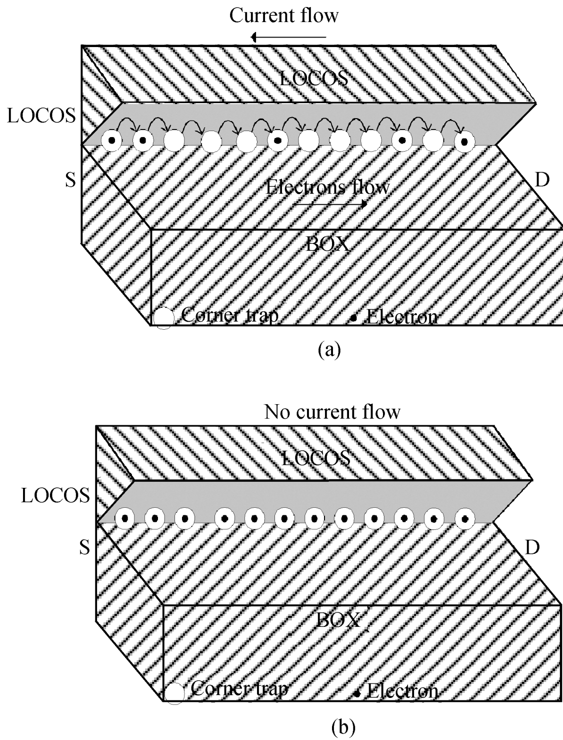


Fig. 11. Schematic diagram of trap transport electrons form source to drain for an SOI NMOSFET. (a) Before back-gate stress. (b) After 120 V back-gate stress.

tered the energy band.

For SOI PMOS devices, the majority of corner traps are acceptor traps, which can trap holes and create leakage along the silicon island. The negative back-gate $V_B = -150$ V introduced a large corner electric field and made the acceptor trap band change for the same reason, which eliminated leakage and improved the V_{TB} of the SOI PMOS devices. But when we applied positive back-gate bias for a certain time, the V_{TB} of SOI PMOS devices could not be drawn back to low values. Instead, the off-state current was so large that the devices were ruined by the large electric field. The reasons are still being investigated.

4. Conclusion

The back-gate threshold voltage of LOCOS isolated SOI MOSFET devices can be improved by application of a large back-gate stress for a certain time. The back-gate bias induces a large corner electric field at the corner of BOX and LOCOS, and the large electric field changes the state of corner traps, which are the main cause of source to drain leakage. For SOI NMOSFETs we can apply an opposite back-gate stress to draw V_{TB} back to the low value but the positive back-gate bias would ruin SOI PMOS devices.

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