A monolithic RF transceiver for DC-OFDM UWB*

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Abstract: This paper presents a first monolithic RF transceiver for DC-OFDM UWB applications. The proposed direct-conversion transceiver integrates all the building blocks including two receiver (Rx) cores, two transmitter (Tx) cores and a dual-carrier frequency synthesizer (DC-FS) as well as a 3-wire serial peripheral interface (SPI) to set the operating status of the transceiver. The ESD-protected chip is fabricated by a TSMC 0.13-μm RF CMOS process with a die size of 4.5×3.6 mm^2. The measurement results show that the wideband Rx achieves an NF of 5–6.2 dB, a max gain of 76–84 dB with 64-dB variable gain, an in-/out-of-band IIP3 of –6/+4 dBm and an input loss S_{11} of <-10 in all bands. The Tx achieves an LOLRR/IMGRR of –34/–33 dBc, a typical OIP3 of +6 dBm and a maximum output power of –5 dBm. The DC-FS outputs two separate carriers simultaneously with an inter-band hopping time of < 1.2 ns. The full chip consumes a maximum current of 420 mA under a 1.2-V supply.

Key words: DC-OFDM UWB; RF transceiver; receiver; transmitter; synthesizer; CMOS
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1. Introduction

Ultra-wideband (UWB) technology targeted at a data rate of up to 480 Mbps at 2 m is now in the ascendant of wireless communication technology for short distances. In February 2002, FCC allocated 7.5 GHz (3.1–10.6 GHz) for UWB applications. Afterwards different countries and organizations limited the available spectrum range of UWB systems according to their local policies. In January 2009, China's Ministry of Information Industry Technology (MIIT) approved spectrum use for UWB in China. It allows transmission of 4.2 to 4.8 GHz (low band, requirement of detect-and-avoid function) and 6 to 9 GHz (high band) with a maximum mean equivalent isotropic radiated power (EIRP) density of −41.3 dBm/MHz. Similar to WiMedia's multi-band orthogonal frequency division multiplexing (MB-OFDM) UWB standard[1], a dual-carrier orthogonal frequency division multiplexing (DC-OFDM) UWB standard has been proposed as China's national standard. It divides China's UWB spectrum into 24 bands with a bandwidth of 264 MHz and two bands are used as a band-pair to transmit or receive signals. The effective bandwidth is equal to that of the MB-OFDM standard. However, the speed as well as the design complexity of the ADCs and DACs is reduced and more flexibility in band configuration is achieved at the cost of doubling the amount of hardware, such as ADC, DAC, Rx, and Tx[2].

Although our earlier work on the design of RF modules for DC-OFDM-UWB RF transceivers has been reported[3−5], integration it into a monolithic RF transceiver chip hasn't been demonstrated yet. This paper focuses on the challenges brought by dual-carrier operation and offers a solution to developing the monolithic RF transceiver for DC-OFDM UWB. As shown in Fig. 1, the proposed DC-OFDM UWB transceiver adopts the direct-conversion architecture for full-chip integration and it is mainly composed of two identical receiver cores, i.e. Rx1 and Rx2, two identical transmitter cores, i.e. Tx1 and Tx2, and a dual-carrier frequency synthesizer, i.e. DC-FS.

To cover the entire high band of China's UWB spectrum, techniques are used to widen the bandwidth of the receiver and transmitter circuit design. The detailed circuit designs of the wideband Rx and Tx are described in Sections 2 and 3 respectively. And to cope with dual-carrier operation, the DC-FS is required to output two LO signals with separate frequencies simultaneously to drive the mixers either in the receivers or transmitters. The frequency plan, the architecture of the DC-FS as well as the circuits of the key modules are shown in Section 4. In addition, Section 5 presents the physical implantation and measurement results of this DC-OFDM UWB RF transceiver. Finally, comes the summary and conclusion.

2. Receiver and its circuit design[3]

As shown in Fig. 1 the zero-IF receiver chain contains the wideband low noise amplifier (LNA), the folded IQ down-conversion mixer and analog baseband (ABB) modules including the low pass filter (LPF) and the programmable gain amplifier (PGA).

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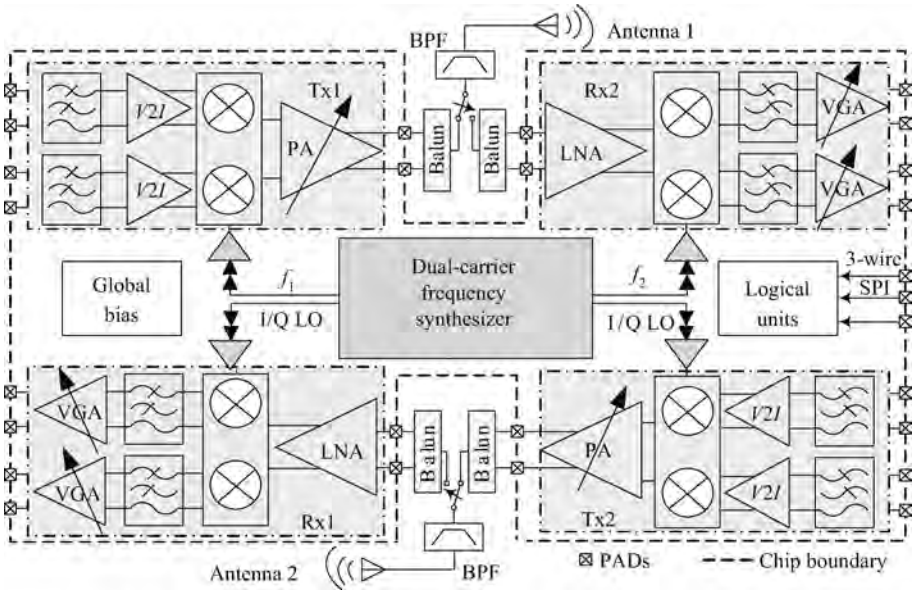

Fig. 1. Block diagram of the DC-OFDM UWB transceiver.

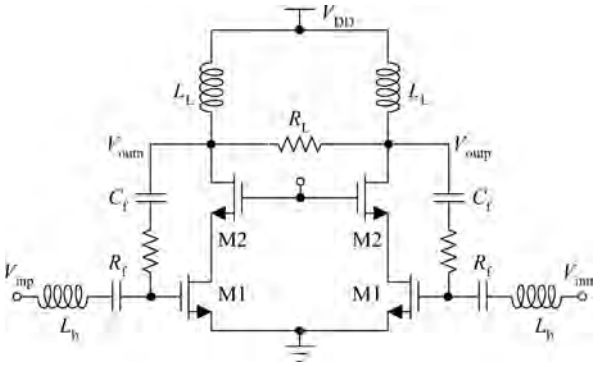

Fig. 2. Resistive feedback low noise amplifier.

2.1. Wideband RF front-end

The requirement of the RF front-end with a noise figure (NF) of less than 6 dB as well as wideband operation challenges the design of the LNA and down-conversion mixer. Techniques such as LC ladder[6], transformer feedback[7] and resistive feedback[8] are employed to obtain a wideband input impedance matching of the LNA. However, the size of the on-chip inductors and transformers is quite large. To minimize the chip area, a resistive shunt feedback LNA is adopted in this proposed UWB receiver and a fully differential structure is utilized to acquire immunity to the common-mode noise and interference.

As illustrated in Fig. 2, the core of the LNA is a common source amplifier formed by M1. A cascade transistor M2 is added to improve reverse isolation and reduce the Miller effect capacitance at the gate of M1, which degrades the broadband impedance matching. The gate of M2 is directly connected to VDD to guarantee the over-drive voltage of M1 greater than 500 mV, which improve its f_T and linearity. The resistor R_f is placed between the drain of M2 and the gate of M1 to provide a negative feedback path. In addition, the on-chip inductor L_L and resistor R_L form a wideband load network of the LNA.

The input impedance Z_{in} and the NF of the LNA can be derived as in Eqs. (1) and (2)[9]. From Eq. (1), we find that the input impedance $Z_{in} = R_f$ at DC. To gain impedance matching at low frequency, an initial value of R_f is set to be 50 Ω. As the frequency increases,

$$Z_{in} = \frac{\left(R_L R_f L C_p\right) s^2 + (R_L + R_f) L s + R_L R_f}{\left(R_L R_f L C_{gs} C_p\right) s^3 + a s^2 + b s + R_L}, \quad (1)$$

where

$$\begin{cases} a = R_L L \left(C_p + C_{gs}\right) + R_f L C_{gs}, \\ b = \left(1 + g_m R_L\right) L + R_L R_f C_{gs}, \end{cases}$$

C_p is the parasitic capacitance at the LNA output node. Capacitance C_{gs}, C_p, inductance L, and resistance R_L, R_f will determine Z_{in}. Also, Equation (1) shows that the wideband RLC load network introduces two zeroes which could reduce the impact of C_{gs} on input matching. By properly adjusting the value of the resistors and inductor according to the parasitic capacitance and trans conductance g_m, a good input matching with two resonate points is achieved.

$$\mathrm{NF} = 1 + \frac{(R_S + R_f)^2 \left(\gamma g_m + \dfrac{1}{R_L}\right) + (1 + g_m R_S)^2 R_f}{(1 - g_m R_f)^2 R_S}. \quad (2)$$

As in Eq. (2), the output noise is mainly contributed by the channel noise of M1 and the thermal noise of feedback resistor R_f. By increasing the trans conductance of M1, the feedback resistor will reduce the noise figure, but care should be taken to balance input impedance matching. A small sized cascode transistor M2 is able to reduce its parasitic capacitance.

In addition, the equivalent inductance of the input bonding wire L_b is the most significant factor of uncertainty during the design of the input matching network since the length of bonding wires depends on the final size and position of the die. Post simulated input return loss S_{11} verses different bonding wire inductance values indicate that S_{11} is less than –10 dB over

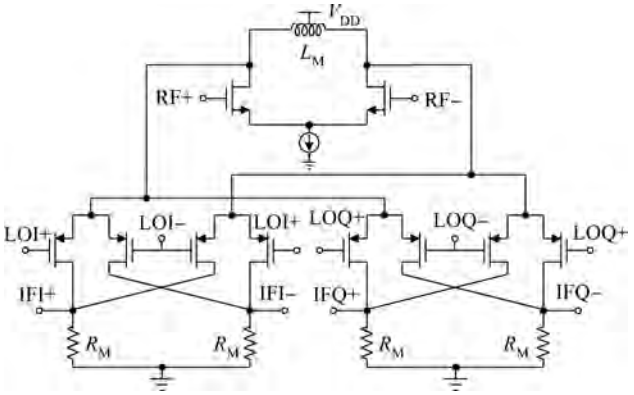

Fig. 3. Folded IQ merged down-conversion mixer.

6–9 GHz and a ±10% variation in the length of bonding wires can be tolerated.

The mixer down-converts received RF signals into IF signals. The conversion gain (CG) and $1/f$ noise are the main design consideration of the down-conversion mixer in this zero-IF receiver. As depicted in Fig. 3, a fully differential Gilbert cell based structure with IQ branches sharing the same RF input stage, say IQ merged down-conversion mixer, is adopted in this design[10]. It eliminates the mismatch in the separated IQ down-conversion mixers and minimizes the capacitive load to the LNA.

In this transceiver, the output voltage swing of the LO signal from the dual-carrier frequency synthesizer is around 250 mVp. The switches in this mixer operate in hard switching states, thus the conversion gain (CG) of the mixer is approximately that shown in Eq. (3).

$$\mathrm{CG} \approx \frac{2}{\pi} g_{\mathrm{m,RF}} R_{\mathrm{M}}, \tag{3}$$

where $g_{\mathrm{m,RF}}$ is the trans conductance of the input stage and R_{M} designates the load of the mixer. Thus the CG is determined mainly by $g_{\mathrm{m,RF}}$ and R_{M}. As the folded structure is utilized in this work, bias current in the input stage and switching stage can be set independently. A slightly large bias current is necessary in the input stage to obtain a moderate CG and a low NF. On the contrary, small current is preferred in the switching stage for reducing the $1/f$ noise and DC-offset, which are significantly important in a zero-IF receiver. Also, a variable gain is obtained by changing the value of the resistive load R_{M}.

2.2. Analog baseband

The analog baseband includes a low pass filter (LPF) and a programmable gain amplifier (PGA). The LPF eliminates the out-of-band inferences and the PGA adjusts the swing of the IF signal to fit the input range of the ADC.

A 5th-order Chebyshev LPF is adopted to fulfill the requirements of an out-of-band attenuation of 45 dB at $2f_{\mathrm{c}}$, an in-band ripple of < 1 dB and relatively good phase linearity. It has a real pole and two complex poles. As shown in Fig. 4, the real pole of the LPF is realized in the 1st-order RC filter while the two complex poles are formed in the Biquads, i.e. B_1 and B_2. To connect the LPF to the down-conversion mixer, the load resistors of the mixer, i.e. R_{M}, are shared as the resistors

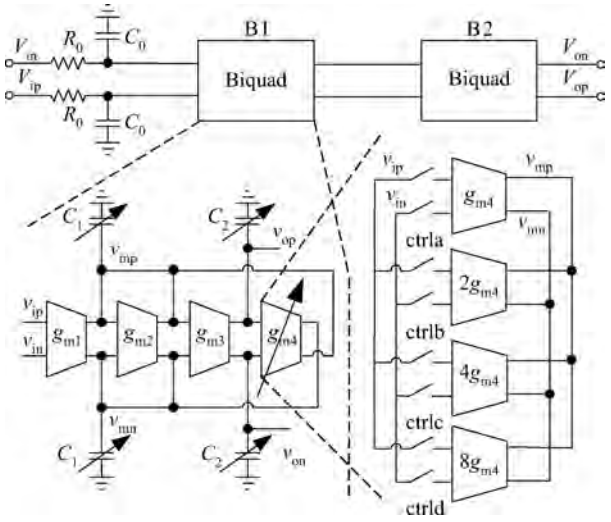

Fig. 4. Architecture of the 5th-order Chebyshev LPF.

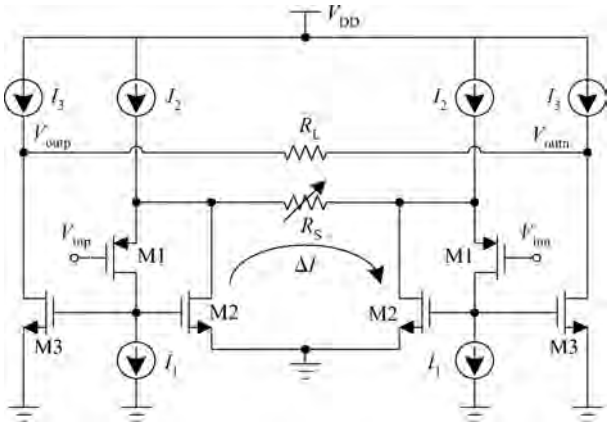

Fig. 5. Schematic of the PGA cell.

in the passive RC filter. In the circuit design, intensive simulations are carried out to optimize the overall frequency response of the mixer and the LPF.

The Biquad is composed of the trans conductors g_{m1}–g_{m4} as well as capacitors C_1–C_2. The variable trans conductor g_{m4} is realized by four parallel trans conductors. By switching the 1×-, 2×-, 4×-, 8×-g_{m4}, a variable gain of 36 dB is achieved with a gain step of 6 dB in this LPF. Also, the capacitors are implemented with digital controlled capacitor arrays (DCCAs) to compensate for process variations. Moreover, the g_{m} in the Biquads is built with Nauta's trans-conductor, which is suitable for high frequency applications since it has no internal nodes and no parasitic poles or zeros are introduced[11].

As the last stage of the Rx, the linearity of the PGA is the main design consideration. As illustrated in Fig. 5, the PGA in this Rx is based on an enhanced source degenerated circuitry[12]. The signals from the LPF are fed into the PGA via transistor M1. Transistor M2 as well as current source I_1 form the feedback loop. With the level-1 MOS model, the input IP3 of the PGA can be derived as in Eq. (4).

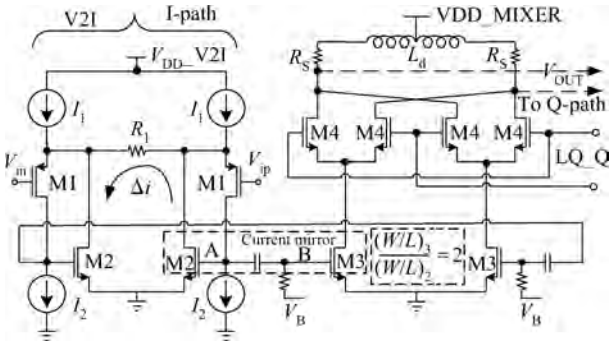

Fig. 6. Simplified I-path of the up-mixer.

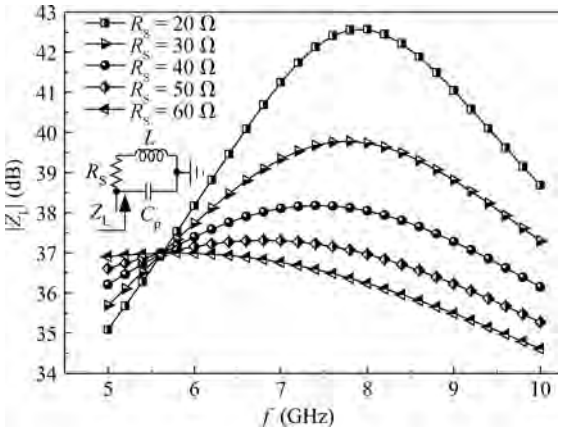

Fig. 7. Frequency response of up-mixer load versus R_s.

$$\text{IIP3} \approx 3.3 g_{m2} \frac{R_S}{2} \frac{I_1}{V_{GS} - V_{TH}} \frac{1}{\lambda I_1/2} (V_{GS} - V_{TH})$$

$$= 3.3 \frac{g_{m2} R_S}{\lambda}. \quad (4)$$

From Eq. (4), by increasing the loop gain $g_{m2}R_S$, a PGA with high linearity is achieved. However, a trade-off between linearity and power consumption needs to be made. As the gain of the PGA is proportional to the ratio of R_L and R_S, a programmable gain can be realized by switching the size of R_L and R_S. However, switching the size of R_L will change the frequency response of the PGA, which deteriorates the gain flatness. On the other hand, the linearity of the PGA is affected by the value of R_S as in Eq. (4). However, a large R_S is used when the input signal is large; the loop gain is large enough to ensure a high linearity of the PGA. The R_L is fixed in this design while R_S is variable. The PGA achieves a total voltage gain of 10–30 dB with a step of 2 dB. The gain flatness is within 1 dB from 1 to 300 MHz. The PGA consumes a current of 4.8 mA with an OIP3 of around +15 dBm.

3. Transmitter and its circuit design[4]

As shown in Fig. 1, this direct-conversion transmitter chain includes an IQ LPF, a single-sideband (SSB) up-mixer as well as a two-stage power driver amplifier (PA). The IQ LPF filters out the DAC image and spurs to reconstruct the ABB signals. Then they are up-converted into RF counterparts by the SSB mixer. Finally, the RF signals are boosted to the desired power level by the PA to drive the antenna. Because the LPF in the transmitter is similar to that in the Rx, its design method has been depicted in subsection 2.2. Therefore, the subsections of this part only present the detailed circuit design of the SSB up-mixer and the PA.

3.1. SSB up-mixer

As illustrated in Fig. 1, the SSB up-mixer acts as a modulator as well as an up-converter in this direct-conversion transmitter. Thus the performance of this transmitter is mainly determined by this circuit. As shown in Fig. 6, two double balanced Gilbert cells with their outputs are connected to form the SSB up-mixer. High linearity, low spurs and wideband operation are the main design challenges for this up-mixer.

A separate voltage-to-current (V2I) unit is employed to enhance the linearity of the up-mixer. With the help of the feedback loop, which is composed of transistors M1, M2, and current source I_2, the input voltage at the gate of M1 is effectively applied to resistor R_1 and is linearly converted into the current counterpart Δi. Then Δi circulates in M2 and is bridged into the switches of the SSB mixer via the current-mirror. The core circuit of the V2I is the same as that of the PGA. According to section 2.2, the linearity of the V2I is guaranteed as long as the loop gain is large enough. Therefore a high linearity SSB up-mixer is achievable. An AC coupling is used at the interface between the V2I and the switch stage for eliminating the dc-offset to reduce the LO leakage power at the SSB mixer output. A highly symmetric layout considering the IQ path as well as the differential path is desired to reduce the main spurs, i.e. the LO leakage and the sideband or the image.

Moreover, a broadband operation of the mixer is obtained by the wide-band load network composed of the differential inductor L_d, the parasitic capacitance C_p and two series resistors R_s. The single-ended AC equivalent circuit of the wideband load is shown in Fig. 7. Its impedance Z_L is derived as in Eq. (5), where $L_s = L_d/2$.

$$Z_L = (R_S + SL) // \frac{1}{SC_P} = \frac{R_S + SL}{1 + SR_S C_P + S^2 L C_P}. \quad (5)$$

The capacitance C_p is around 400 fF including the parasitic capacitors at the drain of M4 and the input capacitors of the PA. According to C_{par}, L_d is chosen as about 2 nH to make the conversion gain peaks around 7.5 GHz. With these parameters Z_L versus frequency at different R_s is plotted in Fig. 7. Larger R_s leads to a flatter frequency response but lower conversion gain. Finally, a 40-Ω R_s is selected to balance the gain and the ripple.

3.2. Power driver amplifier

The power driver amplifier (PA) boosts the RF signal from the SSB up-mixer to the required level to drive the off-chip antenna. Since the input capacitance of the main amplifier is usually large, it degrades the output bandwidth of the SSB up-mixer.

A two-stage PA is employed as shown in Fig. 8. The 1st stage is a combination of source follower (M1) and common

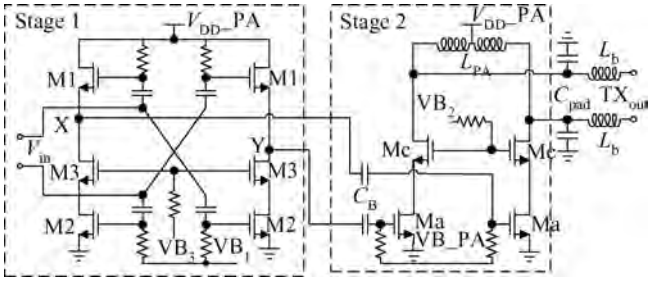

Fig. 8. Simplified schematic of the two-stage PA.

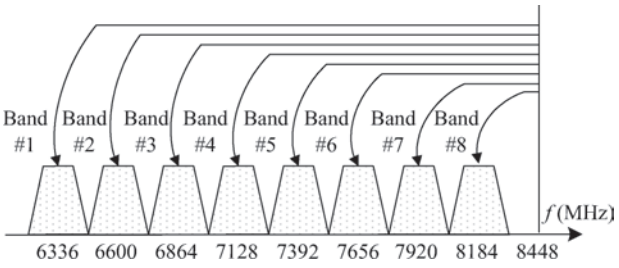

Fig. 9. Frequency plan of the proposed DC-FS.

source amplifier (M2)[13] to lower the loading effect of the PA to SSB mixer and to increase the common-mode rejection ratio of the transmitter. The 2nd stage is the main amplification unit. Its linearity as well gain is important. Therefore a class-A common source amplifier (Ma) is employed. A differential inductor L_{PA} is used to resonate with the parasitic capacitance at the output node and the capacitance of the PAD C_{pad}. The value of L_{PA} is optimized with C_{pad} and bonding inductance L_b to ensure the peak of the gain is around 9 GHz to compensate the gain drop at high frequency. Also, the cascode transistors M3 and Mc are utilized to reduce the miller capacitance and avoid the breakdown of the transistors during a large signal period.

4. Dual-carrier frequency synthesizer[5]

Due to a required inter-band hopping time of less than 9.5 ns, the conventional phase-locked-loop (PLL) based synthesizers are ill-suited. While the SSB-mixer based ones are commonly adopted to generate the desired frequency within nanoseconds by switching the input frequency of the SSB mixer[14−16]. However, the mismatch and nonlinearity of the SSB mixer produce spurs all over the spectrum due to cross-products of the input harmonics. Therefore, the number of SSB mixers should be minimized. As a rule, the fewer SSB mixers used, the fewer spurs at output could be expected. On the other hand, the number of SSB mixers is directly related to the frequency plan of the synthesizer.

As a prototype design for the DC-OFDM UWB system, the synthesizer outputs only eight frequencies from 6336 to 8184 MHz with an interval of 264 MHz. The proposed frequency plan is shown in Fig. 9. A center frequency of 8448 MHz is chosen. The desired eight frequencies are produced as Eq. (6).

$$f_{FS\_out} = 8448 - 264n, \quad n = 1, 2, \cdots, 8. \tag{6}$$

According to the above frequency plan, the architecture of the proposed dual-carrier frequency synthesizer (DC-FS) is given in Fig. 10. The quadrature VCO (QVCO) in the PLL oscillates at 8448 MHz. The divider-by-2 divider chain creates all of the required intermediate frequencies. The desired frequencies are obtained by mixing all the intermediate frequencies with the output of the QVCO.

In this way the synthesizer uses only one PLL, a divided-by-2 divider chain, two SSB mixers and three frequency multiplexers (MUX) to generate the eight carriers. By duplicating the frequency synthesizing part, the DC-FS can output two carriers with separate frequencies simultaneously. Besides, an IQ calibration buffer is inserted before SSB mixer 2 and 4 respectively to calibrate the IQ mismatch of the switchable intermediate frequencies. The IQ LO buffers based on an LC-loaded common source amplifier are also included in this DC-FS to drive mixers either in the transmitters or the receivers.

Referring to the circuit design of the DC-FS, the QVCO is considered as the key module in the PLL since its phase noise determines the overall PLL output noise performance. As shown in Fig. 11, the QVCO adopts a complementary cross-coupled topology with separate tail current sources for each VCO core. The noise contribution of the coupling differential pair is decreased by separating its current source from that of the main differential pair. The resonators are made of a differential inductor with an array of 5-bit binary weighted switched capacitors and thick oxide MOS varactors. The tuning voltage ranges from 0 to 1.2 V. A small $K_{vco} = 75$ MHz/V is adopted to achieve low AM-FM noise conversion.

Another key module in the DC-FS is the MUX. As shown in Fig. 12, the core of the basic 2-to-1 MUX consists of two differential pairs (M1 & M2, M5 & M6) sharing a common resistance load R_L. When Sel is high and Selb is low, V_{in1} is selected as the output. Otherwise, V_{in2} equals V_{out}. Furthermore, two source-coupled dummy transistor pairs (M3 & M4, M7 & M8) are added to reduce the port-to-port leakage, which is the main issue in the design of MUX. For example, when V_{in1} is selected, the other input V_{in2} leaks to the output node through two different paths, i.e. the differential pair M5, M6 and the dummy pair M7, M8. Because the drains of the dummy pair are cross-coupled at the output node, the leakage of V_{in2} from the differential pair is eliminated. When V_{in2} is selected, the leakage of V_{in1} at the output is eliminated in the same way. The gate of the dummy tail current source is connected to the ground. Hence, good isolation is achieved without extra power consumption. Post simulation results indicate that the port-to-port isolation in improved by about 30 dB with the dummy pairs. By connecting more MUX of this type in parallel, an N-to-1 frequency MUX with low port-to-port leakage is obtained[17].

Besides, the SSB mixer consists of two double balanced mixers with IQ inputs to realize the frequency summing or subtracting. Two types of SSB mixer are used in this design. SSB mixer 1/3 operates in a relatively low frequency around 4 GHz. A resistive load is employed. SSB mixer 2/4 works in a higher frequency up to 9 GHz. An inductive load is used to achieve a broadband operation. Band selection is accomplished by adding capacitor arrays to change the resonance frequency of the tank. The operation principle of these SSB mixers in the DC-FS is the same as that in the Tx. The design method in subsection 3.1 can be used.

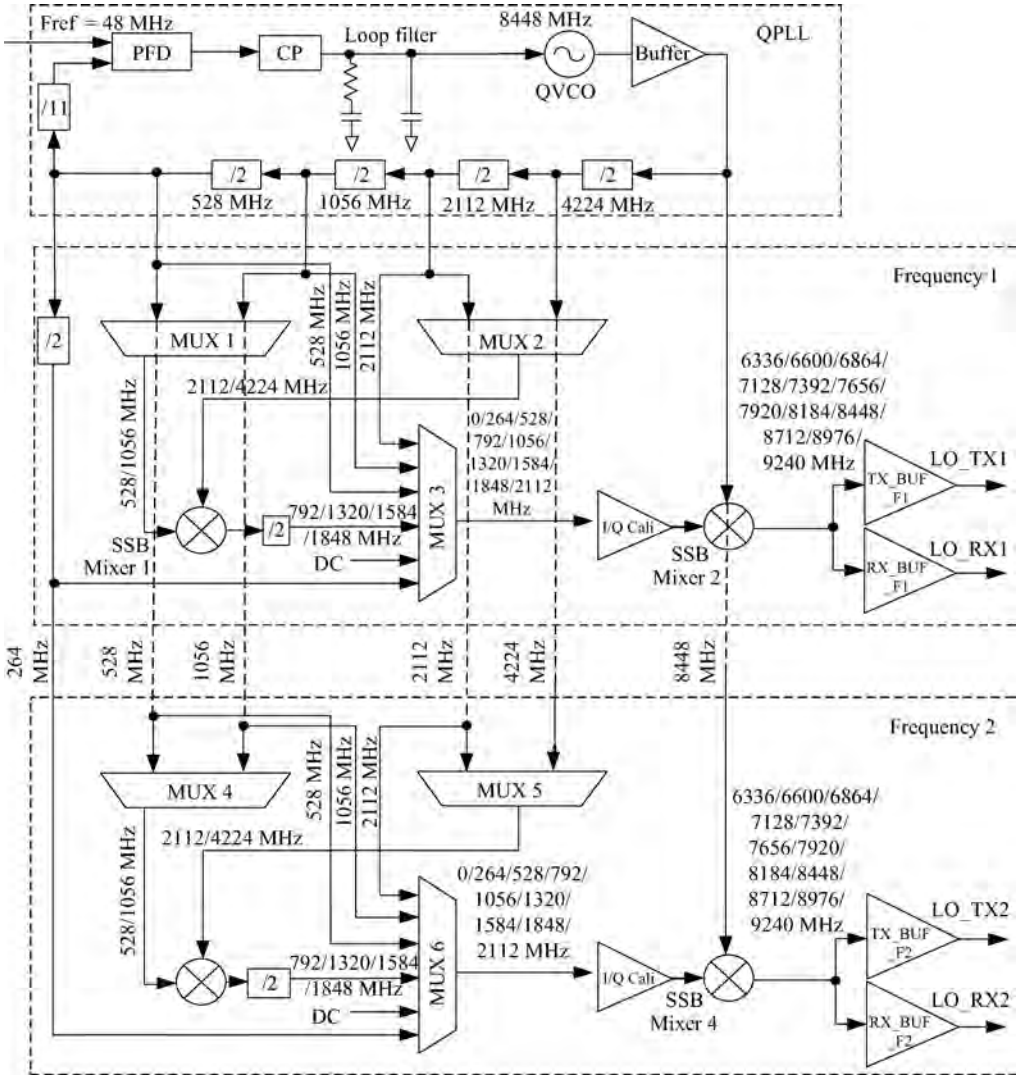

Fig. 10. Architecture of the proposed DC-FS.

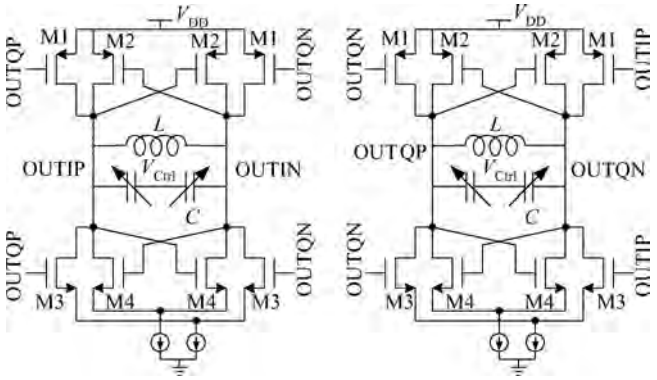

Fig. 11. Simplified schematic of the QVCO.

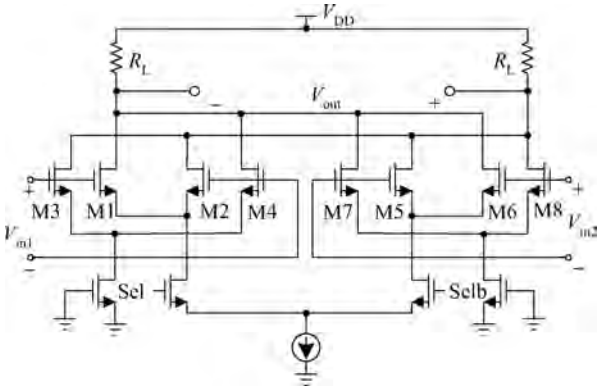

Fig. 12. Schematic of the 2-to-1 MUX.

5. Measurement results

This DC-OFDM monolithic transceiver chip is fabricated using a TSMC 0.13-μm RF CMOS process with dimensions of 4.5 × 3.6 mm^2. As shown in Fig. 13, the receivers and transmitters are at the top and bottom side of the chip respectively. The DC-FS with LO buffers are placed at the center for ease of providing LO signals to both Rxs and Txs. In addition, the 3-wire SPI with logic unit controlling the operating status of the transceiver is also integrated.

The transceiver is bonded to the PCB with a chip-on-board (COB) package for test as illustrated in Fig. 14. The RF inputs of the Rxs and the RF outputs of the Txs are placed at the

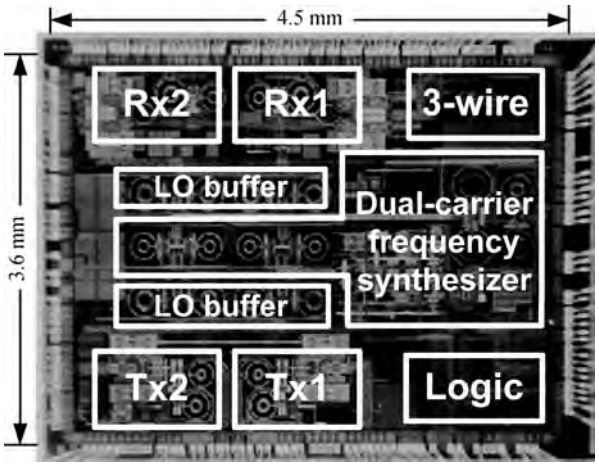

Fig. 13. Microphotograph of the transceiver chip.

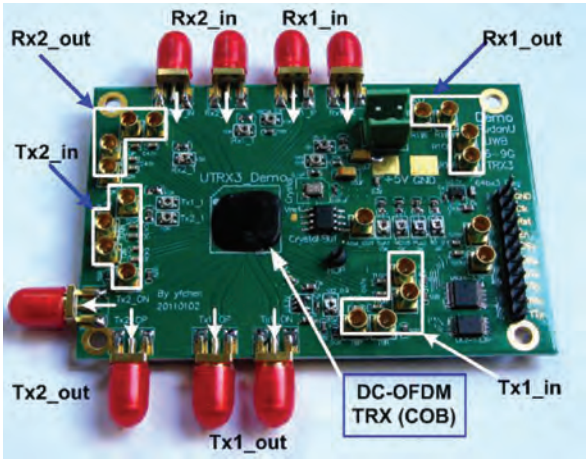

Fig. 14. Test PCB of the transceiver chip in a COB package.

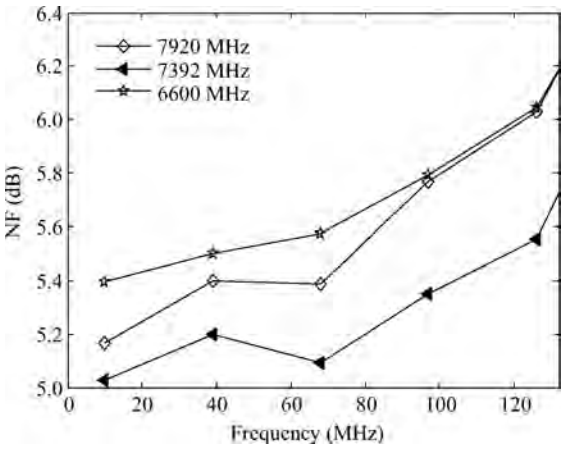

Fig. 15. NF of the Rx in typical bands at maximum gain.

top and bottom of the PCB in accordance with the chip layout floor plan. The ABB signals are connected using the small SMA connectors to save the PCB area. Besides, a crystal oscillator is mounted on the PCB to provide the accurate 48-MHz reference for the DC-FS. When the chip is tested, the control words are sent by the digital baseband processor or the PC using a single-chip machine (SCM) via the 3-wire SPI.

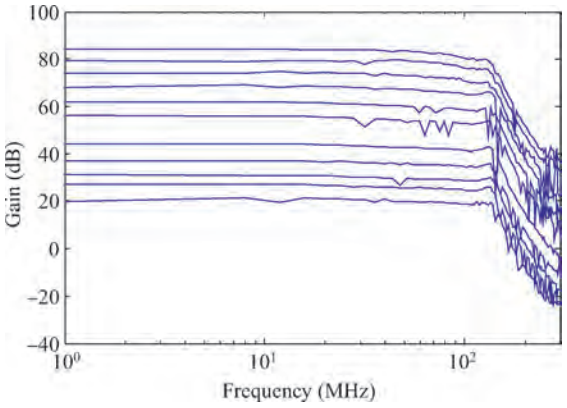

Fig. 16. Rx frequency response under different gains.

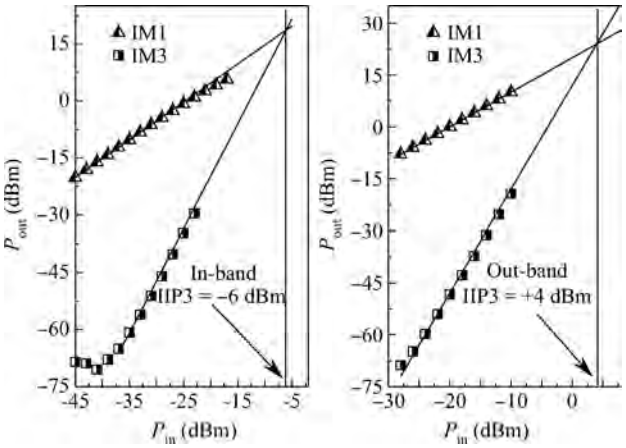

Fig. 17. In-/out-of-band input IP3 of the Rx at 6600 MHz.

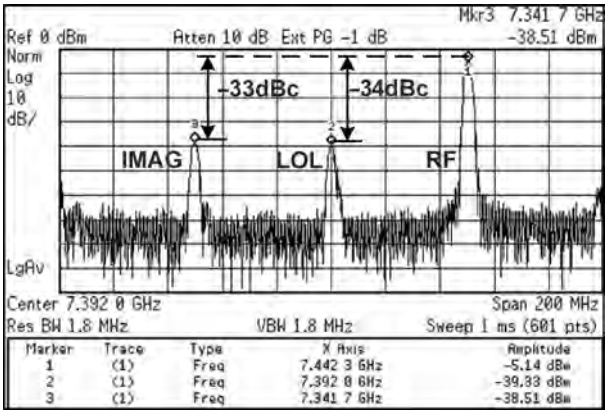

Fig. 18. Output spectrum of Tx at 7392-MHz LO.

As shown in Fig. 15, the measured NF of the entire Rx chain is 5–6.2 dB within a 132-MHz bandwidth at a maximum gain setting excluding a 1.5-dB insertion loss of the balun and the PCB trace.

The minimum conversion gain of the Rx is around 20 dB and the variable gain is 64 dB with a minimum step of 2 dB as depicted in Fig. 16 (only a section of the graph is shown for clarity of the figure).

The in-band and out-of-band input IP3 of the Rx is –6 dBm

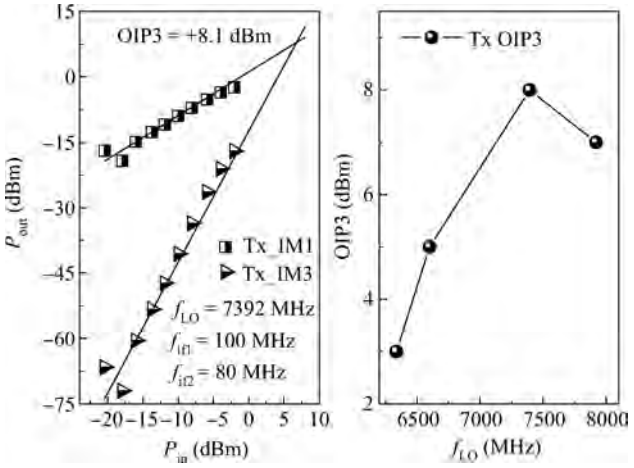

Fig. 19. Output IP3 of Tx at various bands.

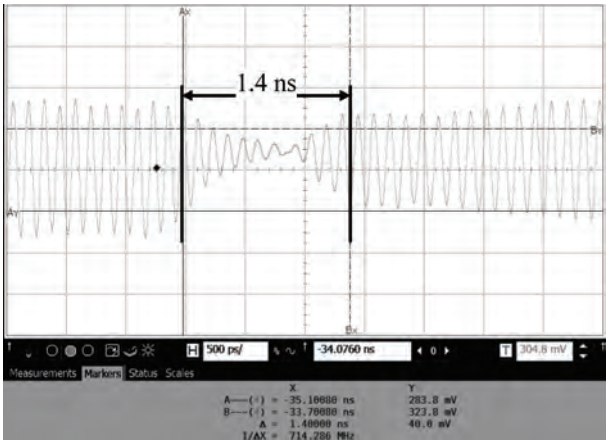

Fig. 20. Hopping time of the DC-FS.

Table 1. Measurement result summary.

Module	Parameter	Measured result
Rx	NF (dB)	5.0–6.2
	S_{11} (dB)	< -10 (6–9 GHz)
	Gain (Max, dB)	78–84 (variable gain 64 dB)
	In-/out-of-band IIP3 (dBm)	–6/+4 (typical)
	Current (Max) (mA)	60 × 2@1.2 V
Tx	LOLRR/IMGRR (dBc)	–34/–34 (typical)
	Output power (dBm)	–27 to –5@0 dBm ABB input
	OIP3 (dBm)/OP_{1dB} (dBm)	+3 to +8/–7 to –2
	Current (Max) (mA)	50 × 2 @ 1.2 V
DC-FS	Output f_{LO} (MHz)	$8448 - 264n (n = 1, 2, 3, \ldots, 8)$
	Output LO number	2 (separate f_{LO} control)
	Phase noise @ 1 MHz (dBc/Hz)	–105
	RMS noise	$< 2^\circ$
	Reference spur (dBc)	< -70 (typical)
	Current (mA)	160–200 @ 1.2 V (with LO buffers)
	Hopping time	< 1.2 ns
Full chip	Power supply (V)	1.2
	Current (Max) (mA)	420 = 120(RXs) + 100(TXs) + 200(DC-FS)
	Area (mm^2)	3.6 × 4.5

Table 2. Performance comparison.

Parameter	This work	Ref. [8]	Ref. [18]
Process (μm)	CMOS 0.13	CMOS 0.18	CMOS 0.18
Operating frequency (GHz)	6–9	3–5	3.1–8.0
Standard (UWB)	DC-OFDM	MB-OFDM	MB-OFDM
Rx variable gain (dB)	20–84	13–68	25.3–84
Rx NF (dB)	5–6.2	5.5–8.8	6.5–8.25
Rx IIP3 (dBm)	−6	−4	−13.7 to −12.6
Tx OIP3/OP_{1dB} (dBm)	+3 to +8/−7 to −2	+2 to +11/−10.7 to −3	−8.2 to −6.8/ > −7
Phase noise (dBc/MHz)	–105 @ 1 MHz	–103.4 @ 1 MHz	–127 @ 10 MHz
RF transceiver power (mW)	504* @ 1.2 V	288 (Rx)/183 (Tx) @ 1.8 V**	285(Rx)/139(Tx) @ 1.8 V**
Area (mm^2)	16.2	6.1	15.4 (wi ADC&DAC)

*: All blocks (2Rx+2Tx+DC_FS) are turned on with Txs and Rxs at max gain setting; **: including power of synthesizer.

and +4 dBm at a typical LO frequency. From Figs. 15, 16 and 17, the main measuring results of the Rx chain have revealed that the Rx in this transceiver is of low noise and high linearity with sufficient gain. Also, the measured input return loss S_{11} is less than –10 dB from 6 to 9 GHz. Hence, a wideband high performance Rx is achieved.

The Tx output spectrum at 7392-MHz LO is shown in Fig. 18, the LO leakage rejection ratio (LOLRR) is –34 dBc and the image rejection ratio (IMGRR) is –33 dBc when the output power is –5 dBm.

By scanning the input power of the two-tone ABB signal (80 MHz and 100 MHz), an output IIP3 of +8.1 dBm is measured at 7392-MHz LO as depicted in Fig. 19. However, the OIP3 of the Tx drops to +3 dBm at 6600-MHz LO because of insufficient LO swing from the DC-FS to drive the Tx SSB mixers. Also the measured conversion gain of the Tx varies only 3 dB in 6–9 GHz and the output return loss S_{22} is less than –8 dB in 6–9 GHz with a minimum S_{22} of –10 dB at around 7.5 GHz.

Figure 20 gives the hopping transient waveform of the DC-FS captured by Agilent's real-time oscilloscope DSO9000. It indicates that 1.4 ns are sufficient for this DC-FS to change its output frequency, which is less than the requirement of 9.5 ns.

Finally, all the measured key parameters of the proposed DC-OFDM-UWB RF transceiver are summarized in Table 1 and the performance comparison is given in Table 2.

6. Conclusion

A monolithic direct-conversion RF transceiver for DC-OFDM UWB applications is proposed and implemented in a TSMC 0.13-μm RFCMOS process. Measurement results show that the wideband Rx achieves an NF of 5–6.2 dB, a max gain of 76$\sim$84 dB with a 64-dB variable gain. The Tx achieves a LOLRR/IMGRR of –34/–33 dBc, a typical OIP3 of +6 dBm. The DC-FS outputs two LOs with an inter-band hopping time of < 1.2 ns. The full chip occupies 16.2 mm^2 with a maximum power consumption of 504 mW. As in Table 2 with a dual-carrier operation, the proposed RF transceiver achieves a comparable performance with other MB-OFDM transceivers. It validates the proposed design methods for wideband circuitry. This paper provides a solution to integration of monolithic DC-OFDM-UWB RF transceivers for the first time.

References

[1] Multi-band OFDM physical layer proposal for IEEE 802.15 task group 3a. IEEE P802.15 Working Group for Wireless Personal Area Networks, Mar. 2004

[2] Zhang Zaichen, Bi Guangguo. A DC-OFDM UWB wireless communication system. Chinese High Technology Letters, 2007, 17(7): 676

[3] Gao T, Zhou F, Li W, et al. A 6.2–9.5 GHz receiver for Wimedia MB-OFDM and China UWB standard. Sci China Inf Sci, 2011, 54(2): 407

[4] Chen Yunfeng, Gao Ting, Li Wei, et al. A dual-mode 6–9 GHz transmitter for OFDM-UWB. Journal of Semiconductors, 2011, 32(5): 055004

[5] Fu Haipeng, Cai Deyun, Chen Danfeng, et al. A low-spurious fast hopping 12-band synthesizer for dual-carrier MB-OFDM UWB applications. Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), 2011: 2873

[6] Zhou Feng, Gao Ting, Lan Fei, et al. A low noise CMOS RF front-end for UWB 6–9 GHz applications. Journal of Semiconductors, 2010, 31(11): 115009

[7] Bevilacqua A, Niknejad A M. An ultrawideband CMOS low-noise amplifier for 3.1–10.6-GHz wireless receivers. IEEE J Solid-State Circuits, 2004, 39(12): 2259

[8] Zheng Renliang, Jiang Xudong, Yao Wang, et al. A monolithic 3.1–4.8 GHz MB-OFDM UWB transceiver in 0.18-μm CMOS. Journal of Semiconductors, 2010, 31(6): 065007

[9] Shin D H, Park J, Yue C P. A low-power, 3–5-GHz CMOS UWB LNA using transformer matching technique. IEEE ASSCC Dig Tech Papers, 2007: 95

[10] Sjöland H, Karimi-Sanjaani A, Abidi A A. A merged CMOS LNA and mixer for a WCDMA receiver. IEEE J Solid-State Circuits, 2003, 38(6): 1045

[11] Nauta B. A CMOS transconductance-C filter technique for very high frequencies. IEEE J Solid-State Circuits, 1992, 27(2): 142

[12] Sansen W. Analog design essential. Springer Press, 2006

[13] Kim C W, Lee S S, Park B H, et al. A CMOS direct-conversion I/Q up-mixer block for ultra-wideband system. Adv Commun Technol, 2005: 230

[14] Wang C S, Li W C, Wang C K, et al. A 3–10 GHz full-band single VCO agile switching frequency generator for MB-OFDM UWB. IEEE Asian Solid-State Circuits Conference, 2007: 75

[15] Huang Z, Kuo F, Wang W, et al. A 1.5-V 3–10-GHz 0.18-μm CMOS frequency synthesizer for MB-OFDM UWB applications. MTT-S International Microwave Symposium Digest, 2008: 229

[16] Lu T Y, Chen W Z. A 3-to-10 GHz 14-band CMOS frequency synthesizer with spurs reduction for MB-OFDM UWB system. IEEE International Solid-State Circuits Conference, 2008: 126

[17] Chen D F, Fu H P, Chen Y F, et al. A sideband-suppressed low-power synthesizer for 14-band dual-carrier MB-OFDM UWB transceivers. Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), 2010: 2139

[18] Zheng H, Lou S Z, Lu D T, et al. A 3.1 GHz–8.0 GHz single-chip transceiver for MB-OFDM UWB in 0.18-μm CMOS process. IEEE J Solid-State Circuits, 2009, 44(2): 414