A 1.2-V CMOS front-end for LTE direct conversion SAW-less receiver*

Wang Riyan(王日炎)[1], Huang Jiwei(黄继伟)[2, 3, †], Li Zhengping(李正平)[1], Zhang Weifeng(张伟峰)[1], and Zeng Longyue(曾隆月)[1]

[1]Guangzhou Runxin Information Technology Co. Ltd, Guangzhou 510663, China
[2]College of Physics and Information Engineering, Fuzhou University, Fuzhou 350002, China
[3]Institute of RF- & OE IC, Southeast University, Nanjing 210096, China

Abstract: A CMOS RF front-end for the long-term evolution (LTE) direct conversion receiver is presented. With a low noise transconductance amplifier (LNA), current commutating passive mixer and transimpedance operational amplifier (TIA), the RF front-end structure enables high-integration, high linearity and simple frequency planning for LTE multi-band applications. Large variable gain is achieved using current-steering transconductance stages. A current commutating passive mixer with 25% duty-cycle LO improves gain, noise and linearity. A direct coupled current-input filter (DCF) is employed to suppress the out-of-band interferer. Fabricated in a 0.13-μm CMOS process, the RF front-end achieves a 45 dB conversion voltage gain, 2.7 dB NF, –7 dBm IIP3, and +60 dBm IIP2 with calibration from 2.3 to 2.7 GHz. The total RF front end with divider draws 40 mA from a single 1.2-V supply.

Key words: RF CMOS; front-end; passive mixer; 25% duty-cycle; variable gain; quadrature demodulator
DOI: 10.1088/1674-4926/33/3/035005 **EEACC:** 2570

1. Introduction

The direct-conversion receiver (DCR) has attracted widespread attention recently for its simple architecture and high integration. For multiple channel bandwidths operation, wide-bandwidth signals can be more easily accommodated in DCR with an on-chip lowpass filter, rather than the off-chip bandpass filter. As a result, a low-frequency ADC can be inserted to demodulate the incoming signal, which enables the possible development of a multi-band receiver to detect many standard signals simultaneously[1]. In addition, RF CMOS offers the potential for low cost. Until now, the DCR has become a dominant integrated circuit (IC) technology for GSM, GPRS[2], CDMA[3], and WCDMA[4].

The development of the WCDMA communications standard towards increasing user demands is currently standardized by third Generation Partnership Project (3GPP) as long term evolution. LTE standards support a large number of bands from 700 to 2700 MHz, and also tremendous channel bandwidths from 1.4 to 20 MHz. LTE transceivers will also benefit from the use of multiple-input and multiple-output (MIMO) technology which increases the data throughput by introducing spatial diversity. Since MIMO relies on using several receiver chains simultaneously, it is strongly desired to have a highly-integrated monolithic solution for mobile terminals[5].

In a frequency division duplexing (FDD) system, the transmitter and receiver are on simultaneously. A duplexer is used to isolate the receiver from the transmit signal but the isolation at the transmitter (TX) frequency is not more than 55 dB. The TX maximum output power at the PA is +25 dBm and the receiver will see a TX leakage of up to –30 dBm. The typical solution deals with the TX blocking problem by using an external LNA and receiver (RX) inter-stage SAW filter to achieve sufficient RX linearity. In time division duplexing (TDD) mode, however, the receiver does not need an inter-stage SAW filter between LNA and mixer. With the development of multi-mode and multi-band transceiver, there is a strong demand to reduce the need for inter-stage SAW filters.

In this paper, a 1.2-V RF front-end with 25% LO for LTE direct conversion receiver fabricated in 0.13-μm CMOS process is presented. High out-of-band linearity performance is achieved by reducing the RF circuitry and filtering the out-of-band blockers after direct down conversion. The 25% duty-cycle LO results in higher signal conversion efficiency and lower noise sensitivity relative to a 50% duty-cycle implementation.

2. Architecture

Figure 1 shows the blocks diagram of RF front-end for LTE receiver. RF frequency from 2300 to 2700 MHz is supported, which includes band 7/38/40 in LTE standards. The duplex mode of band 7 is FDD, with a TX to RX carrier centre frequency separation of 120 MHz. The duplex mode of band 38 and band 40 is TDD. The receiver architecture is a direct conversion without any inter-stage SAW filters.

In the presence of a strong modulated TX blocker at the receiver input, the total noise at the output of the receiver consists of four contributions: the IC RX noise figure, the TX noise in the RX band, the reciprocal mixing of the TX blocker and the second order intermodulation (IM2). Targeting on a 0.2 dB noise-figure degradation at maximum TX power due to recip-

* Project supported by the National High-Tech R&D Program of China (No. 2009AA01Z260), the Guangdong Science and Technology Program (No. 2009A010100004), and Guangdong & Hong Kong Cooperation Key Area 2010 (No. 2010498E1).
† Corresponding author. Email: seuhjw@seu.edu.cn
Received 5 August 2011, revised manuscript received 24 October 2011

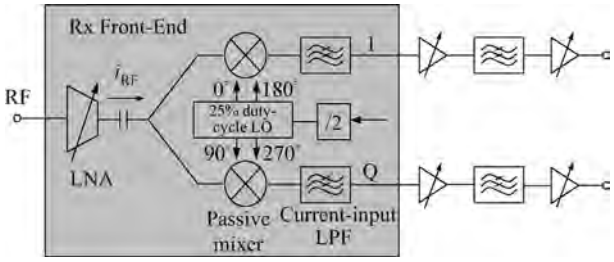

Fig. 1. Block diagram of RF front-end for LTE receiver.

rocal mixing and IM2 products, then the LNA referred receiver requirement is an IIP2 > +55 dBm and LO phase noise < –156 dBc/Hz at >120 MHz offset.

There are many obstacles in CMOS direct conversion receiver design, including the flicker noise, DC offset, and second-order inter-modulation (IM2). These problems can be efficiently relaxed by using current-commuting passive mixers in RF front-end[6, 7]. To improve the front-end linearity, a current-input low pass filter (LPF) following the mixer is utilized. The impedance of the current-input LPF is relatively low, therefore the voltage swing is reduced at the output of the mixer and the mixer linearity is improved. Additionally, the out-of-band interferer will be sufficiently suppressed at the output of current-input LPF, comparing to the transimpedance amplifier with a real pole[7]. The low voltage swing enables a low voltage supply in base-band design. Both of the methods improve the linearity and enlarge the dynamic range. To improve the ability of handling large signals, more than 36 dB gain control is designed in the low noise transconductance stage. The 25% duty-cycle LO eliminates crossover of the non-ideal 0° and 180° LO pulses. This topology results in 3 dB more gain, a lower noise figure and a lower $1/f$ noise[8]. It's not easy to achieve high voltage swing in 25% duty-cycle LO at the frequency of 2700 MHz. A divide-by-two circuit with high sensitivity and 25% duty-cycle local oscillator (LO) generator are also included in this work. Placing a 25% duty-cycle LO generator close to the passive mixer is necessary, for the stringent requirement in rise-time and fall-time at high frequencies.

3. Design of key blocks

This section describes each building block of the RF front-end: LNA, mixer, and LPF. All circuits described here operate from a 1.2-V power supply.

3.1. Variable gain LNA

For achieving high gain and low noise, the common source cascode LNA with inductive load is employed. The source degeneration is provided by the package parasitic inductance. In the front-end, the noise contribution of the TIA increases as the impedance at the mixer input decreases. Therefore, an LC tank is used at the LNA cascode output with switchable capacitors to adjust the tank resonant frequency according to the frequency of operation and provide high impedance at the mixer input. The analysis and design of a low noise amplifier in CMOS with 1.2 V supply has been reported by Sivonen[9]. However the performance of the RF front-end will degrade as the power

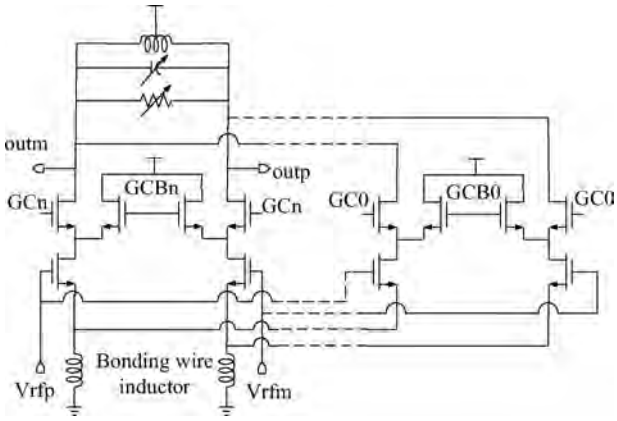

Fig. 2. Low noise amplifier with binary gain control.

of the input RF signal increases. The receiver maximum input level in LTE standard is –25 dBm. Therefore, gain control must be included in the RF front-end to improve the input dynamic range. In this paper, a novel gain control method is presented. As shown in Fig. 2, the transconductance stage is divided into five binary-weighted sections, including low noise common source NMOS with source degeneration in each transconductor. Each transconductance unit has its current either directed to the load or to the power supply by digitally steering all of current in the cascade device. Thus, the input impedance will not be affected by gain control. Moreover, with this architecture, the gain control could be linear and flexible. A gain control range of 36 dB is realized, with step of 6 dB. Q-tuning in RLC tank is designed to get fine gain control by reducing load resistance with the addition of a smaller shunt load.

3.2. Passive mixer with 25% duty-cycle LO and current-input low-pass filter

A current commutating passive mixer approach was selected because of its potential for low $1/f$ noise, exceptional large signal handling capability and very low intermodulation distortion. In this current-driven passive mixer topology as shown in Fig. 3, the mixer outputs are connected to the virtual grounds created by TIAs, the voltage swings at the mixer input and output are significantly reduced, resulting in improved linearity. A demodulator shows $1/f$ noise corner of 9–33 kHz, IIP3 of 4–10 dBm, and IIP2 better than +52 dBm with current commutating passive mixer architecture[10].

With 50% duty cycle LO, the current from LNA is split equally to both the I and Q mixers, and at any given instant one transistor is on in the both mixers. The current entering each of the mixers is effectively multiplied by a pulse train of 1, –1 repeating every LO cycle. This pulse train can be represented using Fourier series as

$$F_{50\%}(t) = \frac{4}{\pi}\left(\cos\omega_{\mathrm{LO}}t - \frac{1}{3}\cos 3\omega_{\mathrm{LO}}t + \frac{1}{5}\cos 5\omega_{\mathrm{LO}}t - \cdots\right). \tag{1}$$

Therefore, the magnitude of the desired difference frequency ($f_{\mathrm{RF}} - f_{\mathrm{LO}}$) current signal can be written as

$$I_{\mathrm{IF}} = \frac{2}{\pi}\cos\omega_{\mathrm{LO}}t \times \frac{I_{\mathrm{LNA}}}{2}, \tag{2}$$

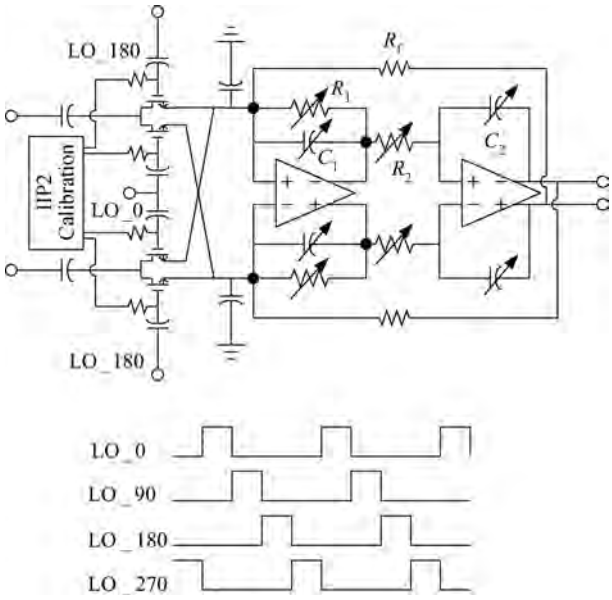

Fig. 3. Passive mixer with current-input LPF.

where the factor $\frac{2}{\pi}$, instead of $\frac{4}{\pi}$, accounts for the equal splitting of the signal current from the LNA into sum and difference frequencies after mixing with the LO, $I_{\rm LNA}$ is the output current of the LNA and $\frac{I_{\rm LNA}}{2}$ accounts for the equal splitting of this current in both the I and Q mixers.

Now with 25% duty cycle LO, only one of the four transistors is on at any given time, so the entire output current from the LNA flows through this transistor. This current is effectively multiplied by the pulse train 1, 0, –1, 0 repeating every LO cycle. This pulse train can be represented using Fourier series as

$$F_{25\%}(t) = \frac{2\sqrt{2}}{\pi}\left(\cos\omega_{\rm LO}t + \frac{1}{3}\cos 3\omega_{\rm LO}t - \frac{1}{5}\cos 5\omega_{\rm LO}t + \cdots\right). \quad (3)$$

Therefore, the magnitude of the desired difference frequency current signal can be written as

$$I_{\rm IF} = \frac{\sqrt{2}}{\pi}\cos\omega_{\rm LO}t \times I_{\rm LNA}. \quad (4)$$

Comparing the current signal of 50% duty cycle LO and 25% duty cycle LO, the 3 dB higher gain can theoretically be achieved when 25% duty cycle LO is used. This 3 dB improvement in gain will reduce the noise contribution of the filter.

Furthermore, with 25% duty cycle LO, the LNA current flows into only one of the mixers at any given time, and the IQ mixers are isolated in the time domain.

The linearity performance in the front-end depends on the linearity of transconductance stage, the linearity of the passive mixer stage and the transimpedance amplifier. The linearity of the current input filter depends strongly on the frequency offsets of the blocking signal from the carrier. In order to suppress the out-of-band interference and provide low impedance at the mixer output, the feedback structure of the current-input biquad is selected. Shunt capacitors at the mixer output nodes to ground are employed to filter out high frequency currents, including LO leakage and generated LO harmonics.

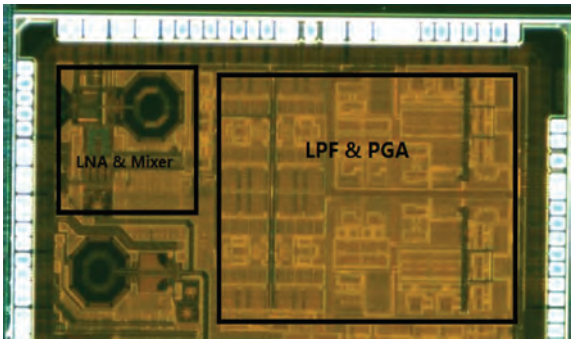

Fig. 4. Die photo of receiver.

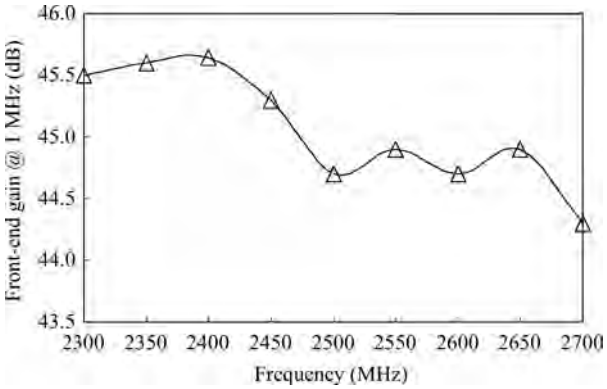

Fig. 5. Measured conversion gain versus LO frequency.

Non-idealities that affect IIP2 performance include device mismatch and layout asymmetry. IIP2 performance can vary with interferer offset and modulation bandwidth. To compensate for the mismatch between the quadrature switches, an on chip IIP2 calibration technique is realized. The IIP2 calibration is done with an automated closed loop routine by injecting calibration signals at the receiver input, setting the DAC offset at the mixer gates, based on an algorithm which is implemented in firmware, detecting the IM2 components in the baseband and repeating to minimize the second-order distortion component. With IIP2 calibration, the IM2 products arising from the modulated TX blocker reduce to be acceptable, and then the inter-stage SAW filter can be eliminated in the LTE receiver.

4. Measurement results

The receiver was fabricated in the 0.13 μm CMOS process as a part of LTE transceiver. Figure 4 shows the die microphotograph of receiver with PLL, including the PADs and ESD protection. The LNA and mixer area is about 0.5 mm by 0.7 mm. Two inductors are used, one in LNA and another in VCO.

The RF front-end voltage gain and noise figure with LO frequency are illustrated in Figs. 5 and 6, respectively. The conversion voltage gain is about 45 dB and the maximum gain is about 45.6 dB. The DSB noise figure is from 2.5 to 3.1 dB as shown in Fig. 6. Figures 7 and 8 show the conversion gain and double sideband noise figure at 2.5 GHz RF frequency. The flicker noise corner is lower than 16 kHz.

The input reflection coefficient S_{11} is better than –12 dB

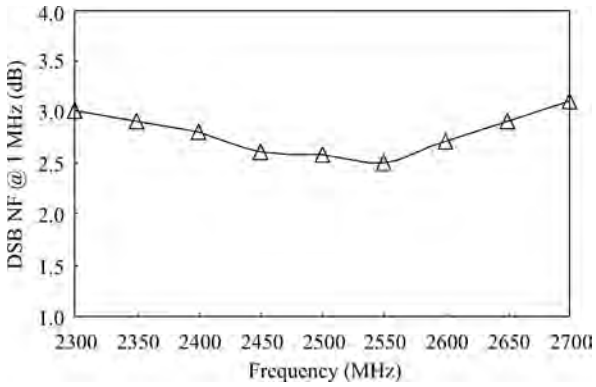

Fig. 6. Measured noise figure versus LO frequency.

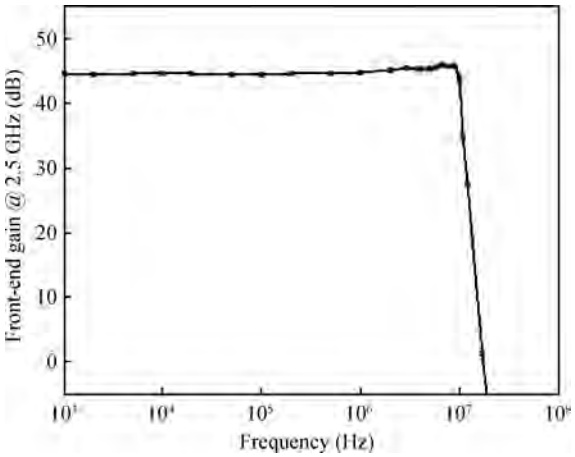

Fig. 7. Measured gain versus IF frequency.

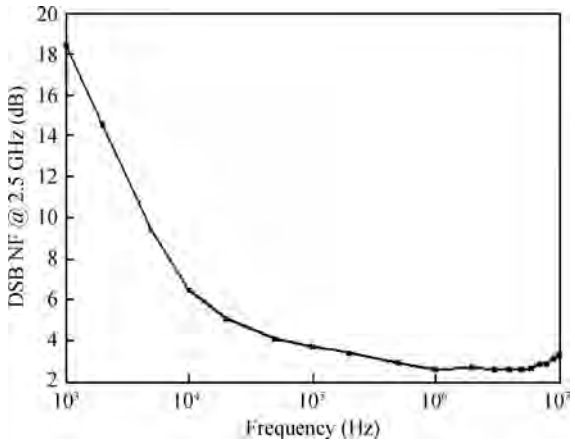

Fig. 8. Measured noise figure versus IF frequency.

from 2.3–2.7 GHz. RF front end gain control test results at the output frequency of 1MHz are shown in Fig. 9. The total gain control range is 36 dB with steps of about 6 dB. The highest gain is about 45.6 dB at 2.4 GHz RF frequency. Due to the parasitic capacitance, the gain rolls off at 2.7 GHz. The result shows a good consistency of gain step as RF frequency sweeps from 2.3 to 2.7 GHz.

The two-tone linearity of the front end at the highest gain has been measured. At the input of RF front end, two tones,

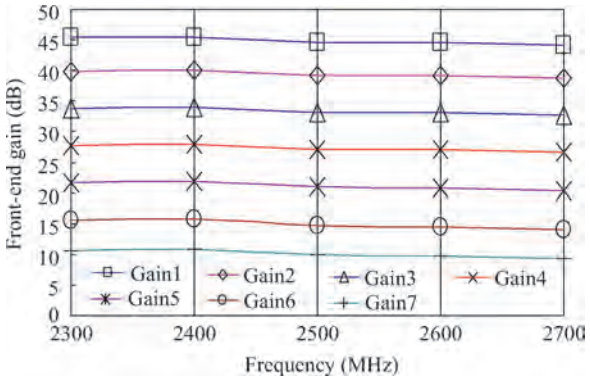

Fig. 9. Measured RF front-end gain control.

Table 1. Performance comparison with recent publications.

Parameter	This work	Ref. [6]	Ref. [9]
Process	0.13 μm CMOS	90 nm CMOS	0.13 μm CMOS
Frequency (GHz)	2.3–2.7	2–5.8	1.93–1.99
S_{11} (dB)	–12	–15	–12
Gain (dB)	45	44	50
DSB NF (dB)	2.7	4.5	3.9
IIP3 (dBm)	–7	–21	–9
IIP2 (dBm)	+60		+30
LO leakage at RF port (dBm)	–78		–94
Baseband bandwidth (MHz)	1.4/3/5/10/15/20		
Supply (V)	1.2	2.7	1.2
Current dissipation	40 (with divider)	31.5	87.5 (with VCO)

with −46 dBm at 17.5 MHz, and −46 dBm at 34 MHz, are applied. The IIP3 measured result is better than −7 dBm. The two-tone test was also conducted for the IIP2 measurement, with two TX tones of −30 dBm at 120 MHz and 121 MHz offset from the 2.65 GHz LO signal. Without calibration, the measured IIP2 of front-end is better than +30 dBm. After calibration, the IIP2 performance can be improved over +60 dBm.

Table 1 summarizes the performance of this prototype and shows the comparison of this work to other published broadband receiver front-ends.

5. Conclusion

A RF front-end for LTE direct conversion receiver has been fabricated in 0.13 μm CMOS process. Low noise transconductance amplifier provides a total gain control range of 36 dB with gain step of 6 dB. A current commutating with 25% duty-cycle LO has significant advantages in noise, intermodulation distortion and large signal handling capability. The current input lowpass filter biquad suppresses the interferer out-of-band, and improves the performance of the RF front-end. The RF front-end achieves 2.7 dB noise figure, 45 dB conversion gain, better than –7 dBm IIP3 and +60 dBm IIP2. From 1.2 V supply, the RF front-end consumes 40 mA with divider.

References

[1] Lee T. The design of CMOS radio-frequency integrated circuits. Cambridge, UK: Cambridge University Press, 1998

[2] Chen P W, Lin T Y, Ke L W, et al. A 0.13 μm CMOS quad-band GSM/GPRS/EDGE RF transceiver using a low-noise fractional-N frequency synthesizer and direct-conversion architecture. IEEE J Solid-State Circuits, 2009, 44(5): 1454

[3] Kim N, Larson L E, Aparin V. A highly linear SAW-less CMOS receiver using a mixer with embedded Tx filtering for CDMA. IEEE J Solid-State Circuits, 2009, 44(8): 2126

[4] Moon H, Han J, Choi S I, et al. A 0.13-μm CMOS multi-band WCDMA/HSDPA receiver adopting silicon area reducing techniques. IEEE Radio Frequency Integrated Circuits (RFIC) Symp Dig Papers, 2009: 17

[5] Rodrigures S, Rusu A, Ismail M. WiMAX/LTE receiver front-end in 90 nm CMOS. IEEE International Symposium on Circuit and System (ISCAS), 2009: 1036

[6] Zhou S, Chang M C F. A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver. IEEE J Solid-State Circuits, 2005, 40(5): 1084

[7] Zhan J H C, Carlton B R, Taylor S S. A broadband low-cost direct-conversion receiver front-end in 90 nm CMOS. IEEE J Solid-State Circuits, 2008, 43(5): 1132

[8] Kaczman D, Shah M, Alam M, et al. A single-chip 10-band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with DigRF 3G interface and +90 dBm IIP2. IEEE J Solid-State Circuits, 2009, 44(3): 718

[9] Sivonen P, Tervaluoto J, Mikkola N, et al. A 1.2-V RF front-end with on-chip VCO for PCS 1900 direct conversion receiver in 0.13-μm CMOS. IEEE J Solid-State Circuits, 2006, 41(2): 384

[10] Poobuapheun N, Chen W H, Boos Z, et al. A 1.5-V 0.7–2.5-GHz CMOS quadrature demodulator for multiband direct-conversion receivers. IEEE J Solid-State Circuits, 2007, 42(8): 1669