Digital post-calibration of a 5-bit 1.25 GS/s flash ADC*

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Abstract: We report a high-speed flash analog to digital converter (ADC) linearization technique employing the inverse Volterra model and digital post processing. First, a 1.25 GS/s 5-bit flash ADC is designed using a 0.18 μm CMOS, and the signal is quantized by a distributed track-and-hold circuit. Second, based on the Volterra series, a proposed digital post-calibration model is introduced. Then, the model is applied to estimate and compensate the nonlinearity of the high-speed flash ADC. Simulation results indicate that the distortion is reduced effectively. Specifically, the ADC achieves gains of 4.83 effective bits for a 117.1 MHz frequency input and 4.74 effective bits for a Nyquist input at 1.25 GS/s.

Key words: flash ADC; Volterra series; digital post-calibration
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1. Introduction

Nowadays, digital signal processing techniques are rapidly developing. As a result, requirements on speed and high accuracy of systems are increasing, especially in fields of high resolution image and video processing, wireless communication, etc. As links between analog and digital signal processing systems, analog to digital converters (ADCs) are aiming at increasing the resolution and the dynamic range[1].

In general, there are trade-offs in noise, speed, consumption, and non-linearity of ADCs, and high precision requires that both noise and distortion of the circuit are well suppressed[2]. For Flash ADCs, higher speeds can be achieved compared with other structures, but the area and power consumption grow exponentially with resolution, which means that implementing high resolution flash ADCs is a challenging problem[3]. To solve this problem, a digital calibration technique has been proposed, which is based on the special circuit structure of ADCs and the various factors causing nonlinearity. By employing calibration to compensate for nonlinearity of ADCs, high accuracy can be achieved[4].

In this paper, a novel hybrid (time and frequency domains) digital post-calibration technique based on the Volterra series is proposed. By solving the n-th order of Volterra kernels, the output signal of a high-speed Flash ADC is calibrated. Compared with signals without calibration, distortion is reduced effectively. Specifically, the SNDR and SFDR are improved from 26.67 and 32.44 to 30.32 dB and 40.74 dB respectively for a Nyquist input at 1.25 GS/s.

2. Digital post-calibration

Generally, there are two kinds of digital calibration technique: pre-calibration and post-calibration.

For the pre-calibration technique, sometimes a separate cycle is required, and the error is then derived from the output signal by comparison. Although the speed of error extraction for pre-calibration is very fast, the additional separate calibration cycle leads to an undesirable pause during conversion[5]. For some systems, this is unacceptable.

On the other hand, the post-calibration technique uses the correlation between the input and the output codes of pseudo-random signals to extract the error parameter, and then subtracted the error from the output to acquire the calibrated output. To avoid the correlation between the correction sequence and the analog input sequence, a long pseudo-random sequence is applied. Although the post-correction takes more time because of the processing effect, it supports simultaneous calibration and conversion, which cannot be achieved by pre-calibration (Fig. 1). As discussed above, this paper considers the digital post-calibration method for the linearization of ADCs.

To calibrate the nonlinearity of ADCs, the analysis of its nonlinear characteristics should be carried out first by modeling. The most well-known problem of ADCs compared with other non-linear systems is the "memory effect", which is caused by the incomplete charge and discharge of capacitors and other effects which impact on the next state during conversion[6].

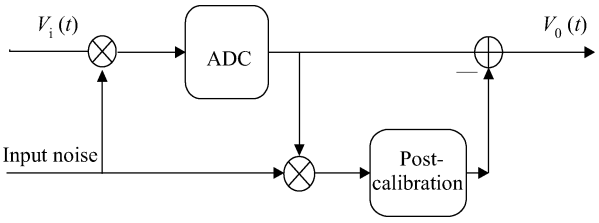

Fig. 1. Digital post-calibration theory.

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3. Volterra series calibration model

Previously, four methods have been employed based on the nonlinear model of ADCs: the Power series, the exponential series, the Taylor series, and the Volterra series[3]. The former three are not effective for broadband systems because they assume that the system is memoryless and thereby ignore the frequency dependence.

On the other hand, the Volterra series, which could be considered as a "Taylor series with memory"[4], does account for the frequency dependence. Considering the Volterra series, a general-purpose approach for modeling and linearizing a nonlinear system is described in this paper. The Volterra series is normally employed in either the time domain or the frequency domain and each way has pros and cons. Since the processing is relatively simple for small or medium-sized non-linear circuits with only the first few orders, the Volterra series can model the nonlinear system accurately. Therefore, by considering the structure of ADCs as well as their functional properties and nonlinear effects, the Volterra series is used for non-linear digital post-calibration of ADCs.

The most important part of the Volterra series method is to acquire the n-th order kernels of each stage[5, 6]. Once the transfer function of each stage is derived, the nonlinear system can be transformed into a linear system.

First, the input signal can be represented as:

$$x(t) = \sum_{\substack{i=-m \\ m\neq 0}}^{m} a_i \exp(\mathrm{j}w_i t). \tag{1}$$

For the n-th order, the output signal can be expressed as:

$$y_n(t) = \sum_{i_1=-m}^{m} \cdots \sum_{i_n=-m}^{m} a_{i_1} \cdots a_{i_n} \times H_n(\mathrm{j}w_{i_1}, \cdots, \mathrm{j}w_{i_n}) \times \exp\left(\mathrm{j}\sum_{k=1}^{n} w_{ik} t\right), \tag{2}$$

where $H_n(\mathrm{j}w_{i_1}, \cdots, \mathrm{j}w_{i_n})$ is the n-th-order frequency domain Volterra kernel:

$$H_n(\mathrm{j}w_{i_1}, \cdots, \mathrm{j}w_{i_n}) = \frac{Y_n(\mathrm{j}\sum_{k=1}^{n} w_{i_k})}{\prod_{l=1}^{n} a_{i_l}}. \tag{3}$$

As Equation (3) shows, to derive the n-th order Volterra kernel, the key issue is the separation of the output variables. For the actual measurement process, a sweep frequency method is used for the measurement of the output signal. The sweep method involves step scanning the input signal frequencies from DC to the sampling frequency, and then capturing the output signal as the required data[1]. To acquire the complete Volterra kernels, the interpolation of the measured frequencies is needed, and only the interpolated Volterra kernels are applied in ADC modeling:

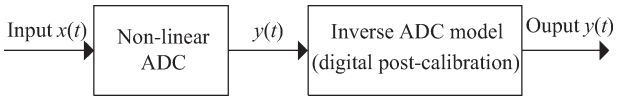

Fig. 2. Digital post-calibration design.

$$\begin{aligned} y(t) = & \int_{-\infty}^{\infty} h_1(\tau)x(t-\tau)\mathrm{d}\tau \\ & + \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h_2(\tau_1,\tau_2)x(t-\tau_1)x(t-\tau_2)\mathrm{d}\tau_1\tau_2 \\ & + \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h_3(\tau_1,\tau_2,\tau_3) \\ & \times x(t-\tau_1)x(t-\tau_2)x(t-\tau_3)\mathrm{d}\tau_1\tau_2\tau_3. \end{aligned} \tag{4}$$

After constructing the ADC module, we can develop the inverse module and apply the post calibration.

As Figure 2 shows, based on the Volterra seires, an inverse Volterra module can be employed to execute the post calibration to get the distortion-compensated output signal $y(t)$.

4. Flash ADC circuit

This paper focuses on the calibration of a 5 bit flash ADC (as shown in Fig. 3) to verify the proposed model of our digital post-calibration technique.

4.1. Distributed track-and-hold circuit

Figure 4 presents a schematic diagram of the proposed distributed track-and-hold circuit. When two switches are on, it works as a pre-amplifier. The output of the preamp is

$$\begin{aligned} V_{\mathrm{out}+} - V_{\mathrm{out}-} &= A_{\mathrm{d}}[(V_{\mathrm{in}+} - V_{\mathrm{ref}+}) - (V_{\mathrm{in}-} - V_{\mathrm{ref}-})] \\ &= A_{\mathrm{d}}[(V_{\mathrm{in}+} - V_{\mathrm{in}-}) - (V_{\mathrm{ref}+} - V_{\mathrm{ref}-})], \end{aligned} \tag{5}$$

where A_{d} is the gain of the preamp, and $V_{\mathrm{in}+} - V_{\mathrm{in}-}$ and $V_{\mathrm{ref}+} - V_{\mathrm{ref}-}$ are the differential input signal and reference voltage, respectively. When the circuit is operating in "hold" mode, it only determines whether the input signal is higher or lower than the reference voltage at the end of the previous tracking period, and keeps the charges of the parasitic capacitors associated with the output nodes being held correctly. Therefore, the linear requirements employing the distributed track-and-hold circuit are relaxed compared with conventional pre-amplifiers for flash ADCs.

4.2. Comparator

The design of a high-speed comparator has been a bottleneck in ADC design. In this paper, the structure of the pre-amplification latched comparator is considered, which is shown in Fig. 5. It achieves both high accuracy and large input bandwidth.

The latch circuit of the comparator is shown in Fig. 6. The function of this circuit is to provide a sufficient gain to pull the pre-amp output up to VDD or GND. For that purpose, logic

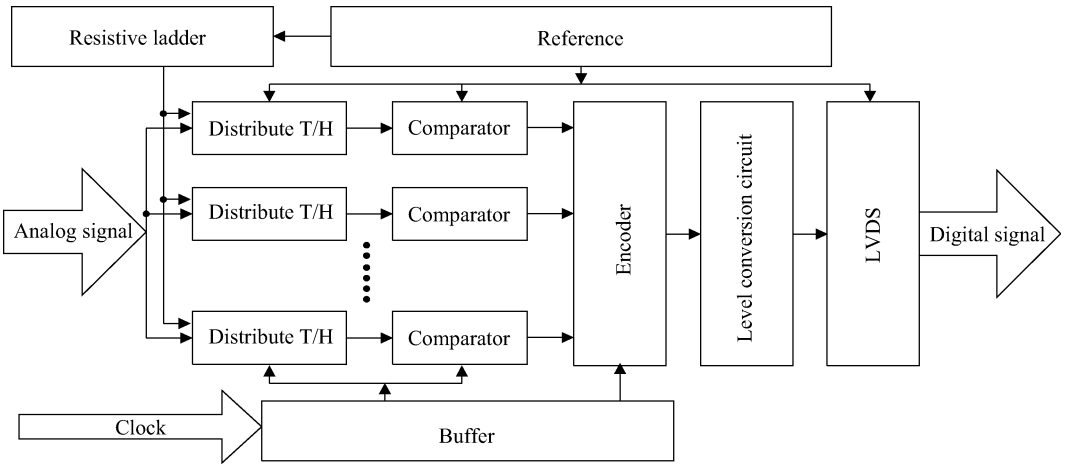

Fig. 3. System diagram of a flash ADC.

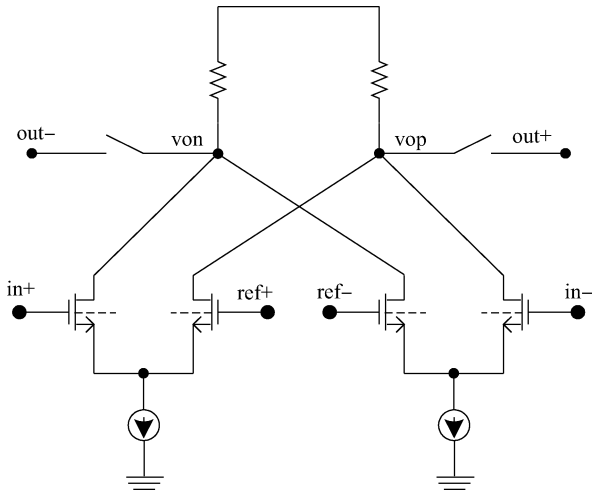

Fig. 4. Schematic of distributed track-and-hold.

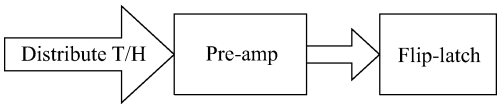

Fig. 5. Comparator circuit.

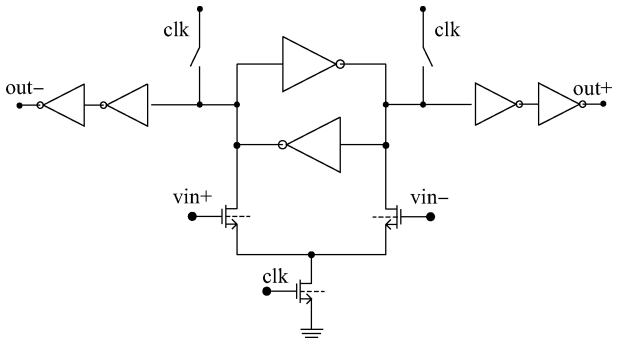

Fig. 6. Latch circuit.

gates are required to convert the signal, and then the output buffer of the latch is made from two inverters, which increase the drive capacity of the latch.

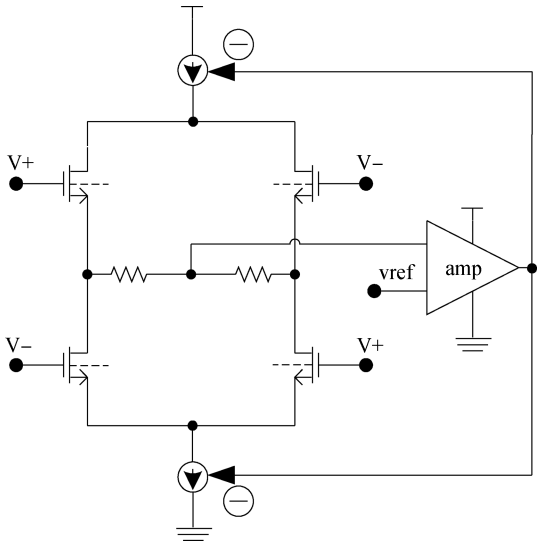

Fig. 7. LVDS interface circuit.

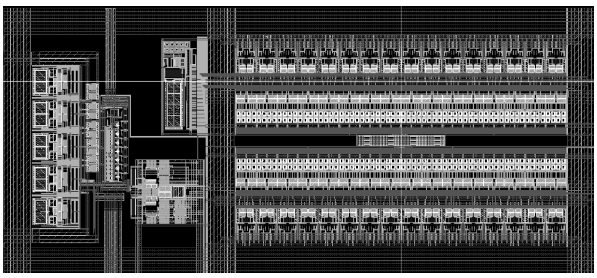

Fig. 8. Layout of the proposed ADC.

4.3. Output interface circuit

When the frequency is high it is difficult to accomplish the test or get the output of a large swing signal due to the impact of the pad, the on-chip parasitic, and the parasitic parameters of the test equipment. Therefore, this design uses an LVDS output standard. At the chip output, full-swing digital signals are converted to LVDS signals through an LVDS circuit. The LVDS

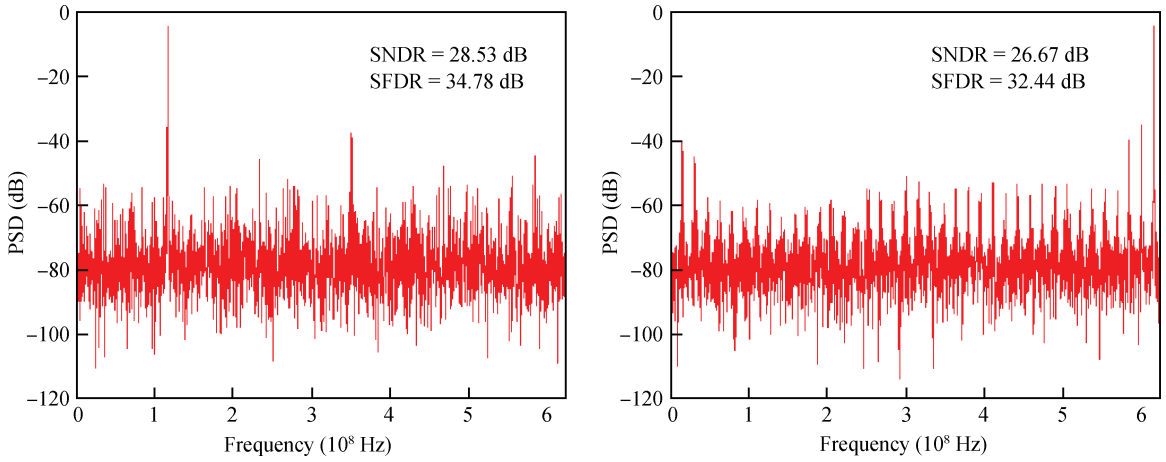

Fig. 9. The original PSD simulation result.

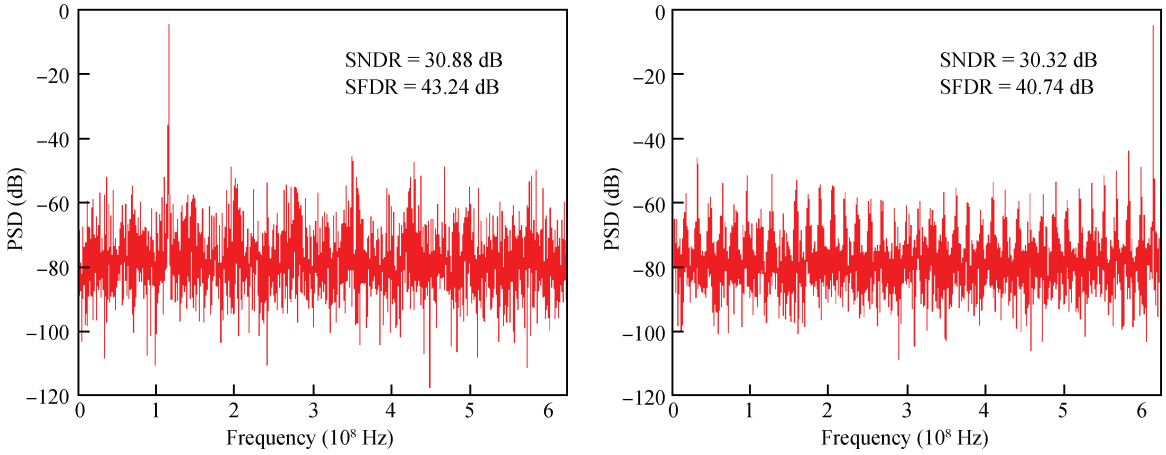

Fig. 10. The PSD simulation result after calibration.

Table 1. Comparision of high-speed flash ADCs.

Parameter	This work	Ref. [7]	Ref. [8]
Technology (nm)	180	180	180
Resolution (bit)	5	6	4
ENOB (bit) @ f_s, f_{in}	4.84 @ 1.25 GS/s, 117.1 MHz 4.74 @ 1.25 G/s, 611.1 MHz	5.78 @ 2 GS/s, 1.22 MHz	3.47 @ 3.4 GS/s, 800 MHz
Supply (V)	1.8	1.8	1.8
Power (mW)	230	570	633
ERBW (MHz)	Over 600	Less than 200	—
Fom	6.88	—	16.80

interface circuit is shown in Fig. 7.

The amplifier in Fig. 7 realizes the common-mode negative feedback function, and it can also stabilize the common-mode output of the LVDS module to 1.25 V. Because the peak output value of the LVDS module could reach 1.4 V or higher, it increases the difficulty of the design for the 1.8 V supply voltage. Therefore, this design applies the 3.3 V supply voltage, and it needs a level conversion circuit to convert the CMOS output of the encoder from 0–1.8 V to 0–3.3 V.

5. Simulation result

The proposed flash ADC has been designed with a 0.18 μm 1-poly 6-metal CMOS technology. Figure 8 shows the layout of the proposed ADC. The active layout area is 1.48 mm^2. The ADC consumes 230 mW from a 1.8 V supply when the clock frequency is 1.25 GHz.

Let the frequency of the single tone input signal be 117.1 MHz and the Nyquist frequency be 1.25 GHz clock frequency. The measured and synthetic data of the output signal in the frequency domain are displayed in Fig. 9.

Figure 10 displays the compensated data by applying the proposed inverse ADC module. The results show that distortion is reduced effectively. Specifically, the SNDR and SFDR are improved from 28.53 and 34.78 to 30.88 dB and 43.24 dB respectively when the input frequency is 117.1 MHz. When

the input is increased to the Nyquist frequency, the SNDR and SFDR are improved from 26.67 and 30.32 to 32.44 dB and 40.74 dB respectively. The results show that the ADC achieves gains of 4.83 effective bits for the 117.1 MHz input and 4.74 effective bits for the Nyquist input at 1.25 GS/s.

We note a figure-of-merit of 6.88 pJ per conversion for the flash ADC. And this ADC has an input capacitance of about 750 fF. If we assume that a degradation of 1 bit of effective resolution from ideal is allowable, the allowable clock jitter and skew is about 14.0 ps. Table 1 compares this work with other recently published single channel flash ADCs having a sampling rate of more than 1 GS/s.

6. Conclusion

In this paper, a high-speed flash ADC is designed and a novel technique for digital post processing founded on the Volterra series is proposed for the linearization of ADCs. This paper provides three contributions. First, the flash ADC is efficiently designed. Second, an inverse module with a post-calibration technique based on the Volterra series is constructed. Finally, the proposed digital post-calibration module compensates effectively the distortion caused by the ADCs, which is supported by experimental results.

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