Analysis and design of a high-linearity receiver RF front-end with an improved 25%-duty-cycle LO generator for WCDMA/GSM applications*

Hu Song(胡嵩), Li Weinan(李伟男), Huang Yumei(黄煜梅)†, and Hong Zhiliang(洪志良)

State Key Laboratory of ASIC and System, Fudan University, Shanghai 201203, China

Abstract: A fully integrated receiver RF front-end that meets WCDMA/GSM system requirements is presented. It supports SAW-less operation for WCDMA. To improve the linearity in terms of both IP3 and IP2, the RF front-end is comprised of multiple-gated LNAs with capacitive desensitization, current-mode passive mixers with the proposed IP2 calibration circuit and reconfigurable Tow-Thomas-like biquad TIAs. A new power-saving multi-mode divider with low phase noise is proposed to provide the 4-phase 25%-duty-cycle LO. In addition, a constant-g_m biasing with an on-chip resistor is adopted to make the conversion gain invulnerable to the process and temperature variations of the transimpedance. This RF front-end is integrated in a receiver with an on-chip frequency synthesizer in 0.13 μm CMOS. The measurement results show that owing to this high-linearity RF front-end, the receiver achieves -6 dBm IIP3 and better than $+60$ dBm IIP2 for all modes and bands.

Key words: receiver; multi-mode; multi-band; SAW-less; IP2 calibration; 25% duty-cycle

DOI: 10.1088/1674-4926/33/2/025007 **EEACC:** 1205

1. Introduction

With the demand for lower cost cellular handsets, multi-mode and multi-band receivers are dominating the current market. Direct conversion receivers (DCRs) have gained wide attention. Compared with their heterodyne counterparts, the DCRs enable more hardware sharing, lower power consumption and fewer external components[1].

However, conventionally, an off-chip surface acoustic wave (SAW) filter is needed in the WCDMA DCR. For the frequency division duplexing (FDD) based standard WCDMA, the receiver and transmitter work simultaneously. Since the duplexer can only provide finite isolation, the transmitting signals can leak into the receiver and appear as a strong blocker. Due to the modest quality factor (Q) of on-chip passive components, the TX leakage is conventionally attenuated by the off-chip SAW filter placed between the low noise amplifier (LNA) and the down-converter in the WCDMA receiver RF front-end, as shown in Fig. 1. This interstage SAW filter degrades the receiver sensitivity due to its inevitable insertion loss. In addition, this SAW filter makes the chip pins complex, and it is expensive and bulky. Thus it is desirable to remove this SAW filter.

Unfortunately, the elimination of the interstage SAW filter imposes more stringent linearity requirements with regards to both the third-order intercept point (IP3) and the second-order intercept point (IP2) for the receiver RF front-end design[2]. The transmitter leakage gives rise to intermodulation distortions through two mechanisms. One mechanism is the third-order nonlinearity due to the cross-modulation of the TX leakage and other blockers; and the other mechanism is the second-order nonlinearity due to the TX leakage self-mixing. These effects are illustrated in Fig. 2.

This paper presents a WCDMA/GSM RF front-end supporting SAW-less operation for WCDMA[3]. In detail, this paper discusses the system architecture, circuit implementation, and circuit parameter optimization of the receiver RF front-end.

2. Architecture design

The architecture of the multi-mode multi-band receiver RF front-end is shown in Fig. 3. A single-ended version is shown for clarity, and all the circuits are differential in the real application. This receiver RF front-end supports WCDMA band I, GSM high band (DCS 1800/PCS 1900) and GSM low band (GSM 850/GSM 900).

Each of these three modes has a set of individually optimized low noise amplifier and in-phase/quadrature (I/Q) mixer. Reconfigurable transimpedance amplifiers (TIAs) are shared for different modes. The LNA, in fact, acts as a transconductance amplifier and converts the input voltage into current, which directly feeds the current-mode passive mixer. The down-converted mixer output current is subsequently converted to the output voltage using a Tow-Thomas-like biquad TIA, which also creates the complex poles of the baseband low-pass filter.

For some conventional designs, such as Ref. [4], the LNA amplifies the signal in the voltage domain and an intermediate transconductance stage is inserted between the LNA and I/Q mixer. This architecture suffers two drawbacks. First, the extra transconductance stage will hurt the receiver linearity due to voltage-to-current and current-to-voltage conversions. Second, the blocker will experience voltage amplification before filtering. While for the architecture in Fig. 3, there is voltage gain only after filtering.

* Project supported by the National Science and Technology Major Project of China (No. 2009ZX01031-003-002) and the National High Technology Research and Development Program of China (No. 2009AA011605).

† Corresponding author. Email: yumeihuang@fudan.edu.cn

Received 8 August 2011, revised manuscript received 8 September 2011

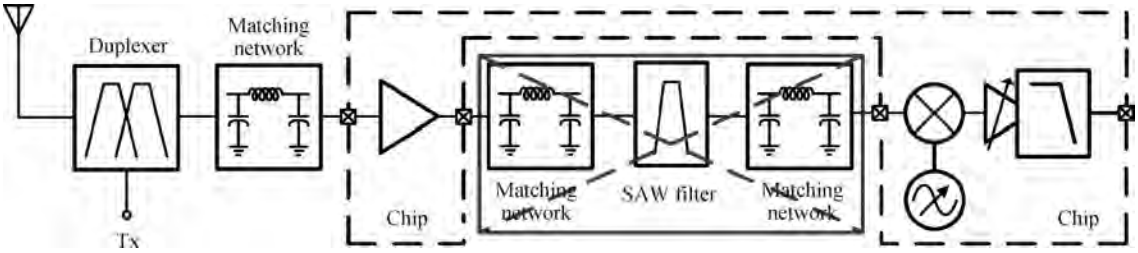

Fig. 1. Interstage SAW filter used in the conventional WCDMA receiver.

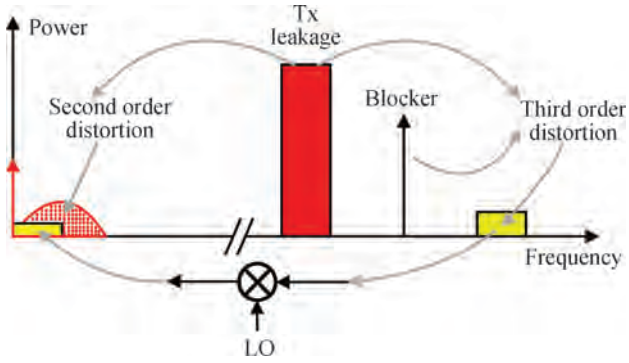

Fig. 2. Effects of the transmitter leakage on receiver.

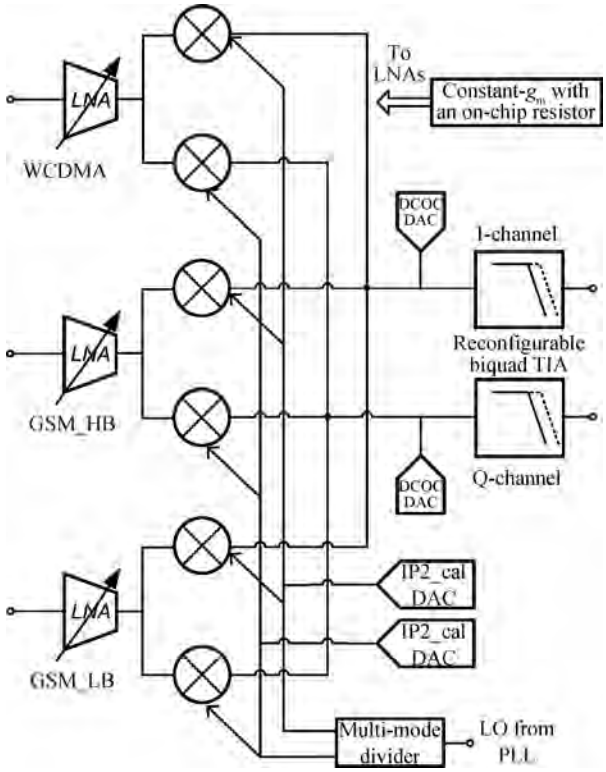

Fig. 3. Block diagram of the receiver RF front-end.

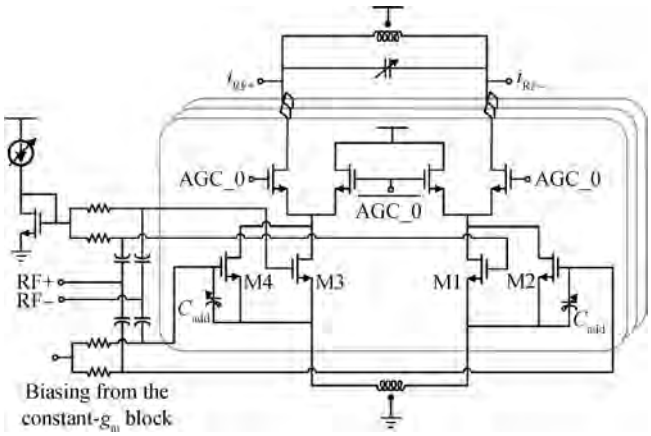

Fig. 4. MGTR LNA with capacitive desensitization.

3. Circuit analysis and design

3.1. High-linearity LNA

A stringent linearity requirement is set for the LNA when the SAW filter is eliminated. The cascode LNA, linearized by the inductive source degeneration, cannot meet the requirement. An LNA with the widely used multiple-gated transistors (MGTRs) can effectively reduce the third-order nonlinearity of g_m[5]. However, the pure MGTR LNA suffers from the "second-order interaction" effect, which limits the upmost achievable linearity[6]. There are some techniques available in the literatures for improving the LNA linearity further in SAW-less receivers[6−9]. However, for the modified derivative superposition (MDS) method presented in Refs. [6, 7], the requirement of a cooperating design of the second-order and third-order distortion makes the effective cancellation range narrow. For the active post-distortion (APD) method used in Refs. [8, 9], the distortion cancellation is done at the output of the LNA, which is sensitive to the impedance fluctuation at the passive mixer input.

This work adopts an MGTR LNA with capacitive desensitization[10], as shown in Fig. 4. Like the conventional MGTR LNA, the auxiliary transistors M2 and M4 are properly sized and biased in the weak inversion region to counteract the transconductance third-order nonlinearity of the main transistors M1 and M3 biased in the strong inversion region. Unlike the conventional MGTR LNA, the extra gate–source capacitor C_{add} is introduced.

This additional capacitor brings two benefits. First, the second-order interaction problem in the conventional MGTR LNA can be alleviated[10]. Since the gate-source impedance is lowered by the additional capacitor, the voltage of the feedback second-order harmonic is reduced. As a result, higher linearity can be obtained when the MGTR is combined with this additional capacitor. Second, this extra gate-source capacitor can decouple the input matching issue from the input transistor size

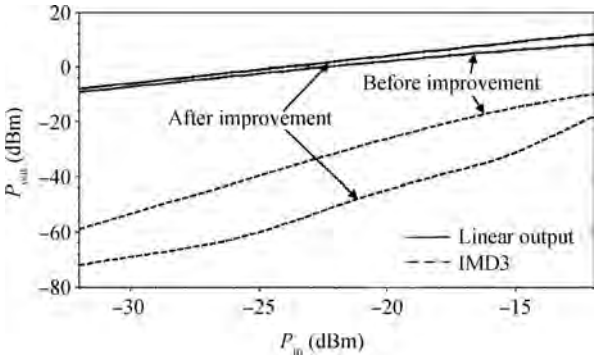

Fig. 5. Linearity comparison before and after improvement.

to some extent. For a common-source LNA, when the Q of the input network is higher, the contribution of the drain thermal noise to the overall noise is decreased, while the contribution of the gate-induced noise to the overall noise is elevated[11]. There is an optimum value of this Q for the low noise design. Meanwhile, it is indicated in Ref. [6] that a transistor biased in the weak inversion region generates more gate-induced noise than a counterpart biased in the strong inversion region. This makes the optimization of this Q value more important in a MGTR LNA. This Q can be expressed as Eq. (1), where R_S is the source impedance; L_S is the source degeneration inductance; and the total gate-source capacitance $C_{gs,TOT}$ is the sum of the intrinsic gate-source capacitance C_{gs0} and C_{add}. Bringing in another design freedom, the extra gate–source capacitor facilitates the noise optimization in an MGTR LNA. This is especially helpful in a low-power MGTR LNA, when the size of the input transistor is relatively small.

$$Q = \frac{1}{\omega_0 R_S C_{gs,TOT} + g_m \omega_0 L_S}. \quad (1)$$

To deal with the process and temperature variations, the additional gate–source capacitor is realized as a three-bit digital-controlled capacitor array and the biasing of the auxiliary transistors is made tunable finely by the DAC.

Figure 5 compares the capacitively desensitized MGTR LNA with the cascode LNA linearized by the inductive source degeneration. The noise figure (NF) difference of these two circuits is less than 0.1 dB after the quality factors of their input networks are optimized. For the MGTR LNA with capacitive desensitization, the gain is lifted by 1.5 dB and the third-order intermodulation distortion (IMD3) is maximally suppressed by 20 dB. With the increasing of the input signal power, this IMD3 improvement narrows due to the contribution of the high order harmonics on the IMD3.

The LNA is loaded by an LC tank, which is tuned to resonate with the parasitic capacitors at the LNA output node to overcome the well-known TIA noise amplification issue[12]. The parameters of the LC tank are decided after a joint optimization with the parasitic capacitance, the coupling capacitance between the LNA and mixer, the ON resistance of the switches and the up-converted baseband impedance. This will be discussed in detail in Section 4.

To realize the gain control, the cascode transistors are divided into three binary-weighted sections, as shown in Fig. 4.

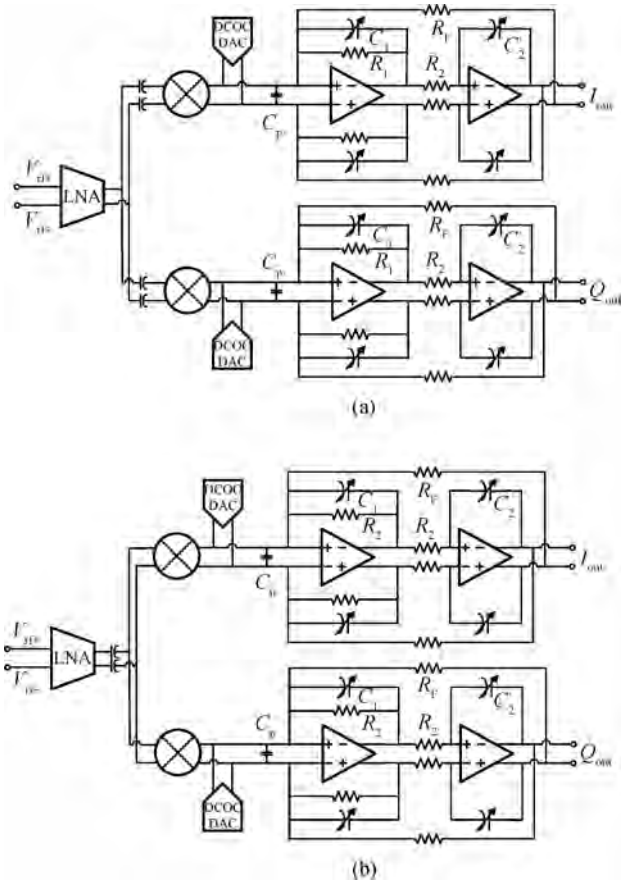

Fig. 6. Discussion on the coupling capacitors between the LNA and mixer.

For each section, the drain current of the transconductor transistor can be steered either to the load or the power rail by controlling the cascoded devices. This gain control method has little effect on the input matching issue since the current flowing through the transconductor transistors keeps constant for different gains.

3.2. Passive mixer with IP2 calibration

As mentioned in Section 2, the output current of the LNA directly feeds the current-mode passive mixer. The current-mode passive mixer is chosen not only for its well-known better flicker noise and linearity over the active Gilbert mixer in low supply voltage applications, but also for its impedance transformation property, which has been widely utilized to construct a built-in high-Q band-pass filter (BPF) suppressing the transmitter leakage and other blockers[13, 14]. Since passive mixers driven by the 50%-duty-cycle clocks suffer the image issue[13, 14], the switches are clocked by the 4-phase 25%-duty-cycle clocks[2, 3, 14−16]. Along with providing isolation between the I/Q channels, this increases the conversion gain, lowers the $1/f$ noise, and improves linearity.

The current mode passive mixers are coupled to the LNA using capacitors for both the I and Q channels. In this way, the DC voltage of these two stages can be set independently. In addition, these coupling capacitors block the low-frequency second-order nonlinearity components and the low-frequency noise from the LNA.

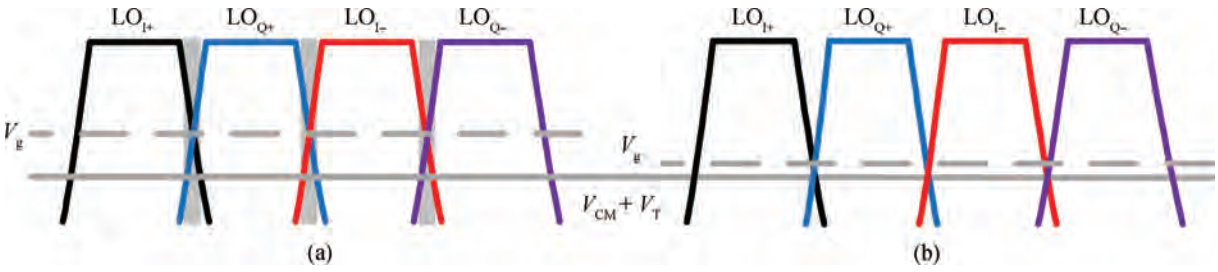

Fig. 7. Tuning of the switch's gate biasing.

Figure 6 depicts two possible configuration choices of the coupling capacitors. A single-mode single-band view is given. For passive mixers driven by the 50% duty-cycle LO, the topology of Fig. 6(a) is necessary to avoid the flicker noise deterioration due to the DC current circulating through the switches between the I/Q channels. This current is introduced by the random offsets of the I/Q TIAs. However, for passive mixers driven by the 4-phase 25% duty-cycle LO, only one channel is ON at any moment ideally. As a result, the topology of Fig. 6(b), which saves two capacitors, is acceptable.

However, the non-ideal clock has a finite slope. The rise and fall times of the clock make it possible that one switch in the I channel and another one in the Q channel are simultaneously ON even for the 4-phase 25% duty-cycle LO case. It is illustrated in Fig. 7(a), where V_g, V_{CM} and V_T represent the gate biasing of the switches, the common-mode input level of the TIA and the threshold voltage value of the switches, respectively. This not only brings about the aforementioned $1/f$ noise exacerbation of the passive mixer, but also amplifies the noise contribution from the TIA. The latter effect results from the decreased impedance seen through the baseband side of the mixer[12] due to the loading of the other channel. Besides, the simultaneous ON state of the I/Q channels makes the impedance seen by the LNA fluctuation. When both channels are ON, this impedance is one half of the value when only one channel is ON. This worsens the linearity, and makes the circuit parameter optimization hard to be implement. To overcome this problem, V_g is made tunable by the DAC, as illustrated in Fig. 7. It should be noted that if there exists an instant when both channels are turned off, a more serious impedance change would occur. So, the gate biasing of the switches should finally be tuned to a value, which ensures at least one channel ON at any moment, while minimizes the time when both channels are ON, as shown in Fig. 7(b).

As mentioned in Section 1, WCDMA SAW-less DCRs claim high linearity in terms of IP2. This imposes a stringent IP2 requirement on the mixer[2], although the second-order nonlinearity products generated inside the LNA have been blocked by the coupling capacitors between the LNA and mixer. Some literatures perform the IP2 calibration by injecting current at the RF side of the passive mixer[17]. However, this method would bring about extra DC offset and noise. An alternative IP2 calibration method is proposed in Ref. [2]. Since the mechanisms of the second-order intermodulation distortion (IMD2) can be modeled as the mismatches with an offset voltage of the DC biasing at the switch gates[18, 19], the IP2 calibration is realized by adjusting these DC bias points dedicatedly and the IMD2 is thus counteracted[2].

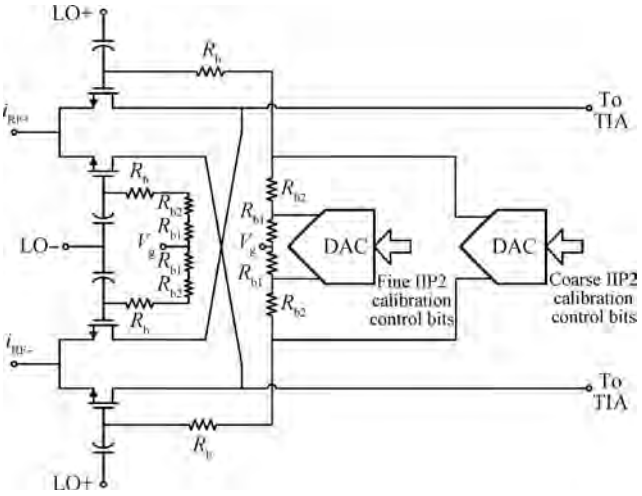

Fig. 8. Passive mixer with the proposed IP2 calibration circuit.

An improved IP2 calibration circuit is proposed in this work, as shown in Fig. 8. Compared with the conventional method in Ref. [2], the coarse and fine calibration is realized by letting the calibration current flow through the resistors with different values, as $2R_{b1}$ and $2(R_{b1} + R_{b2})$ shown in Fig. 8. This proposed method ensures the calibration range and precision simultaneously with a loose requirement on the calibration DAC. The 6-bit binary-weighted calibration DAC has a precision of 1 μA. R_{b1} and R_{b2} are 60 Ω and 170 Ω, respectively. The I and Q channels are made adjustable independently to make the calibration scheme more flexible[4].

3.3. Reconfigurable Tow-Thomas-like biquad TIA

The down-converted mixer output current directly feeds the reconfigurable biquad TIA, which performs the I/V conversion and also realizes a pair of complex poles, as shown in Fig. 6. The biquad TIA outperforms the commonly used first-order TIA[4, 7, 9, 13−15] in the following three aspects. First, there is less in-band gain loss due to the complex response. Second, it is demonstrated in Ref. [20] that for the biquad configuration, the second stage in the loop enhances the overall loop gain compared with the single stage active-RC filter sections. As a result, the nonlinearity caused by operational amplifiers is suppressed more and better linearity is achieved. Last but not least, for the biquad configuration, the blockers can be suppressed more effectively before the first high voltage swing node at the TIA output.

The biquad TIA shown in Fig. 6 is similar to the Tow-

Thomas biquad topology. For better linearity, the input resistor in the Tow-Thomas biquad is removed to provide a virtue ground at the TIA input[2]. This Tow-Thomas-like biquad topology is chosen for its parasitic insensitive property and ease of corner tuning. The transfer function can be expressed as

$$T(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}, \tag{2}$$

where the cut-off frequency ω_0 and quality factor Q are

$$\omega_0 = \sqrt{\frac{1}{R_2 R_F C_1 C_2}}, \tag{3}$$

$$Q = R_1\sqrt{\frac{C_1}{R_2 R_F C_2}}. \tag{4}$$

So, when ω_0 is fixed, R_1 can be adjusted to tune Q while keeping ω_0 unchanged.

The bandwidth of the TIA is made reconfigurable between the wideband WCDMA and narrowband GSM settings. This is realized by tuning the values of the capacitors in TIA, as shown in Fig. 6. The parameters of the operational amplifiers in TIA, such as the gain bandwidth, are also made to be reconfigurable to save power when the narrowband applications are required.

A very low impedance in the desired signal frequency band is created at the TIA input by the operational amplifier feedback loop. However, due to the bandwidth limitation of amplifiers, the TIA input impedance increases as the frequency gets high. For better linearity, the input impedance at the frequency where the residual blockers and feedthrough clock lie in, should also be low. So, the capacitors C_p are added at the input of the TIA to reduce this impedance at high frequency, as shown in Fig. 6.

DC offset calibration DACs are added at the input of the biquad TIAs to cancel out the DC offsets caused by various sources including the LO leakage.

3.4. High-performance 25%-duty-cycle LO generator

Conventionally, to generate the 4-phase 25%-duty-cycle clocks, the quadrature 50%-duty-cycle signals at the desired LO frequency are got firstly by divide-by-2 dividers, and subsequently processed by four AND gates[2, 14, 16], as shown in Fig. 9(a). These extra output logic gates not only draw current from the power supply, but also deteriorate the phase noise. Aiming at lower phase noise, an improved topology, called re-clocking, is presented in Refs. [21, 22], as shown in Fig. 9(b). This technique still requires extra power-consuming logic gates. More importantly, it requires fine phase shift controlled by the buffers and the settling time of the latches[21]. Taking the 4 GHz input clock for example, a quarter of its period is only 62.5 ps. This makes the re-clocking technique only suitable for the advanced process implementation, such as Refs. [21, 22] in 45 nm and 65 nm CMOS, respectively.

A simplified single-ended version of the high-performance multi-mode divider in 0.13 μm CMOS is presented in Fig. 10(a)[23]. The divide-by-2 divider with direct 25%-duty-cycle quadrature outputs is used for WCDMA and GSM high

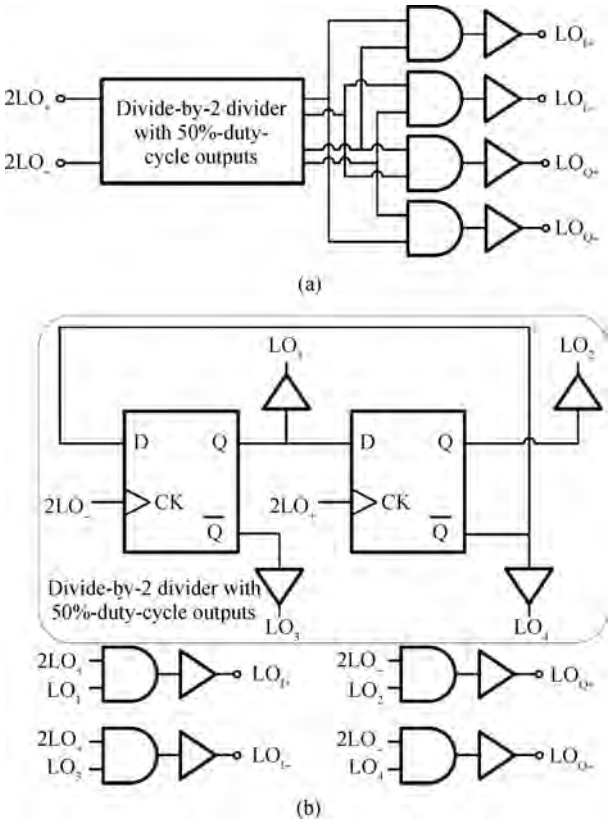

Fig. 9. Conventional methods to generate the 4-phase 25%-duty-cycle clocks. (a) Simply with the output logic gates. (b) With the re-clocking technique.

band. For GSM low band, the divide-by-4 action is needed. This is realized by cascading a divide-by-2 divider with 50%-duty-cycle quadrature outputs and a divide-by-2 divider with 25%-duty-cycle quadrature outputs. The other output of the 50%-duty-cycle divide-by-2 divider is connected to a dummy capacitor for balance. In order to save power as much as possible, the mode selection is done by switching the power supplies of the buffers before the divide-by-2 dividers.

To meet the stringent LO phase noise requirements in receivers, divide-by-2 dividers realized in the full-swing digital CMOS logic, which allows low phase noise operation, are preferred. Besides, considering the non-ideal rise and fall times of the LO pulse, which have impact on the noise and linearity of receivers[2], divide-by-2 dividers should also be fast. As illustrated in Fig. 10(b) and 10(c), Razavi's and Wang's divide-by-2 topologies[24, 25] have been chosen for the divide-by-2 circuits with 25% and 50% duty-cycle outputs, respectively. They exhibit low phase noise and have the potential for high speed applications since there is no stacked PMOS and the signal goes through only two gates per-cycle.

Figure 10(b) depicts the circuit of the divide-by-2 divider with 25% duty-cycle outputs[24]. It is based on the flip-flop topology and comprises two mutually coupled latches. For each latch, there are the sensing pairs (NM1 and NM4, NM5 and NM8), the regenerative loops (NM2 and NM3, NM6 and NM7) and the pull-up devices (PM1–PM4). The operation of this divide-by-2 divider is controlled by the PMOS devices. When the clock is high, PM1–PM2 are off and PM3–PM4 are

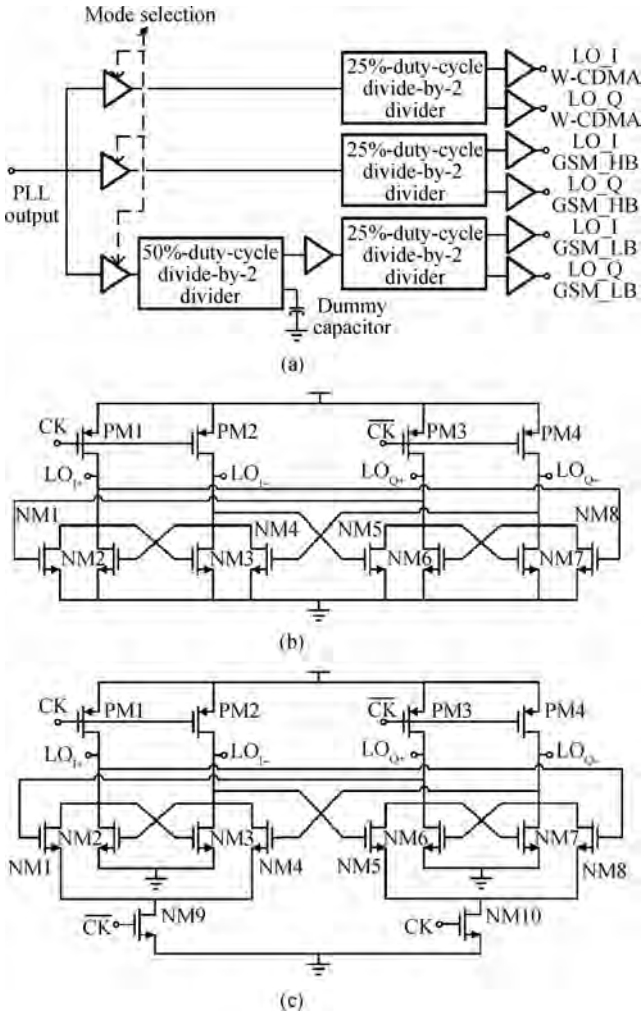

Fig. 10. (a) Proposed multi-mode 25%-duty-cycle LO generator architecture. (b) 25%-duty-cycle divide-by-2 divider. (c) 50%-duty-cycle divide-by-2 divider.

on. The left latch is in the sense mode and the right latch is in the store mode. When the clock goes low, these two latches exchange their states. At any time, only one of four outputs is high, while the other three are low. The reason is that there are two requirements to make the output high. One demand is that the corresponding pull-up PMOS device is turned on, and the other demand is that the gate of the corresponding sense device is connected to the output of the other latch, which is low at the previous phase. So, this divide-by-2 divider has inherent quadrature 25%-duty-cycle outputs.

Figure 10(c) shows the circuit of the divide-by-2 divider with 50%-duty-cycle outputs[25]. It is also flip-flop based. Like the divide-by-2 divider in Fig. 10(b), for each latch, there are sensing pairs, regenerative loops and pull-up devices. However, two clocked switches, NM9 and NM10, are added. This divide-by-2 divider is controlled by these two clocked switches rather than the PMOS devices as the divide-by-2 divider in Fig. 10(b). For this divide-by-2 divider, when the clock is high, the left latch is in the store mode, and the right latch is in the sense mode. When the clock goes low, the state exchange occurs. This essential difference makes these two divide-by-2 dividers exhibit different output duty-cycle properties.

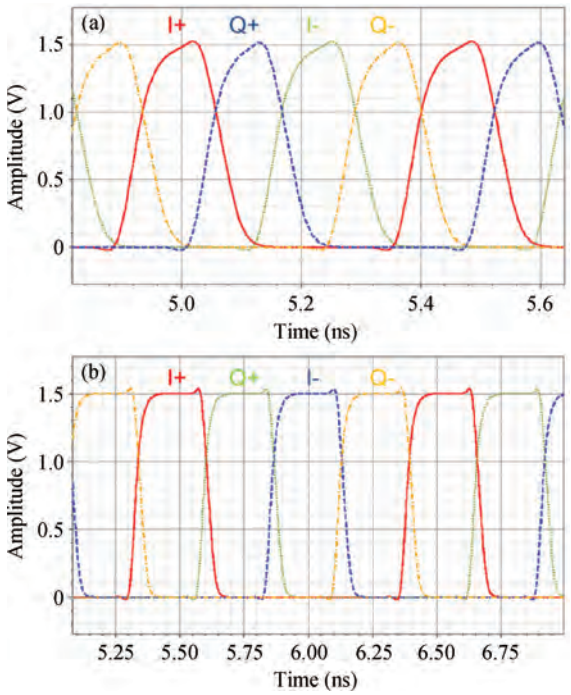

Fig. 11. Transient simulation results in the worst process and temperature case. (a) Divide-by-2 mode for WCDMA. (b) Divide-by-4 mode for GSM low band.

The transient simulation results in the real application with the mixer load for WCDMA and GSM low band modes are shown in Figs. 11(a) and 11(b), respectively. Both the divide-by-2 and divide-by-4 modes with 25%-duty-cycle quadrature outputs can work properly with better than 60 ps rise and fall times in the worst process and temperature case.

Current consumption has been minimized while meeting phase noise and mismatch requirements. The GSM standard has a stringent phase noise demand in order to meet the sensitivity requirements under the blocking conditions. In this application, a simulated phase noise of –149.3 dBc/Hz at 3 MHz offset is achieved. Besides, a phase mismatch of less than 0.5° between the I and Q outputs is ensured at 3σ in the Monte Carlo simulation. To compare with the peer's work, the proposed divider is applied with a 500 MHz clock and it consumes 3.6 mW, saving 10% compared with 4 mW in Ref. [16].

3.5. Constant-g_m biasing with an on-chip resistor

For the receiver RF front-end architecture shown in Fig. 3, the gain is proportional to the product of the g_m of the LNA and the transimpedance of the TIA. To overcome the process and temperature variations of the transimpedance, the main transistors in the LNA are biased with the constant-g_m with an on-chip resistor, as shown in Fig. 4. The constant-g_m biasing circuit is shown in Fig. 12. Since the generated g_m is inversely proportional to the value of the resistor, the variations of the transimpedance are tracked by the g_m when this resistor is integrated on-chip and placed close to the transimpedance. Simulation results reveal that, the gain difference for different process corners and temperatures is at most 0.6 dB.

The receiver would be desensitized due to the bias noise up-conversion when the TX leakage and other blockers are pre-

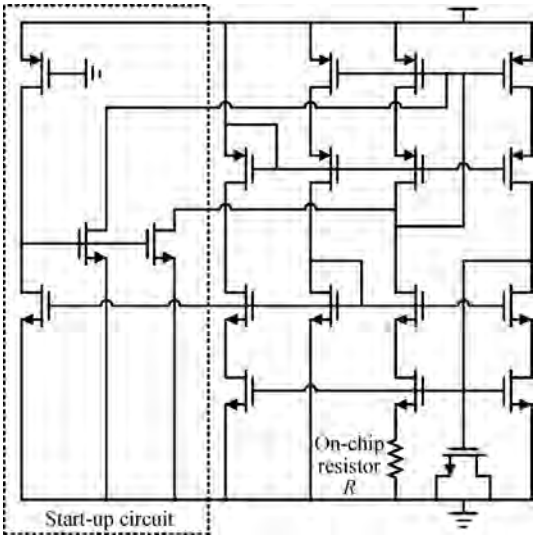

Fig. 12. Constant-g_m biasing with an on-chip resistor.

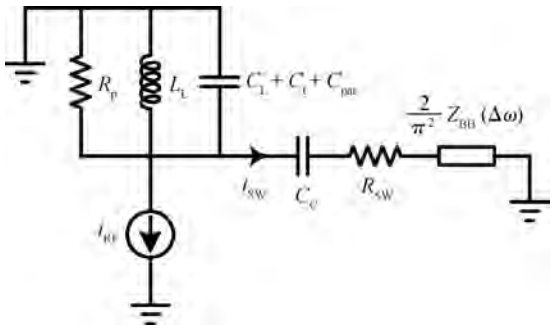

Fig. 13. Equivalent circuit of the RF front-end.

sented. So the constant-g_m block is carefully designed with regard to its output noise, especially the flicker noise.

4. Circuit parameter optimization

In the conventional designs, the parallel LC tank of the LNA is designed to resonate at the signal frequency; and the coupling capacitors between the LNA and mixer are sized large enough to let the output current of the LNA flow to the mixer as much as possible. However, this cannot optimize the RF front-end to the best performance[13, 14]. This work treats the RF front-end as a whole and the parameters of the LC tank are decided after a joint optimization with the parasitic capacitance, the coupling capacitance between the LNA and mixer, the ON resistance of the switches and the up-converted baseband impedance.

Figure 13 depicts the equivalent circuit of the aforementioned RF front-end for the parameter optimization analysis. The inductor in the LC tank is modeled as a parallel network including an inductor L_L, a capacitor C_L and a resistor R_p. C_t and C_{par} represent the capacitor array in the LC tank and the parasitic capacitors, respectively. As discussed in Section 3.2, only one of four paths can be assumed to be ON at any instant. So the impedance seen by the LNA is the series of the coupling capacitance C_C, the ON resistance of the switches R_{sw} and the up-converted baseband impedance, as shown in Fig. 13. It should be noted that the baseband impedance is scaled by $2/\pi^2$ during the frequency-shift[14].

When the LNA is assumed to be applied with an input signal at $\omega_{LO}+\Delta\omega$, from the equivalent circuit shown in Fig. 13, the current delivered to the switches is equal to

$$i_{sw}(\omega_{LO}+\Delta\omega)=\frac{Z_L(\omega_{LO}+\Delta\omega)}{Z_L(\omega_{LO}+\Delta\omega)+Z_C(\omega_{LO}+\Delta\omega)+R_{SW}+\frac{2}{\pi^2}Z_{BB}(\Delta\omega)}, \tag{5}$$

where $Z_L=L_L//(C_L+C_t+C_{par})//R_P$ and $Z_C=1/sC_C$.

Since the rail-to-rail 25%-duty-cycle clock can be represented as

$$F(t)=\frac{\sqrt{2}}{\pi}\left(\cos\omega_{LO}t+\frac{1}{3}\cos 3\omega_{LO}t-\frac{1}{5}\cos 5\omega_{LO}t+\cdots\right), \tag{6}$$

the conversion gain (CG), defined as the baseband current flowing into the TIA over the totally converted RF current, can be obtained as

$$\mathrm{CG}=\frac{i_{BB}(\Delta\omega)}{i_{RF}(\omega_{LO}+\Delta\omega)}=\frac{\sqrt{2}}{\pi}\frac{i_{sw}(\omega_{LO}+\Delta\omega)}{i_{RF}(\omega_{LO}+\Delta\omega)}=\frac{\sqrt{2}}{\pi}\times\frac{Z_L(\omega_{LO}+\Delta\omega)}{Z_L(\omega_{LO}+\Delta\omega)+Z_C(\omega_{LO}+\Delta\omega)+R_{SW}+\frac{2}{\pi^2}Z_{BB}(\Delta\omega)}. \tag{7}$$

Over the desired signal frequency band, the impedance Z_{BB} can be assumed to be purely resistive and equal to R_{BB}. So when the imagine part of $[Z_L(\omega_{LO}+\Delta\omega)+Z_C(\omega_{LO}+\Delta\omega)]$ is zero, that is, Z_L resonates with C_C, the maximum conversion gain is achieved[14]. In this case, the maximal conversion gain can be calculated as

$$\mathrm{CG}_{max}=\frac{1}{\sqrt{2}\pi}\sqrt{\frac{R_P}{R_{SW}+\frac{2}{\pi^2}R_{BB}}}, \tag{8}$$

when

$$\frac{1}{\omega_{LO}C_C}=\sqrt{R_P\left(R_{SW}+\frac{2}{\pi^2}R_{BB}\right)}. \tag{9}$$

Intuitively, this result can be explained as follows. The current delivered to the branch, comprising of the coupling capacitor, the switches and the up-converted baseband impedance, is the total RF current amplified by the effective Q of the entire load shown in Fig. 13.

Equations (8) and (9) not only indicate the optimum size of the coupling capacitor, but also provide some guidelines to maximize the conversion gain. First, R_P should be maximized. A spiral inductor with a high quality factor is preferred and the degradation of the quality factor during the layout should be taken care of. Second, the ON resistance of the switches R_{SW} should be lowered. However, a smaller ON resistance means a bigger switch size. It would require stronger LO buffers and

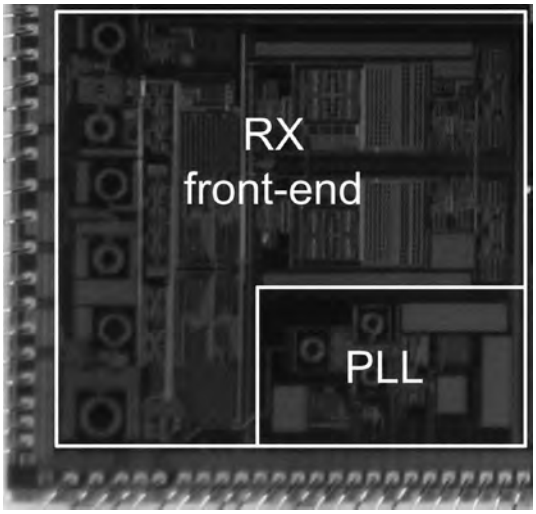

Fig. 14. Chip microphotograph.

more power consumption. Third, the DC gain and bandwidth of the operational amplifiers in the TIA should be properly designed to lower R_{BB} in the desired signal frequency band.

5. Experiment result

The receiver RF front-end was fabricated in a 1P8M 0.13 μm RF CMOS process and implemented in a receiver with an on-chip frequency synthesizer. The chip microphotograph of the receiver is shown in Fig. 14, where the core chip area is 2.5×2.4 mm^2.

The RF inputs are matched using off-chip LC components. Figure 15 illustrates the measured S_{11} for WCDMA and GSM low band. Two traces in Fig. 15(b) depict the measurement results when the GSM low band channel is configured to support the GSM 850 band and the GSM 900 band, respectively. The maximum voltage gain of the receiver is 74/79 dB for WCDMA/GSM, respectively. Figure 16 shows the receiver output spectrum with –110 dBm RF input signal for the WCDMA mode.

The NF is measured using the Y-factor method with Agilent E4440A spectrum analyzer and 346C noise source. For WCDMA, the built-in NF measurement function for the spectrum analyzer is used. For GSM, considering the narrow band characteristic, the noise source is switched on and off manually, and the change of the output noise floor is read from the spectrum analyzer. The change of the noise floor is defined as $Y = N_{on}/N_{off}$. Then the NF is expressed as $\mathrm{NF} = \mathrm{ENR}/(Y-1)$, where the excessive noise ratio (ENR) is provided by the noise source manufacturer. Figures 17(a) and 17(b) illustrate the measured noise figure for WCDMA and GSM, respectively. 5.0/5.1 dB NF are achieved for WCDMA/GSM, respectively. Due to the low-flicker-noise passive mixer, a flicker noise corner of 40 kHz is obtained.

Figures 18 and 19 show the in-band IP3 measurement results with the highest gain. Figures 18(a) and 18(b) are the output spectrum when the receiver is applied with -40 dBm two-tone input. The two-tone frequencies are set at 10/21 MHz and 0.8/1.7 MHz offset from the LO frequency for WCDMA and GSM, respectively. Thus the IMD3 products lie in 1 MHz

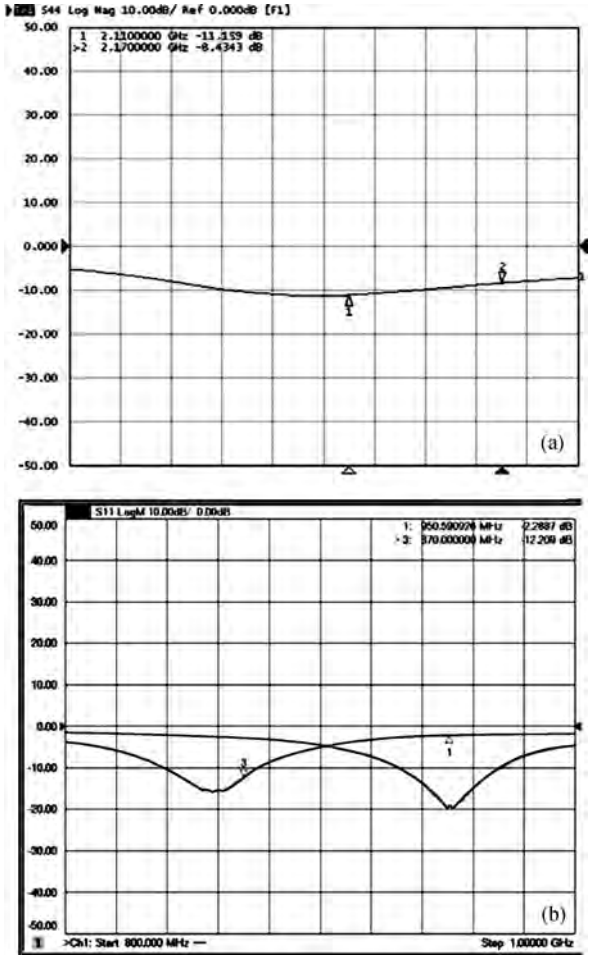

Fig. 15. Measured S_{11} for (a) WCDMA and (b) GSM low band.

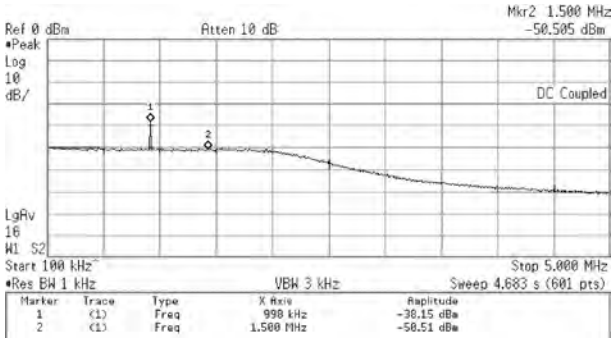

Fig. 16. Measured output spectrum of the receiver with a –110 dBm RF input signal for WCDMA.

and 0.1 MHz for WCDMA and GSM, respectively. When the two-tone power is swept, the linearity measurement results are shown in Figs. 19(a) and 19(b) for WCDMA and GSM, respectively. Both modes obtain -6 dBm input IP3 (IIP3).

For WCDMA, the maximum output power could be $+25$ dBm ($+24$ dBm with tolerance of +1/–3) at the antenna. Considering 2 dB loss between the PA output to the antenna, and 52 dB of the duplexer isolation at the TX frequency, the receiver will see TX leakage of -25 dBm ($25+2-52$). IP2 is measured with the TX leakage modeled as –25 dBm two-tone signals set at the TX frequency band, which is 190 MHz below

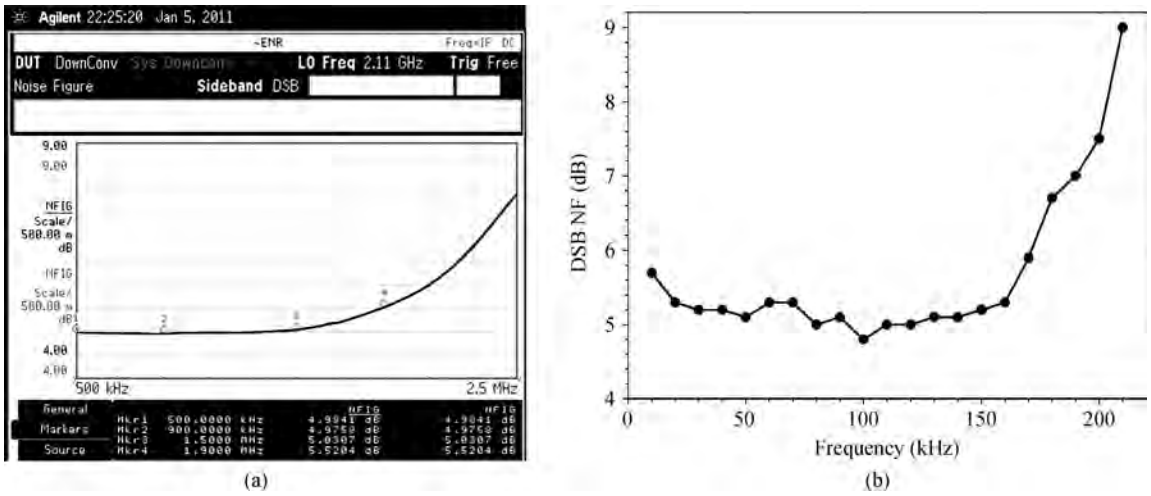

Fig. 17. Measured noise figure for (a) WCDMA and (b) GSM low band.

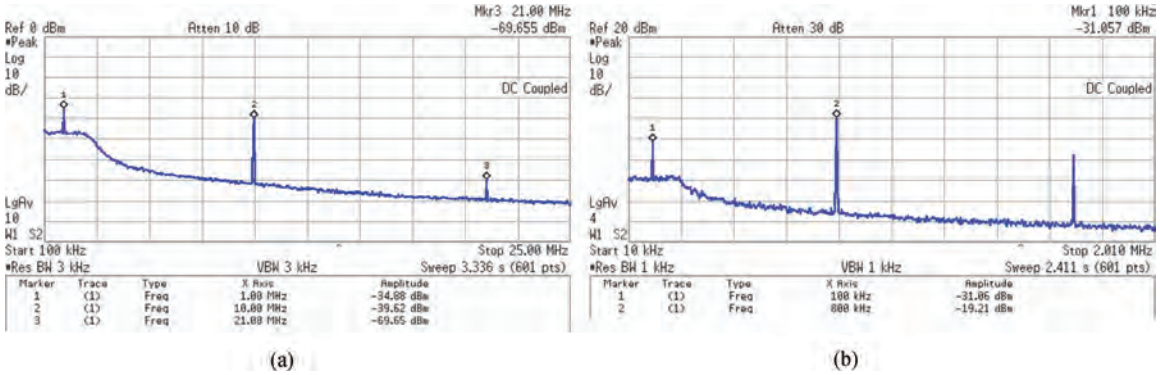

Fig. 18. Measured output spectrum in linearity tests for (a) WCDMA and (b) GSM low band.

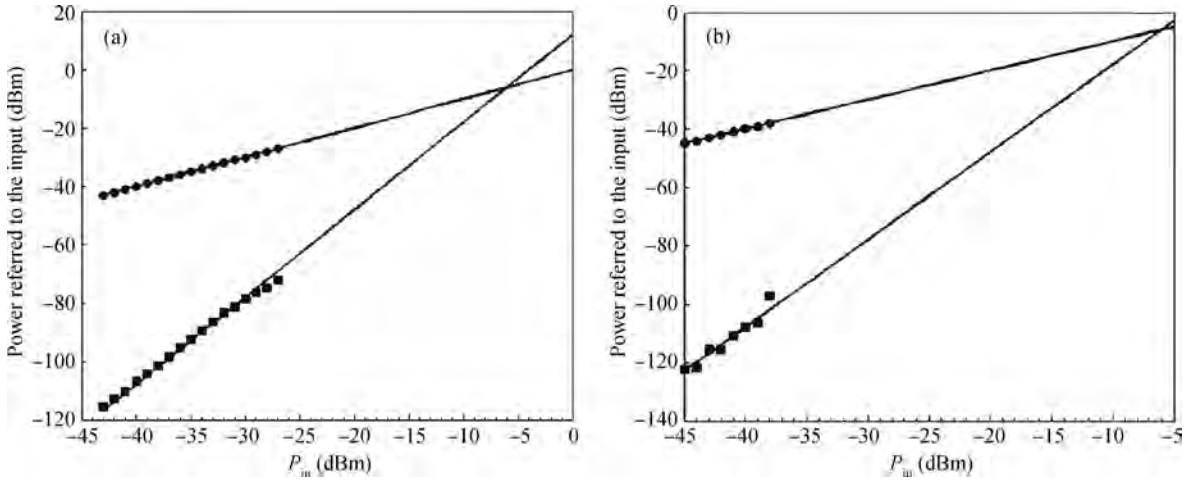

Fig. 19. IP3 measurement results for (a) WCDMA and (b) GSM low band.

the RX band. After tuning the IP2 calibration DACs, better than +60 dBm input IP2 (IIP2) is achieved.

The whole circuit, working under 1.5 V supply voltage, consumes 80/47 mA for WCDMA/GSM, respectively.

The performance is summarized and compared with the references in Table 1. The design target is satisfied with an 11 dB IIP3 margin. Table 1 also demonstrates that, owing to the proper architecture and linearity enhancement techniques, the linearity of this work is superior to the peers' works.

6. Conclusion

This paper presents the analysis and design of a fully integrated receiver RF front-end implemented for WCDMA/GSM

Table 1. Performance summary and comparison.

Parameter	Measured result		Design target	ISSCC 2010[4]	RFIC 2009[15]	Unit
	WCDMA	GSM				
Technology	130 nm	130 nm	—	130 nm	65 nm	CMOS
V_{DD}	1.5	1.5	—	1.5	1.3	V
Voltage gain	74	79	> 60	38.5	37.1	dB
DSB NF	5.0	5.1	< 9	2.6	3	dB
$1/f$ noise corner	40	40	—	50	—	kHz
In-band IIP3	–6*	–6**	> -17	–17.6	–7.4	dBm
IIP2	> 60	> 60	> 58	> 60	62.5	dBm
Power	80	47	—	15***	21****	mA

*10, 20 MHz offset blockers; **0.8, 1.6 MHz offset blockers;
***not include the frequency synthesizer; ****only include the LNA and mixer.

in 0.13 μm RF CMOS. SAW-less operation for WCDMA is supported. Enhancement and calibration techniques are adopted to improve the linearity in terms of both IP3 and IP2. A high-performance multi-mode divider is proposed to provide the 4-phase 25%-duty-cycle LO. A constant-g_m biasing with an on-chip resistor makes the conversion gain of the RF front-end invulnerable to the process and temperature variations of the transimpedance. The measurement results show that the receiver in which this high-linearity RF front-end is implemented achieves -6 dBm IIP3 and better than $+60$ dBm IIP2 for all modes and bands.

References

[1] Razavi B. RF microelectronics. Upper Saddle River: Prentice Hall, 1998

[2] Kaczman D, Shah M, Alam M, et al. A single chip 10-band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with DigRF 3G interface and +90 dBm IIP2. IEEE J Solid-State Circuits, 2009, 44(3): 718

[3] Hu S, Li W N, Huang Y M, et al. A high-linearity receiver RF front-end with a high-performance 25%-duty-cycle LO generator for WCDMA/GSM applications. Proc IEEE International Symposium on Radio-Frequency Integration Technology, RFIT, 2011

[4] Feng Y, Takemura G, Kawaguchi S, et al. A low-power low-noise direct-conversion front-end with digitally assisted IIP2 background self-calibration. Proc IEEE Intl Solid State Circuits Conf, 2010: 70

[5] Kim T W, Kim B K, Lee K R. Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors. IEEE J Solid-State Circuits, 2004, 39(1): 223

[6] Aparin V, Larson L E. Modified derivative superposition method for linearizing FET low-noise amplifiers. IEEE Trans Microw Theory Tech, 2005, 53(2): 571

[7] Khatri H, Gudem P S, Larson L E. An active transmitter leakage suppression technique for CMOS SAW-less CDMA receivers. IEEE J Solid-State Circuits, 2010, 45(8): 1590

[8] Kim N, Aparin V, Barnett K, et al. A cellular-band CDMA 0.25 μm CMOS LNA linearized using active post-distortion. IEEE J Solid-State Circuits, 2006, 41(7): 1530

[9] Kim N, Larson L E, Aparin V. A highly linear SAW-less CMOS receiver using a mixer with embedded TX filtering for WCDMA. IEEE J Solid-State Circuits, 2009, 44(8): 2126

[10] Jin T H, Kim T W. A 5.5 mW +9.4-dBm IIP3 1.8-dB NF CMOS LNA employing multiple gated transistors with capacitance desensitization. IEEE Trans Microw Theory Tech, 2010, 58(10): 2529

[11] Andreani P, Sjoland H. Noise optimization of an inductively degenerated CMOS low noise amplifier. IEEE Trans Circuits Syst II, Analog, Digit Signal Process, 2001, 48(9): 835

[12] Leenaerts D, Readman-White W. $1/f$ noise in passive CMOS mixers for low and zero IF receivers. Proc European Solid-State Circuits Conf, ESSCIRC, 2001: 41

[13] Mirzaei A, Darabi H, Leete J, et al. Analysis and optimization of current-driven passive mixers in narrowband direct-conversion receivers. IEEE J Solid-State Circuits, 2009, 44(10): 2678

[14] Mirzaei A, Darabi H, Leete J, et al. Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers. IEEE Trans Circuits Syst I: Reg Papers, 2010, 57(9): 2353

[15] Khatri H, Liu L, Chang T, et al. A SAW-less CDMA receiver front-end with single-ended LNA and single-balanced mixer with 25% duty-cycle LO in 65 nm CMOS. Proc IEEE RF Integrated Circuits Symp, RFIC, 2009: 13

[16] Blaakmeer S C, Klumperink E A M, Leenaerts D M W, et al. The Blixer, a wideband balun-LNA-I/Q-mixer topology. IEEE J Solid-State Circuits, 2008, 43(12): 2706

[17] Giannini V, Nuzzo P, Soens C, et al. A 2-mm^2 0.1–5 GHz software-defined radio receiver in 45-nm digital CMOS. IEEE J Solid-State Circuits, 2009, 44(12): 3486

[18] Manstretta D, Brandolini M, Svelto F. Second-order intermodulation mechanisms in CMOS downconverters. IEEE J Solid-State Circuits, 2003, 38(3): 394

[19] Chehrazi S, Mirzaei A, Abidi A. Second-order intermodulation in current-commutating passive FET mixers. IEEE Trans Circuits Syst I, Reg Papers, 2009, 56(12): 2556

[20] Balankutty A, Yu S, Feng Y, et al. A 0.6-V zero-IF/low-IF receiver with integrated fractional-N synthesizer for 2.4-GHz ISM-band applications. IEEE J Solid-State Circuits, 2010, 45(3): 538

[21] He X, van Sinderen J. A low-power, low-EVM, SAW-less WCDMA transmitter using direct quadrature voltage modulation. IEEE J Solid-State Circuits, 2009, 44(12): 3448

[22] Andrews C, Molnar A C. A passive mixer-first receiver with digitally controlled and widely tunable RF interface. IEEE J Solid-State Circuits, 2010, 45(12): 2696

[23] Hu S, Li W N, Huang Y M, et al. Design of a low-power low-phase-noise multi-mode divider with 25%-duty-cycle outputs in 0.13 μm CMOS. IEEE 9th International Conference on ASIC, ASICON, 2011

[24] Razavi B, Lee K F, Yan R H. Design of high-speed, low-power frequency dividers and phase-locked loops in deep submicron CMOS. IEEE J Solid-State Circuits, 1995, 30(2): 101

[25] Wang H. A 1.8 V 3 mW 16.8 GHz frequency divider in 0.25 μm CMOS. Proc IEEE Intl Solid State Circuits Conf, 2000: 196