Analysis and implementation of an improved recycling folded cascode amplifier*

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Abstract: A generally improved recycling folded cascode (IRFC) is analyzed and implemented. Analysis and comparisons among the IRFC, the original recycling folded cascode (RFC) and the conventional folded cascode (FC) are made, and it is shown that with the flexible structure of IRFC, significant enhancement in transconductance, slew rate and noise can be achieved. Prototype amplifiers were fabricated in 0.13 μm technology. Measurement shows that IRFC has 3× enhancement in gain-bandwidth and slew rate over conventional FC, and the enhancement is 1.5× when compared with the RFC.

Key words: CMOS; operational amplifiers; transconductance; noise; low-power circuits
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1. Introduction

The operational transconductance amplifier (OTA) is still a necessary building block for many applications, such as baseband circuits[1] and data convertors[2], and consumes considerable power. A power-efficient OTA should have large transconductance while consuming a small amount of power. In Ref. [3], an AB output stage is adopted to enhance gain-band width (GBW), but it requires a large capacitor to emulate a battery. In Ref. [4], a slew rate enhancing method is proposed. In Ref. [5], a recycling folded cascode (RFC) topology was proposed to enhance the power efficiency of OTA. In RFC, current mirrors are formed by splitting transistors to enhance transconductance and slew rate. However, AC and DC currents basically share the same path in RFC, which makes the DC currents from the cascoding branch necessary for current mirrors. This not only limits the enhancement of performance, but also makes the modification unsuitable for other structures of OTAs, such as telescopic OTA. In this paper, we analyze the IRFC in detail and compare the IRFC and FC. We introduce design parameters in IRFC to make it more flexible and more general than RFC, and we prove IRFC to be a more general type of folded-cascode. Optimization of transconductance and noise under constraint is discussed later. Simulation and measurement results are also given to verify the effectiveness of the structure and our analysis.

2. Analysis of IRFC

The topology and DC current of FC OTA and IRFC OTA are shown in Figs. 1(a) and 1(b), respectively. In IRFC, the original input pair M1 and M2 in FC is divided into M1a, M1b, M2a and M2b, in which the ratio of sizes of transistors is M1a : M1b = M2a : M2b = p : $(1-p)$, where $0 < p \leqslant 1$. Also, M3 and M4 in FC are split into M3a, M3b, M3c and M4a, M4b, M4c (Fig. 1(b)), in which the ratio of sizes of transistors is M3a : M3b : M3c = M4a : M4b : M4c = $(1 + p) : \alpha(1 - p) : \beta(1 - p)$, where $\alpha + \beta = 1$. M3a : M3b and M4a : M4b are current mirrors with a ratio of $(1 + p) : \alpha(1 - p)$, which magnify AC currents to improve transconductance. On the other hand, in order to keep correct DC current, M3c and M4c form the DC path. M3c and M4c are biased at constant gate voltage, so ideally only DC current flows into them. To further increase the AC impedance of the DC path, cascode transistors M11b and M12b are inserted. Accordingly, M11a and M12a are inserted in the AC path to improve the matching between DC and AC paths, in which the sizes of transistors M11a : M11b = M12a : M12b = $\alpha : \beta$. Another benefit of transistors M11a and M12a is that they enhance the matching in current mirrors[5]. This separation of AC and DC paths is similar to current bleeding technique in mixers to enhance conversion gain[6], but here it not only improves the performances but also grants more flexibility in OTA design, as will be discussed below.

To make our discussion more general, we consider the limiting case of $p \to 1$, or, the case of FC. In this case, there is virtually no current mirror, so the ratio of current mirror $(1 + p) : \alpha(1 - p) = 0$, i.e., we can express the boundary condition as:

$$\lim_{p\to 1} \alpha = \infty, \quad \lim_{p\to 1} \alpha\,(1 - p) = \infty. \tag{1}$$

Equation (1) can also be intuitively understood by imagining that when $p = 1$, the two branches of current $\alpha(1 - p)I_b$ and $\beta(1 - p)I_b$ have the same infinity magnitude but the opposite direction, making the total current amount to zero. With Eq. (1), all equations in our analysis are effective for FC OTA. On the other hand, RFC is another special case of IRFC with $p = 0.5$ and $\alpha = 1$, so IRFC is a more general type of folded cascode. For clear comparison, we will use the parameters of the components of the original FC and design parameter p and α in the following expressions to describe the performance of OTAs.

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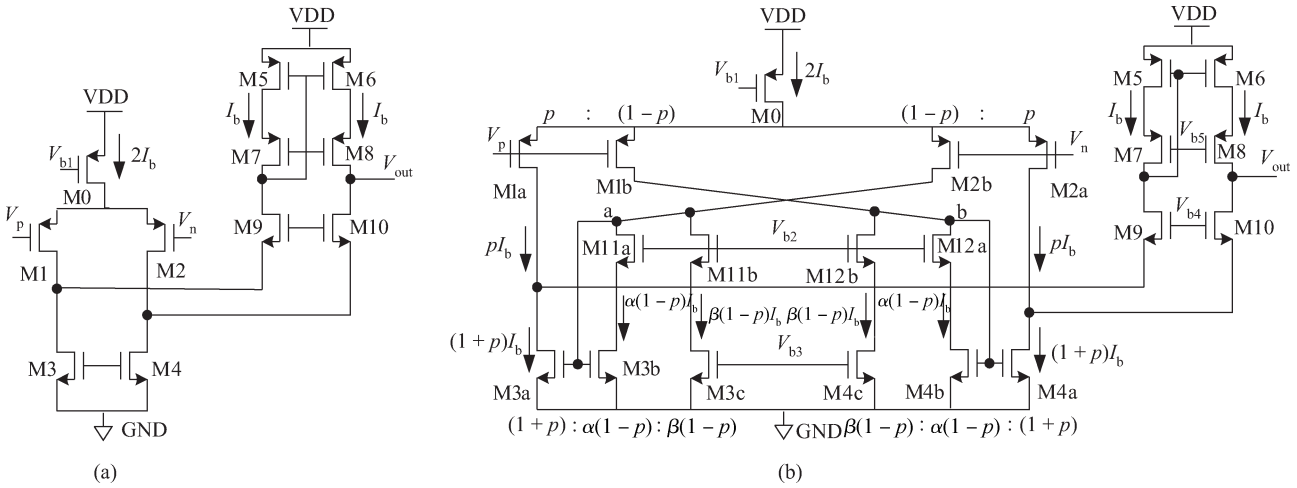

Fig. 1. (a) FC OTA. (b) IRFC OTA.

2.1. Effective transconductance and gain

The effective transconductance of IRFC can be found by calculating the short-circuit current at the output with regard to input[7]. Suppose the transconductance of folded cascode OTA is G_{mFC} (which is the transconductance of M1/M2, $g_{\mathrm{m1,2}}$), then the transconductance of IRFC OTA with the same power consumption can be expressed as:

$$G_{\mathrm{mIRFC}} = \left(p + \frac{1+p}{\alpha}\right) G_{\mathrm{mFC}}. \tag{2}$$

From Eq. (2), it can be seen that we may choose proper parameter p and α to enhance the transconductance of IRFC, which means larger GBW, higher speed and better power efficiency of OTA. Compared with RFC which can achieve 2 times enhancement over FC, IRFC can have better enhancement with proper p and α. In reality, the enhancement of transconductance is slightly lower than Eq. (2) due to the finite output impedance of M3c and M4c. The low frequency gain of IRFC is decided by its effective transconductance and low frequency output impedance. Besides its larger transconductance, IRFC has higher output impedance because compared with M4 in FC, less current flows through M4a[5]. With enhanced effective transconductance and higher output impedance, IRFC has a higher DC gain than FC.

2.2. Poles and zero

The dominant pole (ω_{p1}) in IRFC is at the output node and one non-dominant pole (ω_{p2}) of IRFC is decided by the parasites at the source node of M9/M10, like the case in FC OTA. In addition, the current mirrors of IRFC introduce a pole-zero pair (ω_{p3} and ω_{z3}). The location of poles and zero in S-plane is shown in Fig. 2. The pole-zero pair of IRFC can be expressed as:

$$\omega_{\mathrm{p3}} = \frac{\alpha(1-p) g_{\mathrm{m3,4}}}{[1+p+\alpha(1-p)]\, C_{\mathrm{gs3,4}}}, \tag{3}$$

$$\omega_{\mathrm{z3}} = \frac{[(1-p)(1+p)+\alpha p(1-p)]\, g_{\mathrm{m3,4}}}{[p(1+p)+\alpha p(1-p)]\, C_{\mathrm{gs3,4}}}, \tag{4}$$

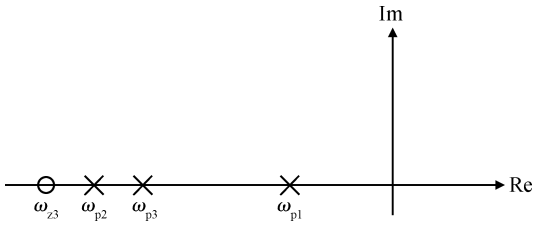

Fig. 2. Poles and zero in S-plane.

where $g_{\mathrm{m3,4}}$ and $C_{\mathrm{gs3,4}}$ are the transconductance and gate–source capacitance of transistor M3/M4 in FC OTA. By comparing the location of the pole and zero in S-plane, we have:

$$\frac{\omega_{\mathrm{z3}}}{\omega_{\mathrm{p3}}} = \frac{(1-p)(1+p)+\alpha p(1-p)}{\alpha p(1-p)} = 1 + \frac{1+p}{\alpha p}. \tag{5}$$

For FC, $p = 1$. Combining Eq. (1) and Eq. (5), we have $\omega_{\mathrm{z3}}/\omega_{\mathrm{p3}} = 1$, i.e., the zero and the pole cancel each other. Actually, phase margin can be a main factor limiting the selection of parameter p and α, as discussed in the next section.

2.3. Slew rate

The slew rate (SR) of IRFC OTA can be calculated as follow. Suppose V_{p} goes high, then M1a and M1b turn off, and consequently M4b, M4a and M2a turn off. The current flowing through M2b is $2I_{\mathrm{b}}$. Part of this current flows through the DC path (M11b and M3c), while the rest goes into M3b and is magnified by the current mirror. With the magnified current, the slew rate is also enhanced. The slew rate can be expressed as:

$$\mathrm{SR}_{\mathrm{IRFC}} = \frac{(1+p)\,[2-(1-\alpha)(1-p)]\, I_{\mathrm{b}}}{\alpha(1-p) C_{\mathrm{L}}}. \tag{6}$$

Equation (6) is also valid for FC and RFC. In practice, the slew rate is limited by non-idealities and thus cannot reach the theoretical value. First, the transient response of current mirror to large signal is different from the case of small signal, so the current ratio is no longer accurate[5]. In addition, for low supply voltage in advanced technologies, transistors M5 and M6 are

likely to enter linear region when output current is large, and thus limit the slew rate.

2.4. Noise

Using the method in Ref. [8], the input-referred noise of IRFC OTA is expressed in Eq. (7):

$$\overline{e_{\rm nf}^2} = \frac{8k_{\rm B}T\gamma}{g_{\rm m1}[p+(1+p)/\alpha]^2} \times \left\{ p + \frac{(1+p)^2}{\alpha^2(1-p)} + \frac{g_{\rm m3}}{g_{\rm m1}}\left[\frac{1+p}{2} + \frac{(1+p)^2}{2\alpha^2(1-p)}\right] + \frac{g_{\rm m5}}{g_{\rm m6}} \right\} + \frac{K_{\rm FP}}{\mu_{\rm p}C_{\rm ox}^2 W_1 L_1 \left(p+\frac{1+p}{\alpha}\right)^2 f} \left\{ p + \frac{(1+p)^2}{\alpha^2(1-p)} + \frac{K_{\rm FN}}{K_{\rm FP}} \times \left[1 + p + \frac{(1+p)^2}{\alpha^2(1-p)}\right]\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_5}\right)^2 \right\}, \tag{7}$$

where L_1, L_3 and L_5 are the gate length of M1, M3 and M5 in FC, respectively. Equation (7) is also valid for FC and RFC. The input-referred noise of FC OTA is:

$$\overline{e_{\rm nf\_FC}^2} = \frac{8k_{\rm B}T\gamma}{g_{\rm m1}}\left(1 + \frac{g_{\rm m3}}{g_{\rm m1}} + \frac{g_{\rm m5}}{g_{\rm m1}}\right) + \frac{K_{\rm FP}}{\mu_{\rm p}C_{\rm ox}^2 W_1 L_1 f}\left[1 + 2\frac{K_{\rm FN}}{K_{\rm FP}}\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_5}\right)^2\right]. \tag{8}$$

Equation (8) can be obtained by setting $p = 1$ in Eq. (7). Comparing Eq. (7) and Eq. (8), we can observe that the noise currents of transistors M1b, M2b, M3b and M4b are amplified by current mirrors, while the gain of OTA increases at the same time, which suppresses noise of transistors. The two factors affect the input-referred noise in opposite direction, so we can find optimized p and α to minimize noise, as discussed in the next section.

2.5. Offset

Using the method in Ref. [5], we can calculate the input offset variance of IRFC as:

$$\sigma^2(V_{\rm OS,IRFC}) = \frac{2A_{\rm VTP}^2}{W_1 L_1\left(p+\frac{1+p}{\alpha}\right)^2}\left\{ p + \frac{(1+p)^2}{\alpha^2(1-p)} + \frac{\mu_{\rm N}}{\mu_{\rm P}}\frac{A_{\rm VTN}^2}{A_{\rm VTP}^2}\left[1 + p + \frac{(1+p)^2}{\alpha^2(1-p)}\right]\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_5}\right)^2 \right\}, \tag{9}$$

where $A_{\rm VTP}$ and $A_{\rm VTN}$ is the area proportionality constant for threshold voltage of PMOS and NMOS, respectively.

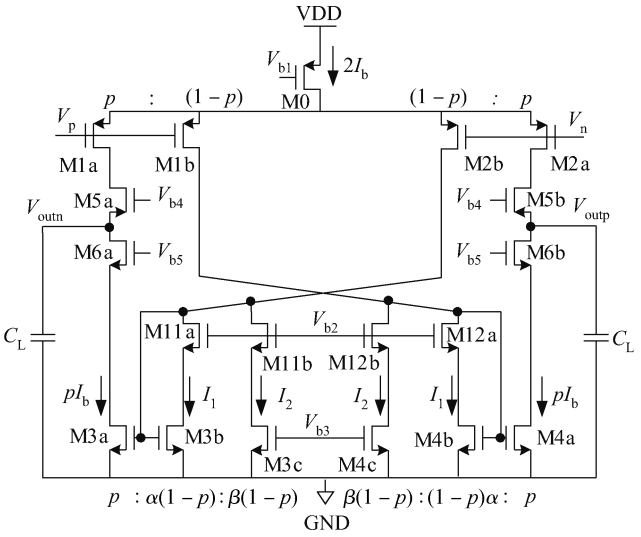

Fig. 3. Improved recycling differential telescopic OTA.

For FC OTA, the input offset variance is

$$\sigma^2(V_{\rm OS,FC}) = \frac{2A_{\rm VTP}^2}{W_1 L_1}\left[1 + 2\frac{\mu_{\rm N}}{\mu_{\rm P}}\frac{A_{\rm VTN}^2}{A_{\rm VTP}^2}\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_5}\right)^2\right]. \tag{10}$$

Such as in the case of noise, the current mirrors boost the drain-current variance and the overall transconductance at the same time, making optimization possible.

2.6. Applicability

In IRFC, the AC and DC current have different paths, so the DC current from the cascode branch is no longer necessary to sustain the correct DC current of current mirrors, which is another advantage over RFC. With the separated AC and DC path, the modification can be applied to various OTAs with differential input and active load, such as differential telescopic OTA (Fig. 3).

3. Design considerations

3.1. Available transconductance enhancement

The enhancement of transconductance is limited by phase margin. Consider Eqs. (3), (4) and (5), with decreased α and fixed p, $\omega_{\rm z3}/\omega_{\rm p3}$ becomes larger, which means that the zero can no longer compensate the pole. In addition, when α decreases, the decreased transconductance of M3b/M4b pushes $\omega_{\rm p3}$ to lower frequency meanwhile the GBW of the OTA increases, thus the phase margin of OTA is degraded. By setting $p = 0.5$, we calculated phase margin versus α and compared it with simulation results (Fig. 4). In our calculations, we assumed $C_{\rm L} = 100C_{\rm gs3,4}$ and $g_{\rm m1,2} = g_{\rm m3,4}$. Since the calculation ignores the effect of non-dominant pole to GBW, there is some difference between calculation and simulation; however, the trends of the calculation and the simulation fit well. From Fig. 4, we can see that α should be greater than 0.4 to achieve enough phase margin and thus avoid ringing in transient response. Generally, the transconductance enhancement should be smaller than 3.5 to guarantee enough phase margin

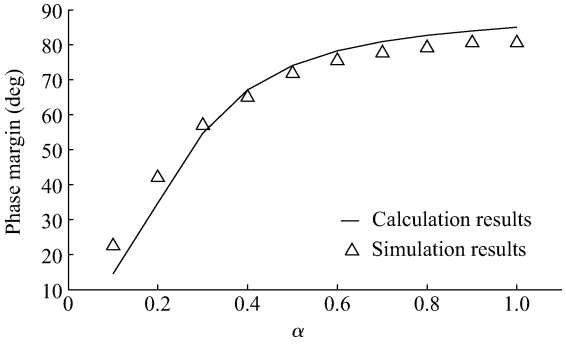

Fig. 4. Calculated and simulated phase margin versus α.

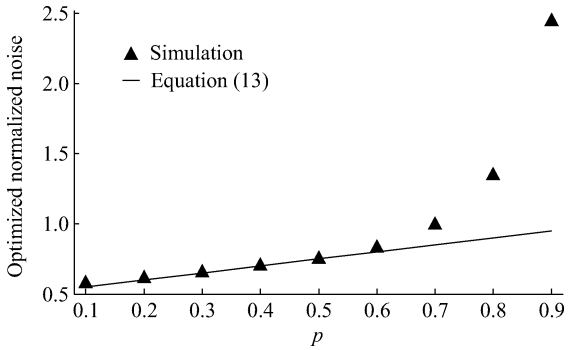

Fig. 5. Calculated and simulated optimized normalized noise.

(about 70°). In fact, when designing IRFC, we have one more dimension of freedom, since we can make trade-off between phase margin and other performances, while in other single stage OTAs, phase margin is generally constant (about 90°).

3.2. Noise consideration

In Ref. [5], RFC can consume less power to achieve the same GBW as FC but at the cost of noise, since no noise optimization was made for RFC. With the flexible structure of IRFC, however, noise performance can be optimized. To simplify Eq. (7), we assume that $L_1 = L_5$ and $g_{m5} = g_{m1}$. With the assumptions above, we have:

$$\overline{e^2_{\text{nf\_IRFC}}} = \frac{1 + p + \dfrac{(1+p)^2}{\alpha^2(1-p)}}{2[p + (1+p)/\alpha]^2} \times \overline{e^2_{\text{nf\_FC}}}. \tag{11}$$

With Eq. (11), we can find optimized p and α for noise. By finding derivative of Eq. (11) regarding α and setting it to zero, we obtain:

$$\alpha = \frac{p}{1-p}. \tag{12}$$

The optimized noise power density for a given p is:

$$\overline{e^2_{\text{nf\_IRFC,opt}}} = \frac{1+p}{2}\overline{e^2_{\text{nf\_FC}}}. \tag{13}$$

From Eq. (13) we can see that the optimized noise is proportional to p. This can be explained by the fact that with small p, the ratio of current mirror M3a : M3b and M4a : M4b is also small, so the noise currents of M1b and M2b are not significantly amplified; in addition, the overall transconductance is mainly decided by α, so it is possible to have small p and large transconductance at the same time, and then the input-referred noise is optimized.

Considering the stability, α should not be too small. Suppose we limit the transconductance enhancement under 3.5 to guarantee phase margin of 70°, then the optimized α with stability constraint is:

$$\alpha = \max\left[\frac{1+p}{3.5-p}, \frac{p}{1-p}\right]. \tag{14}$$

We define the optimized normalized noise as the ratio of the input-referred noise of noise-optimized IRFC and conventional FC, and simulated it for different p (with stability constraint) and compared it with Eq. (13), as shown in Fig. 5. From

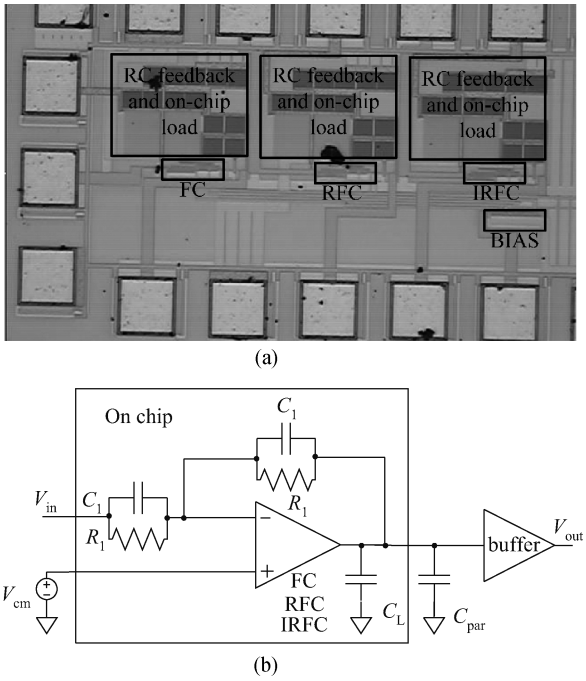

Fig. 6. (a) Chip micrograph. (b) Test schematic.

Fig. 5 we can see that for $p < 0.2$, α is constrained by stability condition and the optimized noise is larger than Eq. (13). For $0.2 < p < 0.5$, the simulated results fit well with Eq. (13). For $p > 0.5$, the optimized value of α in Eq. (12) is greater than 1 and cannot be reached, and thus the noise of IRFC for $p > 0.5$ cannot reach its lower bound in Eq. (13). The global optimized noise of IRFC can be obtained with $p = 0.1$; however, setting $p = 0.1$ means M1b : M1a = 9 : 1 and this large ratio can induce matching problem[8]. Thus, a more practical value of p is 0.2, when M1b : M1a = 4 : 1, and the input-referred noise reduction compared to FC is 39% (2.1 dB). This also implies the potential to design a noise-optimized IRFC having the similar (or better) noise performance and transconductance with FC but consuming far less power. In addition, since the expression of input offset in Eq. (9) is similar to Eq. (7), we can expect that the offset of IRFC has similar characteristic with noise.

As for designs that do not meet the mentioned assumptions, optimized noise can still be found, though the expression can be more complicated. The trend of optimized noise versus p should be similar, since the most influential element in optimized noise is still the ratio of current mirrors.

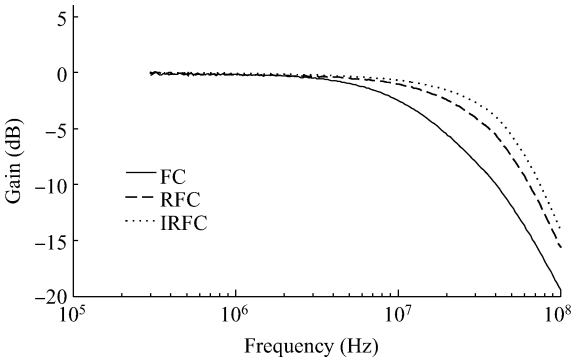

Fig. 7. Measured close-loop bandwidth.

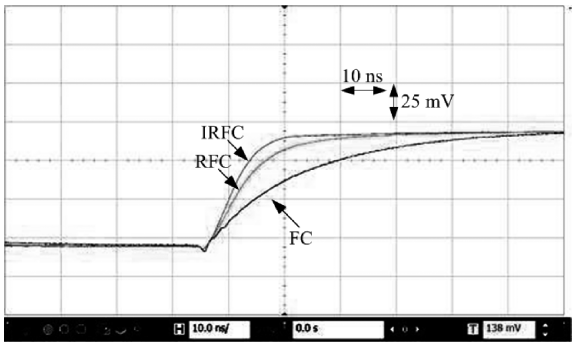

Fig. 8. Measured settling behavior.

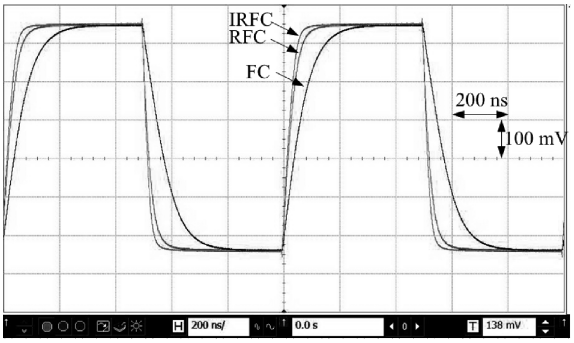

Fig. 9. Measured large-signal response.

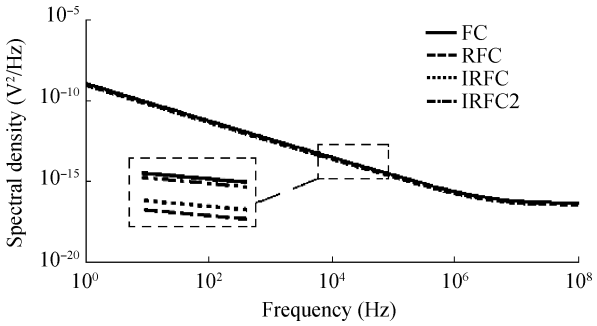

Fig. 10. Simulated input-referred noise.

4. Experimental and simulation results

In this work, the IRFC OTA ($p = \alpha = 0.5$) was implemented in SMIC 0.13 μm technology with nominal V_{DD} of 1.2 V to verify the effectiveness of our analysis. For comparison, an FC OTA and an RFC OTA were also implemented. The RFC and IRFC were modified based on the same FC OTA, so three OTAs have the same area ($17 \times 67\ \mu m^2$) and power consumption (360 μW). The OTAs were configured in unit-gain amplifier with a feedback factor of 0.5 (with on-chip RC network where $R_1 = 490$ kΩ and $C_1 = 1$ pF). The micrograph of the chip and test schematic are shown in Figs. 6(a) and 6(b). An off-chip buffer is inserted to drive 50 Ω load of network analyzer. The on-chip load capacitance is 4.5 pF, and the parasitic capacitance of pad and PCB trace is about 0.5 pF, so the effective load is approximately 5.5 pF (including the loading effect of feedback capacitance C_1) for all OTAs.

The measured BWs of FC, RFC and IRFC are 11.7 MHz, 22.9 MHz and 33.5 MHz, respectively (Fig. 7). Thus the GBWs of FC, RFC and IRFC are their close-loop BWs divided by feedback ratio, i.e., 23.4 MHz, 45.8 MHz and 67 MHz, respectively. Compared with FC, the GBW of IRFC is enhanced almost 3 times; while the enhancement is about 1.5 times when compared with RFC. The enhancement is smaller than Eq. (2) because of the finite output impedance, as discussed in Section 2. To measure the settling time, a small signal step, 75 mVpp at 5 MHz, was applied to the amplifiers (Fig. 8). The measured 1% settling times of FC, RFC and IRFC are 64.9 ns, 32.6 ns and 21.4 ns, respectively. To measure slew rate, a large signal step (600 mVpp at 1 MHz) was applied. The transient response to the large signal is shown in Fig. 9, and the measured slew rates of FC, RFC and IRFC are 6.7 V/μs, 17 V/μs and 20.7 V/μs, respectively; that is, the slew rate of IRFC is enhanced 3 times over the FC and 1.2 times over the RFC. In addition, in the transient responses in Figs. 8 and 9, no signs of ringing are observed, so we can conclude that the IRFC with $p = \alpha = 0.5$ does not induce a stability problem, which was also confirmed by phase margin simulation. Also, with greater transconductance and output impedance, gain enhancement of IRFC over RFC and FC was observed in simulation.

The noise performances of the fabricated IRFC, RFC and FC are characterized by simulation. In addition, a noise-optimized IRFC (IRFC2) with $p = 0.2$ and $\alpha = 3/8$ was also simulated to verify our analysis in Section 3. The spectral density is shown in Fig. 10. The integrated input-referred noise (1 Hz to 100 MHz) of IRFC, RFC, FC and IRFC2 is 98.5 μVrms, 95.5 μVrms, 110.0 μVrms and 107.7 μVrms, respectively. The noise-optimized IRFC has the same noise performance as FC, but it consumes about 40% less current and has about 200% GBW and slew rate.

Another important performance of OTA is linearity. The linearity was simulated by inputting 200 mVpp signal around 1 MHz (100 mVpp at 950 kHz and 100 mVpp at 1.05 MHz) at the V_{in} node of Fig. 6(b) and observing output. Linearity is mainly decided by loop gain: with the large loop gain, the non-linearity is greatly reduced by feedback. Another influential factor is cross-coupling, since non-linearity item can be cancelled with proper cross-coupling (i.e., proper parameter p and α here)[8]. Though the loop gain of IRFC2 is smaller than IRFC at 1 MHz, proper p and α make its third-order intermodulation distortion (IMD3) performance is better (74 dBc) than IRFC (70 dBc). However, FC has the smallest loop gain at 1 MHz and is not cross-coupled, so its IMD3 is the worst (59.1 dBc).

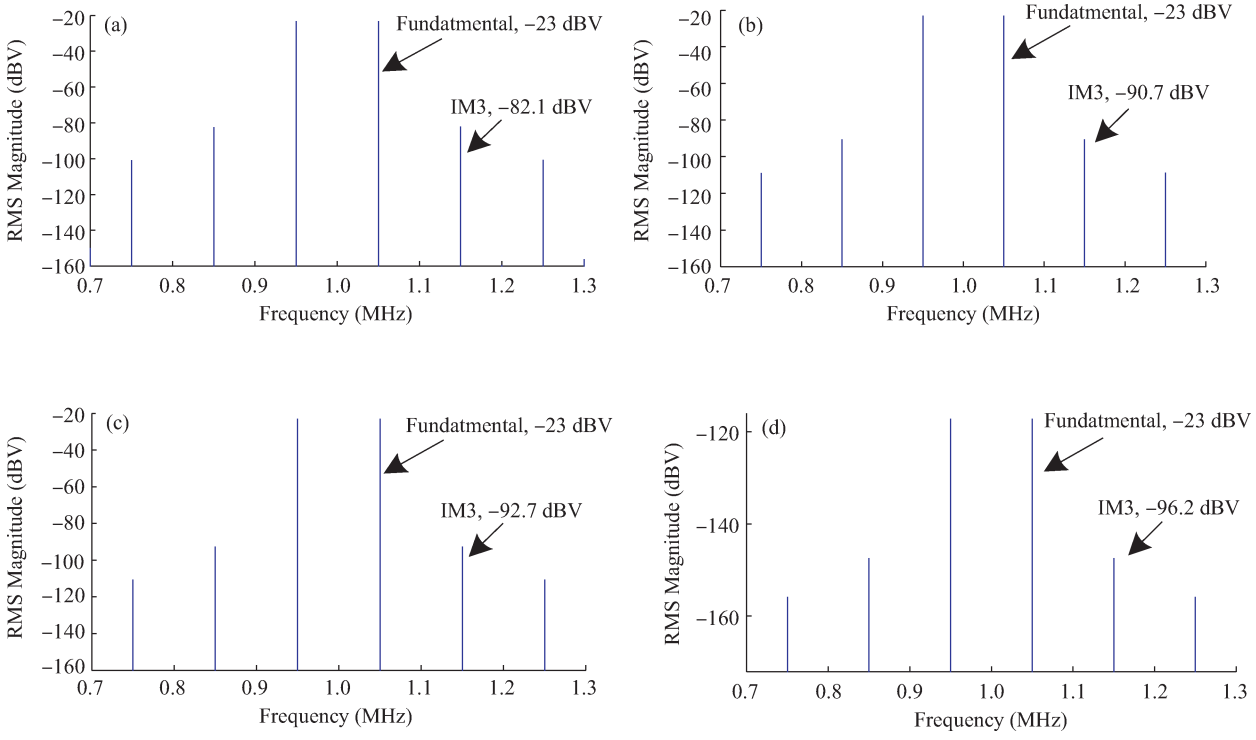

Fig. 11. Simulated IM3 of (a) FC, (b) RFC, (c) IRFC, and (d) IRFC2.

Table 1. Performance summary.

Parameter	FC	RFC	IRFC	IRFC2
Supply voltage (V)	1.2	1.2	1.2	1.2
Current (μA)	300 (300*)	300 (300*)	300 (300*)	185*
Area (μm^2)	17 × 67	17 × 67	17 × 67	N/A
Capacitive load (pF)	5.5	5.5	5.5	5.5
DC gain (dB)*	53.61	60.2	64.9	66.1
GBW (MHz)	23.4 (24.0*)	45.8 (48.0*)	67 (76.2*)	44.9*
Open loop phase margin (degree)*	87.8	83.6	72.7	80.1
Slew rate (V/μs)	6.7 (8.1*)	17 (20.3*)	20.7 (21.2*)	12.7*
Integrated input-referred noise (1 Hz to 100 MHz) (μVrms)*	110.0	95.5	98.5	107.7
IMD3 (200 mVpp at 1 MHz) (dBc)*	59.1	67.7	69.7	73.2
FoM1 (MHz · pF/mA)	429 (440*)	839.7 (889.7*)	1228.3 (1397*)	1335*
FoM2 ((V/μs)pF/mA)	122.8 (148.5*)	311.7 (372.2*)	379.5 (388.7*)	377.6*

* Simulation result.

The simulated IM3 is shown in Fig. 11.

The measurement and simulation results of OTAs are summarized in Table 1. To compare the overall performance, two commonly used figures of merits (FoM) are calculated. The expressions of FoMs are:

$$\mathrm{FoM}_1 = \frac{\mathrm{GBW} \cdot C_\mathrm{L}}{I_\mathrm{D}}, \quad \mathrm{FoM}_2 = \frac{\mathrm{SR} \cdot C_\mathrm{L}}{I_\mathrm{D}}. \tag{15}$$

Compared with FC, IRFC and IRFC2 can achieve about 3 times and enhancement in both FoMs; while the enhancement over RFC is 1.5 times over FoM_1 and 1.2 times over FoM_2. The enhancement in FoMs shows a significant performance improvement of IRFC.

5. Conclusion

A novel transconductance-enhanced FC OTA, IRFC, is analyzed and implemented. Analysis shows that the IRFC is a more general type of FC OTA, and expressions of IRFC are proved to be effective for both RFC and FC OTA. It has been demonstrated by measurement results that the modification can achieve almost 3 times enhancement in FoMs over conventional FC OTA while maintaining enough stability. In addition, simulation shows that noise-optimized IRFC can achieve similar noise performance with FC but with 40% less current and 2x GBW and slew rate. The theoretical results are in good agreement with experimental and simulation results.

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