A novel high speed lateral IGBT with a self-driven second gate

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Abstract: A novel lateral IGBT with a second gate on the emitter portion is presented. A PMOS transistor, driven by the proposed device itself, is used to short the PN junction at the emitter while turned off. Low on state voltage and fast turn off speed are obtained without side-effects such as snapback I–V characteristics and difficulties of process complexity. Numerical simulation results show a drop of fall time from 120 to 12 ns and no increase of on state voltage.

Key words: lateral IGBT; second gate; high speed

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1. Introduction

Insulated gate bipolar transistors (IGBTs) are widely used because of the combination of MOS controlled switching capability and low on state voltage[1, 2]. However, IGBTs produce a current tailing effect during turn off due to the injection of minority carriers of the forward-biased PN junction at the emitter and a long turn off time. Therefore, large turn off losses occur as a result[3]. Many methods are used to reduce turn off time but all these require costs such as increase of on state voltage, additional control terminal and external driving circuits[4−6]. A low voltage transistor is integrated in a vertical IGBT to short the forward-biased PN junction during turn off to eliminate the tail current and the transistor is turned off during on state to ensure sufficient conductivity modulation in Ref. [7]. Driving circuits for the shorting transistor are also integrated into the same chip. Through this way low on state voltage and fast switching capability are combined together with neither an additional control terminal nor external driving circuits. Such an idea could be used in a lateral IGBT (LIGBT) for high voltage power ICs (HVICs) and some necessary changes of the structure are needed. In Ref. [8] an additional passive gate is used in a LIGBT and a field oxide PMOS transistor (PMOST) is turned on during turn off to eliminate the injection of minority carriers. There are some problems with the LIGBT in Ref. [8] such as an additional pad or wiring over voltage sustaining region being needed, as said in Ref. [9]. Some improvements are made in Ref. [9] but additional area is needed due to the lateral diffusion of the n-well and the introduction of a floating n-region.

In this paper, a LIGBT with a self-driven second gate is presented to solve the problem of tailing current during turn off without any difficulty of process complexity. A shorting PMOST connected parallel to the PN junction at the emitter turns on and off driven by a voltage taken from the drift region. That means neither additional control terminal nor external driving circuits are needed. Its source–gate voltage varies from near zero voltage during on state to a certain value during turn off. This paper also presents numerical simulation results by MEDICI[10].

2. Structure and operation of the proposed LIGBT

Figure 1 illustrates the schematic cross-section of the proposed LIGBT and its equivalent circuit. A p-layer and an n-well satisfy the optimum variational lateral doping (VLD) condition[11]. The VLD LIGBT is believed to be capable of sustaining larger voltage in a shorter drift region length and conducting a higher current density[12]. High n-well doping decreases the on state voltage more and works as a buffer layer to prevent the depletion region to get to the emitter.

A shorting PMOST, the gate of which is connected to the end of the p-layer in the drift region, connects the emitter and the floating electrode. The PMOST is turned off during on state to ensure sufficient conductivity modulation. It is turned on during turn off to short the forward-biased PN junction at the emitter and translate electron current to emitter without minority carrier injection such as an LDMOS. The doping dose of the p-layer in region A can be varied to get different gate voltages of the shorting PMOST.

When the LIGBT is off, the p-layer is gradually depleted and holes in the p-layer flow to the collector as the emitter voltage goes up. The p-layer in region A will be depleted completely at some value of the emitter voltage and a barrier is built up between the holes in the p-island right to region A and the p-layer left to it. The holes in the p-island will stop flowing to the emitter due to the resistance of the barrier and the voltage between the p-island and the n-well below it stops growing. This means the source–gate voltage V_{SG2} of the shorting PMOST is fixed at a certain value. The p-layer left to region A continues to deplete to sustain the emitter voltage. Because a fixed source–gate voltage V_{SG2} can be obtained, the shorting PMOST can use the same thin gate oxide as used in the CMOS control circuits, instead of the field oxide used in Refs. [8, 9]. The benefit of using a thin gate oxide is that the threshold voltage can be lowered down to obtain a better on-state char-

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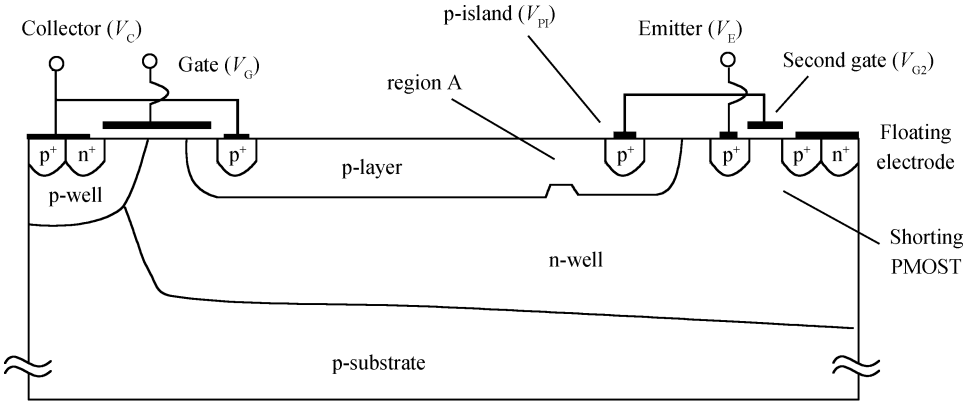
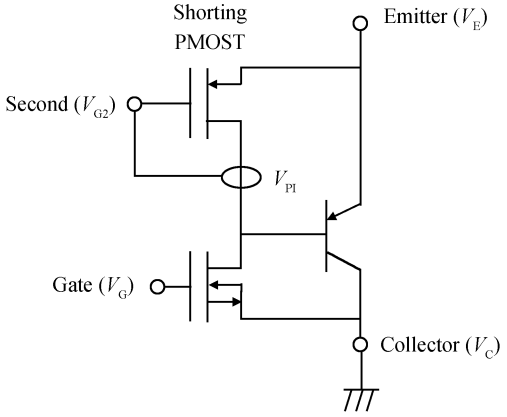


(a) Schematic cross-section of the proposed LIGBT



(b) Equivalent circuit of the proposed LIGBT

Fig. 1. (a) Schematic cross-section and (b) equivalent circuit of the proposed LIGBT.

acteristic of the PMOST and p-plus can be used to form the source and drain of the PMOST, instead of the p-layer used in Refs. [8, 9], reducing the on resistance further.

When the gate voltage is applied to the LIGBT, it turns on and holes are injected into the drift region. Part of the hole current is absorbed by the p-layer and flows to the collector across the p-layer. V_{G2}, the gate voltage of the shorting PMOST, is close to the emitter voltage due to the voltage drop of the hole current flowing across the p-layer. The threshold voltage of the PMOST should be larger than 0.7 V. The reason is when the emitter voltage is below 0.7 V, no hole is injected into the drift region and V_{G2} is 0 V.

If the PMOST turns on before the injection of holes, the PN junction at the emitter will be shorted and there will be no conductivity modulation. The LIGBT will behave like a LDMOS then. Threshold voltage adjustment of the PMOST could be achieved by using the threshold voltage adjustment in the CMOS technology of the low voltage control circuits or changing the doping concentration of n-well under the shorting PMOST.

3. Numerical simulation and discussion

For the convenience of illustration, the proposed structure with $V_{G2} = V_{PI}$ is referred as LIGBT A, the proposed structure with $V_{G2} = V_E$ is referred as LIGBT B, the structure in Ref. [9] is referred as LIGBT C, the proposed structure with $V_{G2} = V_{PI}$ and the threshold voltage of the shorting PMOST lower than 0.7 V is referred as LIGBT D, as can be seen in Fig. 4, 800 V breakdown voltage is obtained for LIGBT A in a p-substrate of 65 Ω·cm resistivity as shown in Fig. 2. The breakdown voltage is 650 V for LIGBT B. In the $V_{G2} = V_{PI}$ condition, the PMOST turns on as V_E increases and the breakdown of LIGBT A is like a LDMOS. While $V_{G2} = V_E$, the PMOST is off all the time. The breakdown voltage is determined by a PNP transistor and it is lower than the one when $V_{G2} = V_{PI}$ because of the current amplification effect of the PNP transistor.

Different source–gate voltages of the shorting PMOST are achieved by varying the doping dose of the p-layer in region A, as shown in Fig. 3. The lower the doping dose of the p-layer in region A is, the sooner the p-layer in region A depletes completely and the barrier is built up. After that, holes in the p-island stop flowing to the collector. The voltage of the p-island starts to increase following V_E and a constant source–gate voltage V_{SG2} of the PMOST is achieved.

The I–V characteristics of LIGBT A, LIGBT B, LIGBT C and LIGBT D are compared in Fig. 4. The gate voltage applied is 6 V. The minority carrier lifetime in the simulation is 10 μs. The I–V characteristics for LIGBT A and LIGBT B are the same, which means the introduction of the shorting PMOST

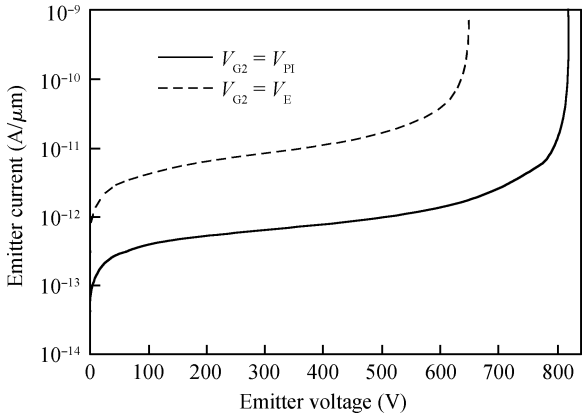


Fig. 2. Breakdown characteristics of the proposed LIGBT with $V_{G2} = V_{PI}$ and $V_{G2} = V_E$.

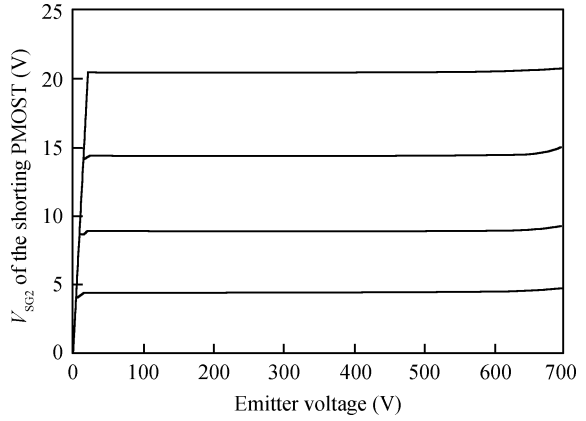


Fig. 3. V_{SG2} of the shorting PMOST under different doses of the p-layer in region A. The dose of the p-layer in region A is a ratio of the dose of the p-layer in other places. The ratio is 1, 0.9, 0.8 and 0.7 from top to bottom, 0.9 is chosen in the design.

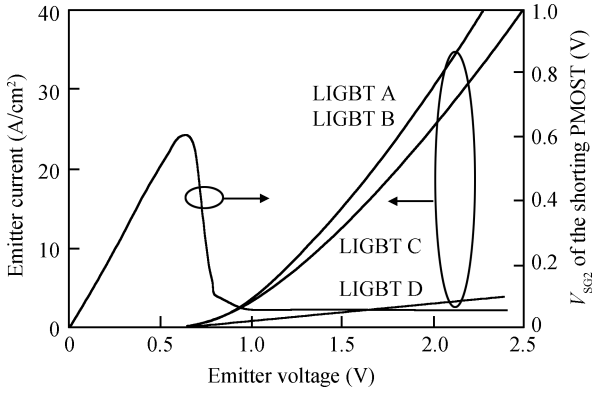


Fig. 4. Forward I–V characteristics of LIGBT A, LIGBT B, LIGBT C, LIGBT D and V_{SG2} of the shorting PMOST of LIGBT A during on state. The curves for LIGBT A and LIGBT B overlap in the figure.

does not decrease the forward current conducting capability. The PMOST of LIGBT A is off during on state, which can be verified by the source–gate voltage of the PMOST, as shown in Fig. 4. V_{SG2} follows the emitter voltage when below 0.7 V and drops down quickly after the injection of minority carriers into the drift region. The current for LIGBT C at a same

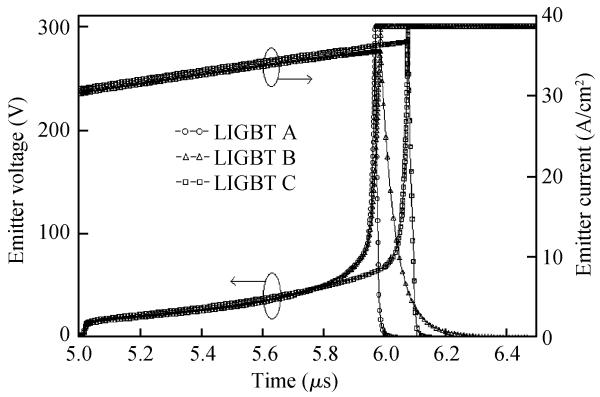


Fig. 5. Switching current and voltage transient waveforms for LIGBT A, LIGBT B and LIGBT C under CIS condition.

emitter voltage is smaller due to the larger silicon area needed for LIGBT C. For LIGBT D, the PMOST turns on before the injection of holes and the LIGBT behaves like a LDMOS.

Figure 5 shows simulated switching current and voltage transient waveforms for LIGBT A, LIGBT B and LIGBT C under clamped inductive switching (CIS) conditions. The applied gate voltage is 6 V and is removed at $t = 5$ μs. The minority carrier lifetime in the simulation is 10 μs. The PMOST turns on in proportion to V_E increasing. Then electrons in the drift region flow to the floating electrode to combine with holes from the emitter instead of flowing through the PN junction at the emitter. Therefore no minority carriers are injected into the drift region then and the current tailing effect is eliminated. The fall time drastically decreases from 120 to 12 ns by the action of the shorting PMOST. The fall time for LIGBT C is 22 ns. The fall time for LIGBT C is larger than LIGBT A because the threshold voltage of the passive PMOST in LIGBTC is much larger than the one in LIGBT A thus the capability of conducting current of the PMOST in LIGBT C is worse. The emitter voltage rising time for LIGBT C is 200 ns longer than LIGBT A. This is because of the larger PN junction capacitance caused by the n-well in LIGBT C and more minority carriers injected into the drift region. The total turn off losses for LIGBT A, LIGBT B and LIGBT C are 1.43, 2 and 1.88 mJ/cm^2. 28.5% reduction of turn off loss is achieved compared with LIGBT B and 24% compared with LIGBT C through the introduction of a shorting PMOST driven by a p-island in the drift region.

4. Conclusion

A novel LIGBT structure with a shorting PMOST driven by a p-island in the drift region has been presented. As the shorting PMOST turns on and off automatically while in turn off and on state, low on state voltage and fast switching capability are combined in one structure. Simulated results show no increase of on state voltage and a drastic drop of fall time for emitter current from 120 to 12 ns compared to one with the shorting PMOST turned off all the time. A drop of turn off loss from 1.88 to 1.43 mJ/cm^2 is obtained compared to the LIGBT in Ref. [9].

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