An output amplitude configurable wideband automatic gain control with high gain step accuracy*

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Abstract: An output amplitude configurable wideband automatic gain control (AGC) with high gain step accuracy for the GNSS receiver is presented. The amplitude of an AGC is configurable in order to cooperate with baseband chips to achieve interference suppression and be compatible with different full range ADCs. And what's more, the gain-boosting technology is introduced and the circuit is improved to increase the step accuracy. A zero, which is composed by the source feedback resistance and the source capacity, is introduced to compensate for the pole. The AGC is fabricated in a 0.18 μm CMOS process. The AGC shows a 62 dB gain control range by 1 dB each step with a gain error of less than 0.2 dB. The AGC provides 3 dB bandwidth larger than 80 MHz and the overall power consumption is less than 1.8 mA, and the die area is 800 × 300 μm^2.

Key words: automatic gain control; output amplitude configurable; high gain step accuracy
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1. Introduction

Automatic gain control (AGC) is an essential function in Global Navigation Satellite System (GNSS) receivers. As long as a receiver is required in a GNSS, the signal strength depends on the propagation path attenuation which will increase the processing difficulties of the following signal processing units in the receiver[1, 2]. The task of the AGC loop is to adjust the gain depending on the receiving signal strength automatically, such that the strength of the signal collected by the signal processing units in baseband modules appears to be close to a constant level no matter the size of the propagation path attenuation.

Many analog exponential function generators[3–5] and other approximation methods[6, 7] are proposed, but their gain errors and power dissipations are not good enough for GNSS applications. What is more, to achieve maximum compatibility toward a multitude of baseband chips, an AGC with a dB-linear digital gain control amplifier, which can also be controlled by a baseband chip, is needed. If we use the analog-controlled VGA, an extra digital to analog converter must be added that is still operating on some discrete points. The gain errors cannot be optimized on these points easily.

As more and more GNSSs are developed, different signal bandwidths are required by different systems. To meet the demands of, and to avoid interference between different systems, the receiver must set a higher IF frequency and take advantage of tunable filters to meet the requirements of different systems. In order to be compatible with all GNSS requirements, the IF amplifier has to provide sufficient bandwidth to ensure that it will not affect the bandwidth of the tunable filter.

During the receiving of a GNSS signal, there are many interfering signals, in which continuous wave interference is particularly serious. A traditional method of suppression[8] involves changing the A/D full-range level to change the quantization of the noise level to achieve continuous-wave interference suppression. There is a new approach that is modifying the full range of AGCs that does not change the A/D to achieve continuous-wave interference suppression. What is more, to make the RF chip cope with different baseband chips, the configurable full range of an AGC output is also needed.

There are many digital gain control amplifiers (DGA)[9]. However, a traditional closed loop digital gain control amplifier with switchable resistive feedback has the critical disadvantage of high power consumption. Several studies[10–13] have been employed in digital gain control amplifier architectures, whose gain still depends on input transconductance and the sensitive gain-steps to process variation due to input transconductance.

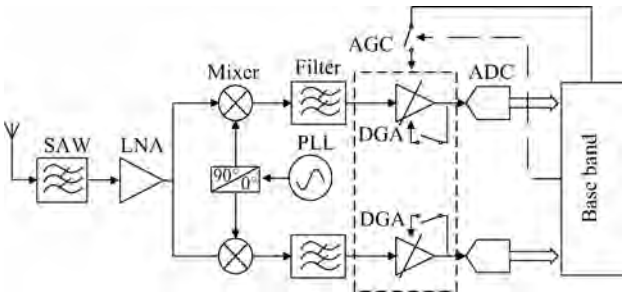

Fig. 1. A multi-band multimode GNSS receiver.

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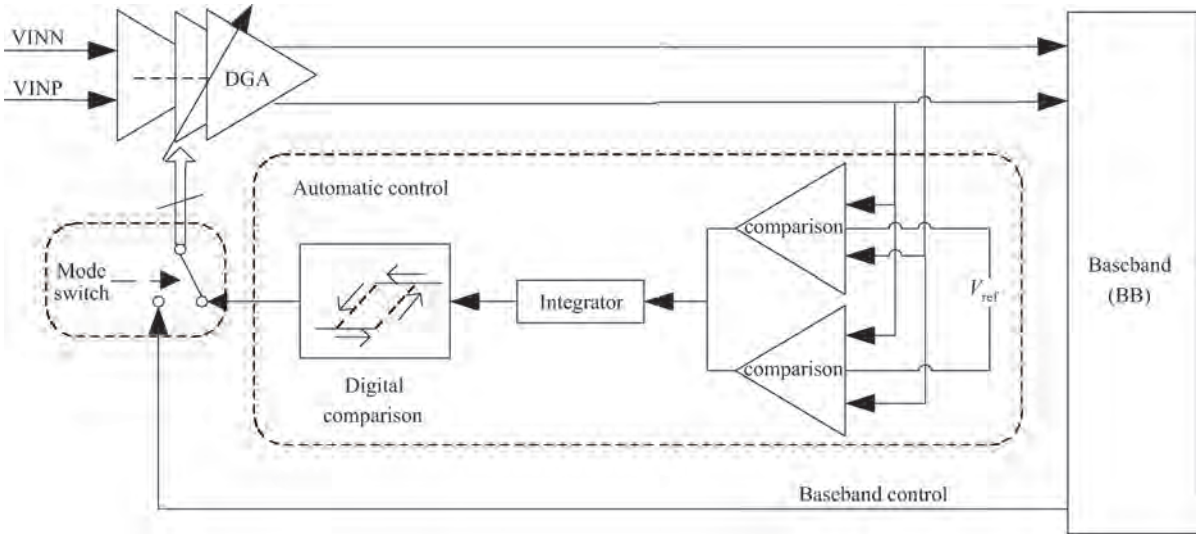

Fig. 2. Architecture of the proposed AGC loop.

Based on the above, an output amplitude configurable wideband automatic gain control with high gain step accuracy is presented. Figure 1 shows a diagram of a multi-mode GNSS receiver where the proposed AGC can be used. Under automatic control mode, the AGC can adjust the gain automatically; under baseband control mode, the control signal of the digital gain control amplifier is generated from the baseband chip.

2. System architecture

The proposed output amplitude configurable wideband automatic gain control with high gain step accuracy block is shown in Fig. 2. It consists of a DGA, an improved digital gain control unit and a mode switch circuit. When the AGC is set under automatic control mode, the baseband chip turns on the switch connected to the digital comparison; while the digital control feedback loop is shut down, and the control code of the DGA is generated from the output of the digital comparison. The signal amplified by the DGA is compared with the reference voltage, and then the output of comparisons is accumulated in a digital integrator. Finally the output of the digital integrator is compared with a set number in a hysteresis digital comparison whose output controls the gain of the DGA until the amplitude of the output signal satisfies the set criterion. When the AGC is set under baseband control mode, the baseband chip turns on the switch connected to the baseband chip, while the automatic feedback loop is shut down. Now the gain control of the DGA circuit is provided by the baseband chip.

The amplified signal is compared with the voltage of the reference and the output of the comparator is shown in Fig. 3. The ratio between the reference voltage and the peak signal determines the ratio of the high voltage of the comparator output throughout the signal cycle and the ratio can be expressed as:

$$P = \frac{\frac{\pi}{2} - \arcsin\frac{V_{\mathrm{REF}}}{V_{\mathrm{M}}}}{\frac{\pi}{2}}, \tag{1}$$

where V_{REF} is the reference voltage and V_{M} is the amplitude of the input signal. The clock signal is imported to sample the output of the comparator and the ratio of high voltage is statistics. If the statistics period is 512 clock cycles, the value of the sample voltage which is larger than the reference voltage is

$$N = \sum_{n=1}^{512} a_1 + a_2 + a_3 + \cdots a_i + \cdots + a_{512}, \tag{2}$$

$a_1 = 0$, if the output of the comparator is 0 in time i,
$a_1 = 1$, if the output of comparator is 1 in time i.

N, which stands for the ratio of the high voltage in the cycle, is compared with N_{a}, which is the preset voltage. If N is larger than N_{a}, the digital module reduces the gain of the digital control amplifier. If N is smaller than N_{a}, the digital module enlarges the gain of the digital control amplifier. When N is equal to N_{a}, the output amplitude is stable and the equation $N_{\mathrm{a}}/512 = P$ is satisfied and the amplitude of the output signal can be expressed as:

$$V_{\mathrm{M}} = V_{\mathrm{REF}} \sin[(1 - N_{\mathrm{a}}/512) \times \pi/2]. \tag{3}$$

From the above formula, the amplitude of the output signal can be controlled by setting N_{a} between 0 and 512. In this design, the output amplitude is limited by the OIP3 and the control ranges from 336 to 800 mV, while V_{REF} is 370 mV.

As the amplitude of the input signal changes constantly and N cannot be the same as N_{a} every time, the hysteresis comparator is introduced. The hysteresis range is set from N_{L} to N_{H}, where N_{a} is smaller than N_{H} but larger than N_{L}. If the amplitude of the input signal is in the area between N_{L} and N_{H}, the gain of the amplifier is unchanged to avoid introducing other digital noise.

Since it is highly difficult to use a single stage DGA to realize a very wide dynamic range of gain tuning, we propose to utilize five stages of individual DGAs to attain the required 64 dB range, wide bandwidth, and decibel linearity. As shown in Fig. 3, the range of the first and second DGA is 0 to 24 dB with an 8 dB gain step; the third and fourth stage is aimed at the 3 to 9 dB range with a 2-dB gain step; and the last stage is 8 to 9 dB with a 1 dB gain step.

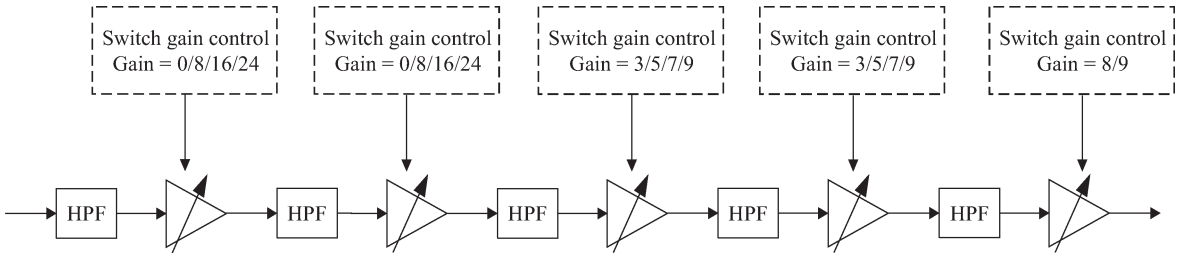

Fig. 3. Architecture of the proposed DGA circuit.

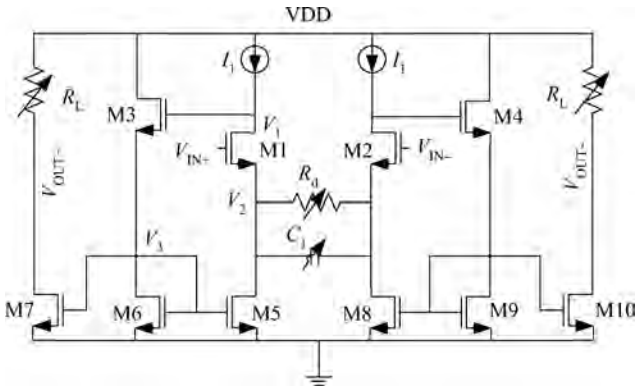

Fig. 4. Schematic of the DGA.

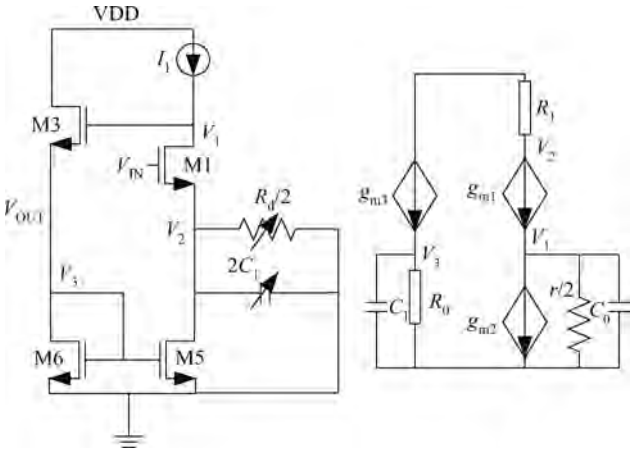

Fig. 5. Gain-boosting circuit and the corresponding small signal model.

3. Circuit design

A portion of the AGC circuits in Fig. 2, including the digital gain amplifier, automatic control circuit and mode switch, is designed based on the 0.18 μm CMOS process.

3.1. Digital gain amplifier

The gain of the traditional structure of the digital gain amplifier circuit[14] is determined by the ratio of the load resistance and source feedback resistance. The main drawback is that the gain is determined by the following formula:

$$A_{\rm v} = g_{\rm m} R_{\rm L}/(1 + g_{\rm m} r), \tag{4}$$

where r is the source feedback resistance. To ensure the accuracy of the gain step, we have to enhance transconductance as much as possible, which consumes too much power and limits the size of the load resistance. This paper introduces a gain-boosting structure[15] and improves the structure by adding a buffer circuit, which improves the driving ability and extends the circuit bandwidth. What is more, the zero compensation technology, which uses the parallel source resistance and source capacitor to generate the zero and compensation for the first pole of the circuit. The whole circuit is shown in Fig. 4.

The gain-boosting part and the corresponding small signal model are shown in Fig. 5, from which we can derive the relationship between the input and output voltage:

$$V_{\rm out} = \frac{(-R_1 g_{\rm m1}) V_{\rm in}}{1 + (A + g_{\rm m1}) r/2}, \quad A = g_{\rm m2} R_1 g_{\rm m1} \frac{g_{\rm m3} R_0}{1 + g_{\rm m3} R_0}, \tag{5}$$

where R_0 and R_1 are equivalent resistances of the tail current source I1, M6 and $g_{{\rm m}i}$ is the transconductance of the corresponding MOSFET. The whole circuit gain can be derived as follows:

$$V_0 = \frac{(R_1 g_{\rm m4} g_{\rm m1} R_{\rm L}) V_{\rm in}}{1 + g_{\rm m2} R_1 g_{\rm m1} r/2} = \frac{g_{\rm m4} R_{\rm L} V_{\rm in}}{g_{\rm m2} r/2}, \tag{6}$$

where $R_{\rm L}$ is the load resistance and r is the source feedback resistance. Compared with the original gain formulator, transconductance has been enhanced by $g_{\rm m2} R_1$ and accuracy is improved.

To extend the bandwidth of the circuit, the zero is introduced which is composed from capacitance C_1 and the source feedback resistance $R_{\rm d}$. The frequency response of the whole circuit can be derived as follows:

$$\begin{aligned} V_0({\rm j}w) &= \frac{(R_1 g_{\rm m4} R_{\rm L} g_{\rm m1}) V_{\rm in}}{1 + g_{\rm m2} R_1 g_{\rm m1} (r/2//1/{\rm j}w C_1)} \frac{1}{1 + {\rm j}w R_{\rm L} C_{\rm gN}} \\ &\quad \times \frac{1}{1 + {\rm j}w C_{\rm gg}/g_{\rm m3}} \\ &= \frac{g_{\rm m4} R_{\rm L} V_{\rm in} (1 + {\rm j}r w C_1)}{g_{\rm m2} r/2} \\ &\quad \times \frac{1}{1 + {\rm j}w R_{\rm L} C_{\rm gN}} \frac{1}{1 + {\rm j}w C_{\rm gg}/g_{\rm m3}}, \end{aligned} \tag{7}$$

where $C_{\rm gN}$ is the equivalent capacitance of the next stage and $C_{\rm gg}$ is the capacitance of M4. The main pole in the circuit is determined by$R_{\rm L} C_{\rm gN}$, which can be compensated for by the zero rC_1.

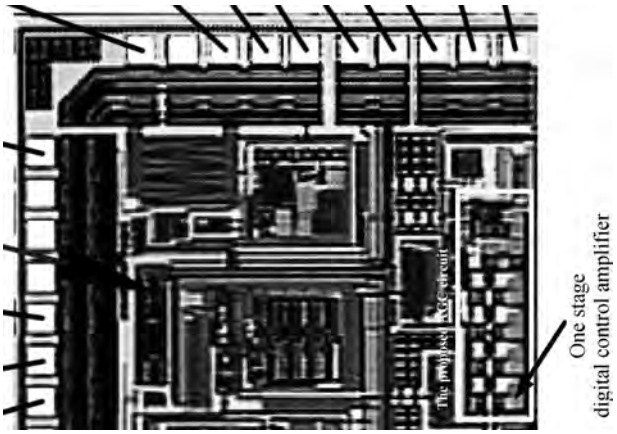

Fig. 6. Die micrograph.

The gain can be adjusted by changing the load resistance or the source feedback resistance. As the two stages have a larger gain step, the gain is adjusted by changing the source feedback resistance and the gain in the three behind stages is adjusted by changing the load resistance. To maintain the zero compensating the pole, capacitance C_1 is changing with the load and source resistance.

3.2. Automatic control circuit

The automatic control circuit consists of two comparators, a digital integrator and a digital hysteresis comparator.

The comparator consists of three parts: the preamplifier, the positive feedback latched circuit and the output buffer. The preamplifier plays a key role in the comparator, which can reduce the input-referred offset and kickback noise of the clocked comparators. If the preamplifier has a high voltage gain, the offset voltage is dominated by the preamplifier, which can be given by[16]

$$V_{\rm OS} = \frac{V_{\rm GS} - V_{\rm th}}{2}\left[\frac{\Delta(W/L)}{W/L} + \frac{\Delta R_{\rm D}}{R_{\rm D}}\right] - \Delta V_{\rm th}, \qquad (8)$$

where ΔW, $\Delta R_{\rm D}$ and $\Delta V_{\rm th}$ are technology mismatch parameters. The most direct way to reduce the offset voltage of the preamplifier is to increase the size of the device while maintaining the gain of the preamplifier and keeping W/L unchanged[17].

A 9 bit counter is used as an integrator. The counter counts the number of ones in every 512 cycle to calculate the high voltage of the comparator output voltage. The result is compared using the hysteresis comparator and the corresponding gain control bits are generated in the hysteresis comparator and fed back to the DGA to provide the desired gain.

4. Measurement results

The wideband automatic gain control circuit with a high precision dB-linear digital gain control amplifier is fabricated in a 0.18 μm single-poly six-metal CMOS process. Figure 6 shows the microphotograph of the fabricated chip. For test purposes, a buffer is added to the output of the AGC block to ensure that the external loading capacitance will not affect the AGC block.

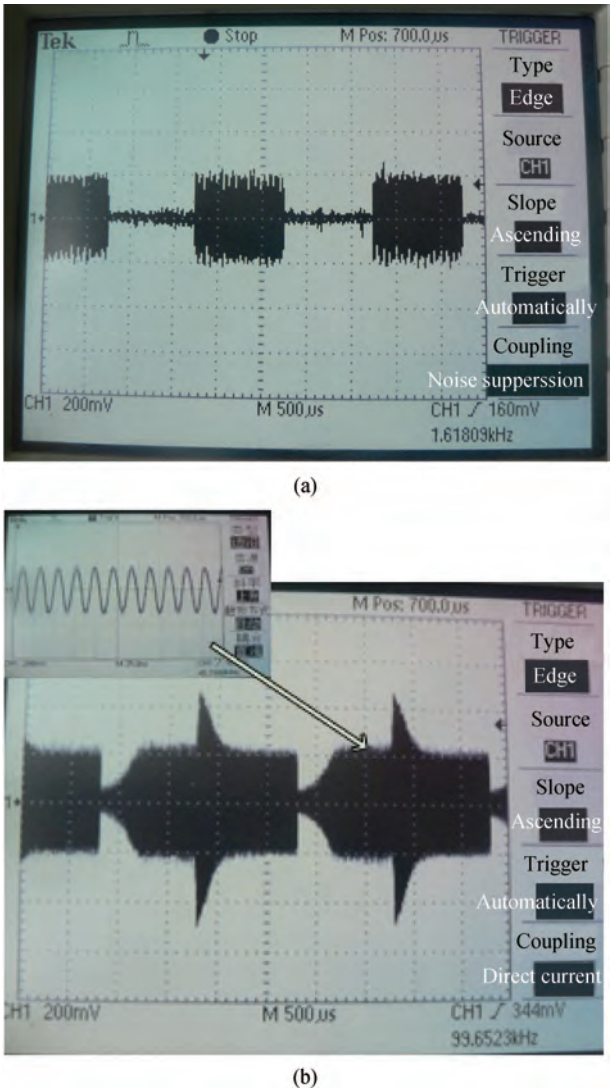

Fig. 7. (a) ASK input signal. (b) Automatic control process and the final stable output of the AGC.

The total current consumption of the AGC is 1.8 mA and the five-stage DGA consumes 1.5 mA current, when the AGC is powered up by a 1.8 V power supply. Therefore, the total power consumption is only 3.24 mW.

4.1. Function of the AGC

To test the function of the AGC, it is configured in automatic control mode and an ASK-modulated signal is imported into the AGC, in which the carrier frequency is 46 MHz and the modulation signal frequency is 500 Hz. The ASK input signal and the test result are shown in Fig. 7. Figure 7(a) shows the ASK input signal, in which the input changes from 20 to 400 mV in a continuous fashion. Figure 7(b) shows the automatic control process. The final stable single-end amplitude shown in the top left corner is about 420 mV.

4.2. Dynamic range

When the AGC is configured in baseband control mode, the gain of the DGA varies with the digital control word. In Fig. 8, the output differential amplitude changes with the input

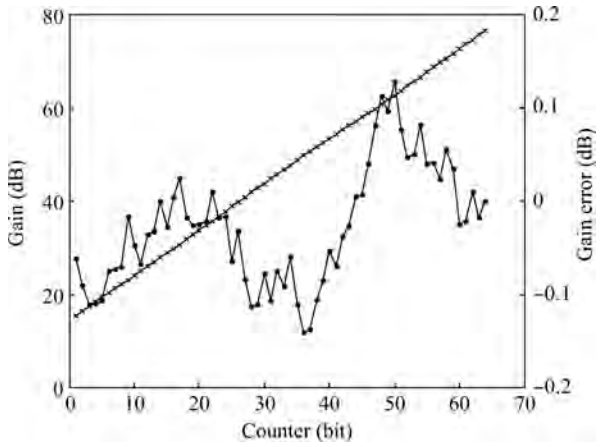

Fig. 8. The measured dynamic range and gain error of the AGC under digital control.

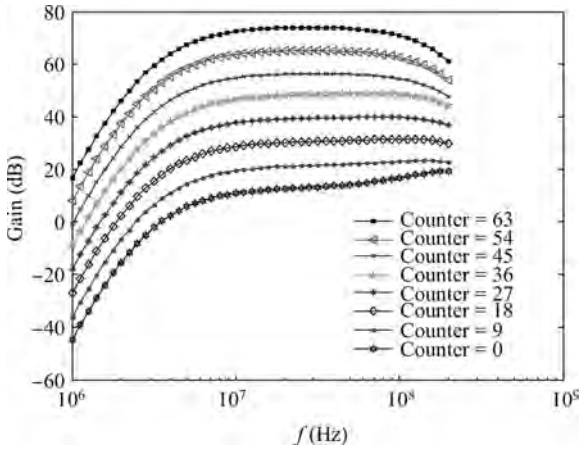

Fig. 9. Frequency response of the DGA under different control counters.

signal by 1 dB, every step corresponding to the digital control word changing from 0 to 62, and the gain error is less than 0.2 dB.

4.3. Frequency response

The AC response of the DGA is measured and shown in Fig. 9 and the band-pass characteristic is evident. The curves from top to bottom correspond to digital control from 63 to 0: the top curve for counter = 63 and the bottom curve for counter = 0. The high pass cutoff frequency is 6 MHz and the –3 dB bandwidth is larger than 80 MHz for all counters (or all levels of gain).

4.4. Input third-order intercept point and the input 1 dB compression point

Figure 10 shows the method using a two-tone test under an input frequency of 46 MHz. The IIP3 of the test result changes with the digital control code and can reach –5 dBm (which can be seen from the figure), while the circuit is configured at minimum gain. The input 1 dB compression point is tested by changing the input signal amplitude under the output signal compressed 1 dB and the test result shows that the P_{1dB} is

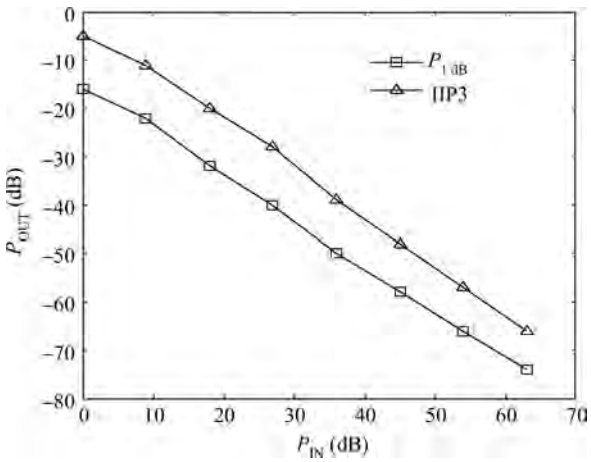

Fig. 10. IIP3 and P1dB of the DGA under different control counters.

Table 1. Overall performance of the proposed AGC.

Parameter	Specification
Maximum gain	79 dB
Die area	0.24 mm^2
Supply voltage	1.8 V
Current consumption	1.8 mA
3 dB bandwidth	[6, 80] MHz
Gain tuning range	62
Gain step accuracy	0.2 dB
IIP3	–5 dBm (minimum gain)

changing from –16 to –74 dBm with the digital control code getting smaller.

The overall AGC performance is summarized in Table 1.

A comparison of the proposed AGC with designs published in the past is given in Table 2. As shown in Table 2, the proposed AGC exhibits a wider bandwidth while consuming less power compared with output amplitude fixed AGC ICs. The proposed AGC has a competitive gain step accuracy compared with other designs.

5. Conclusions

This paper has proposed an output amplitude configurable wide band automatic gain control in order to cooperate with the baseband chips to achieve interference suppression and be compatible with different full range ADCs. The DGA introduces a gain-boosting technology to achieve high gain step accuracy. And what is more, a zero, which is composed by the source feedback resistance and the source capacity, is introduced to compensate for the pole. The stable output amplitude of the AGC is configurable from 336 to 800 mV and the maximum gain is about 79 dB, the dynamic range is 62 dB with a bandwidth greater than 80 MHz. The AGC provides 1 dB every step with a gain error of less than 0.2 dB while operating at 46 MHz. The whole AGC circuit consumes 3.24 mW and provides –5 dBm IIP3 while the gain is set to minimum.

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Table 2. Performance comparison of the proposed and previously reported AGCs.

Parameter	Ref. [4]	Ref. [12]	Ref. [18]	Ref. [19]	This work
Process (μm)	CMOS 0.09	CMOS 0.18	SiGe BiCMOS 0.25	CMOS 0.18	CMOS 0.18
Gain control	Digital	Analogue	Digital	Digital	Digital
Bandwidth (MHz)	[0.1, 30]	[0.8, 18]	[0.068, 95]	[*, 65]	[6, 80]
Gain error	1	*	1	0.5	0.2
Power (mW)	3.6	11.2	13.7	2.16	3.24
Max gain (dB)	71	32	69	32	79
Dynamic range (dB)	71	40	60	54	62
Die area (mm^2)	1.1	0.5625	0.225	0.28	0.24

* not found.

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