AlGaN/GaN HEMTs with 0.2 μm V-gate recesses for X-band application*

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Abstract: AlGaN/GaN HEMTs with 0.2 μm V-gate recesses were developed. The 0.2 μm recess lengths were shrunk from the 0.6 μm designed gate footprint length after isotropic SiN deposition and anisotropic recessed gate dry etching. The AlGaN/GaN HEMTs with 0.2 μm V-gate recesses on sapphire substrates exhibited a current gain cutoff frequency f_t of 35 GHz and a maximum frequency of oscillation f_{max} of 60 GHz. At 10 GHz frequency and 20 V drain bias, the V-gate recess devices exhibited an output power density of 4.44 W/mm with the associated power added efficiency as high as 49%.

Key words: high electron mobility transistors; AlGaN/GaN; V-gate recess

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1. Introduction

High performance AlGaN/GaN HEMTs on sapphire or SiC substrates have been successfully applied to microwave power devices[1, 2]. To date, research has increasingly focused on high frequency applications, for example, X-band or Ku-band[3, 4]. In high frequency applications, the small gate length is critical to device microwave performance[5]. Usually the sub-micrometer gate length is fabricated by using e-beam writers[6], but the gate lithography process of an e-beam writer is complicated and the yield is poor. In addition, e-beam writer equipment is expensive to buy and to maintain. Chu[7] has reported the fabrication of a V-gate HEMT with 12.2 W/mm power density at 10 GHz, and the actual gate footprint length of the device is shrunk from a 1 μm lithography gate length to 0.5 μm after the V-gate-recess etching. In this paper, we describe the process and characteristics of 0.2 μm V-gate recess AlGaN/GaN HEMTs fabricated by 0.6 μm gate footprint lithography and the frequency and power measurement results prove that the device process can be used for X-band microwave power device fabrication.

2. Device structure and fabrication

The AlGaN/GaN HEMT used in this paper was grown on (0001) sapphire substrate in an MOCVD system. The HEMT structure consists of a low-temperature GaN nucleation layer, a 3-μm-thick unintentionally doped GaN buffer layer and an AlGaN barrier layer. The barrier layer consists of a 5-nm un-doped spacer, a 18-nm carrier supplier layer doped at 2×10^{18} cm^{-3}, and a thin un-doped GaN cap layer. Room temperature Hall measurements of the structure yielded an electron sheet density of 1.32×10^{13} cm^{-2} and an electron mobility of 1637 $cm^2/(V{\cdot}s)$.

Device mesa was formed using Cl_2/Ar plasma dry etching in an RIE system followed by the source/drain ohmic contact formation with Ti/Al/Ni/Au (30 nm/180 nm/40 nm/60 nm) annealed at 850 ℃ for 30 s. After 150 nm SiN deposition on the surface of the devices by PECVD, the gate windows with a 0.6 μm footprint length were opened by contact photolithography, and then the 0.6 μm recessed-gate area was treated by CF_4 plasma in an RIE system at an RF plasma bias voltage of 50 V. The recess area of 0.6 μm was etched at 1 nm/s with the depth of 150 nm, and the formation processes are shown in Figs. 1(a) and 1(b). After the formation of 0.6 μm recesses, the second SiN layer of 250 nm was deposited on the surface of the device by PECVD. Isotropic deposition was used to cover the surface

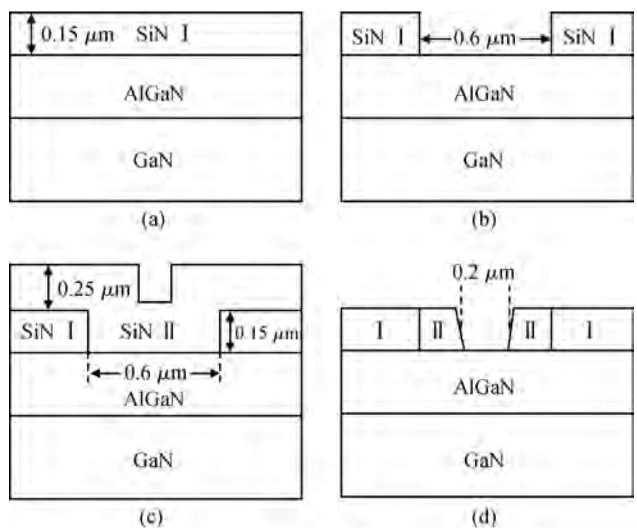

Fig. 1. Process of V-gate recess.

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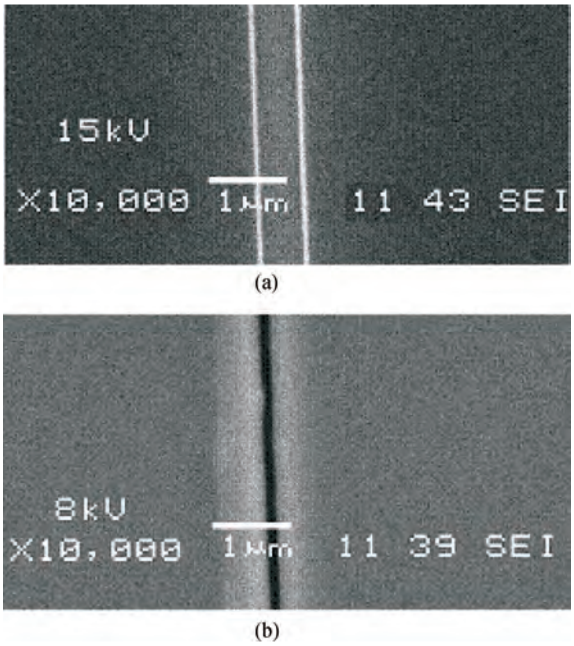

Fig. 2. Gate size of 0.6 μm footprint and V-gate recess.

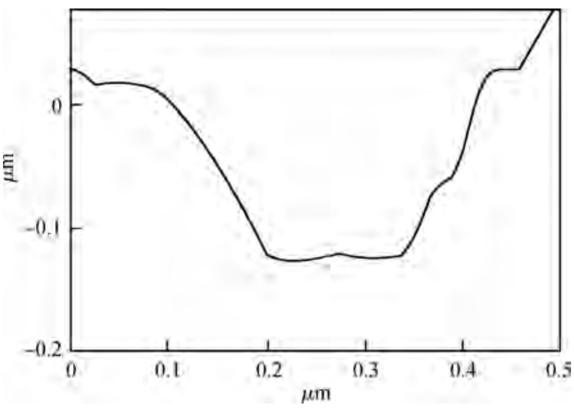

Fig. 3. Cross section of V-gate recess.

with a second SiN layer. Therefore, the SiN layer is then deposited on the sidewall of the recess, thus the 0.6 μm recess length was shrunk. Followed by the 250 nm SiN layer isotropic deposition, the 250 nm SiN layer were etched by anisotropic RIE etching, and the formation process of 0.2 μm V-gate recesses are shown in Figs. 1(c) and 1(d). The etching bias voltage and etching rate of the second SiN layer were same to the first SiN etching. An SEM was used to confirm the size of the V-gate recesses. Figure 2(a) shows the window with a 0.6 μm footprint length and Figure 2(b) shows the 0.2 μm V-gate recess. After isotropic SiN PECVD deposition and anisotropic RIE etching, the gate recess lengths were shrunk obviously. Figure 3 shows the cross section of the V-gate recess, and the V-shape gate cross section was measured by using an AFM.

The Ni/Au (30 nm/200 nm) e-beam evaporation and liftoff were carried out simultaneously to form the gate electrode by using a 0.6 μm footprint length mask. The gate width and source drain distance were 100 μm and 4 μm, respectively. Figure 4 shows the structure of the V-gate recess AlGaN/GaN HEMTs. Using wafer TLM patterns, the contact resistance and

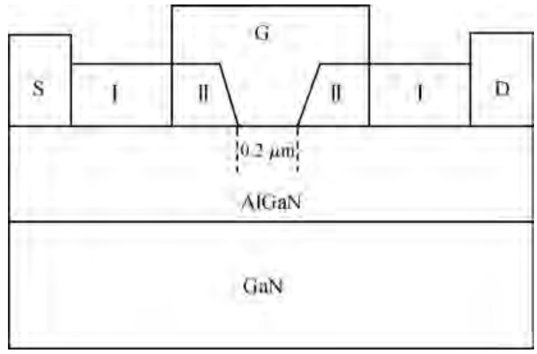

Fig. 4. Cross section for V-gate recess HEMT.

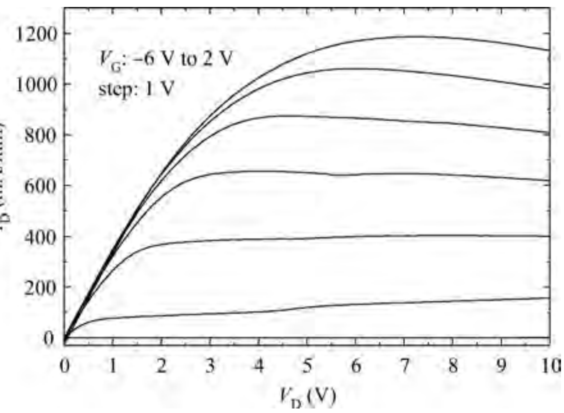

Fig. 5. Output characteristics for V-gate recess HEMTs.

specific contact resistance were measured to be 0.33 Ω·mm and 3.2×10^{-6} Ω·cm^2, respectively. The TLM structures were made on the same HEMT wafer and located regularly around the device. Direct current characteristics and high frequency characteristics were measured by using an HP1500A semiconductor parameter analyzer and an HP8720D network analyzer. Large-signal power measurements were performed by using a load pull system. Device fabrication and measurements were completed at the Key Laboratory of Wide Band gap Semiconductor Materials and Devices of Xidian University.

3. Results and discussion

Figures 5 and 6 show the output and transfer characteristics of the V-gate recess AlGaN/GaN HEMTs, respectively. The maximum drain current density of approximately 1183 mA/mm is reached at V_G of 2 V. The DC transfer characteristics measured at $V_{DS} = 10$ V, and the devices exhibited $g_{m,\max}$ of 252 mS/mm at V_G = –2.8 V and a threshold voltage of –3.7 V.

Figure 7 shows the frequency characteristics of the V-gate recess AlGaN/GaN HEMTs. RF small-signal characterization was performed from 1 to 40 GHz by using an Agilent HP8720D network analyzer. At $V_{gs} = -2.5$ V and $V_{ds} = 10$ V, the current gain cutoff frequency f_T is 35 GHz, and the maximum frequency of oscillation $f_{\max}$ is 60 GHz. The results of RF small-signal characterization indicated that the devices can be applied at X-band.

Large-signal power measurements at 10-GHz frequency

Table 1. DC and microwave power characteristics of different device structures.

Device structure	Gate length (μm)	I_{dmax} (mA/mm)	G_{mmax} (mS/mm)	V_{th} (V)	f_T (GHz)	f_{max} (GHz)	Power density (W/mm)	B_R (V)
Conventional HEMT	0.6	1157	226	−4.1	19	32	3.69 @ 4 GHz	90–100
V-gate recess HEMT	0.2	1183	252	−3.7	35	60	4.44 @ 10 GHz	60–70

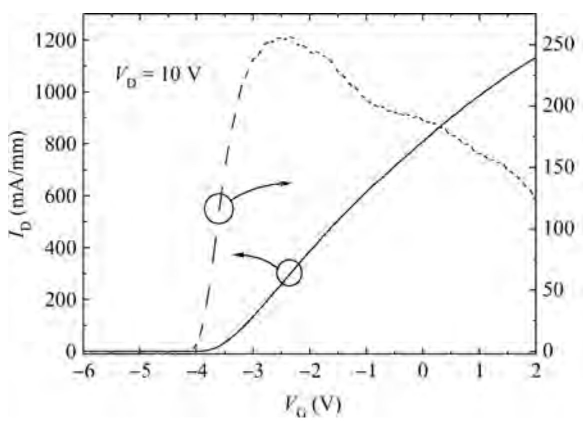

Fig. 6. Transfer characteristics for V-gate recess HEMTs.

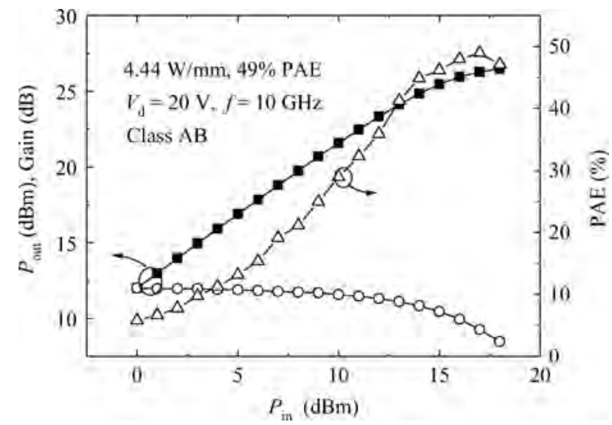

Fig. 8. Power sweep curves for V-gate recess HEMTs.

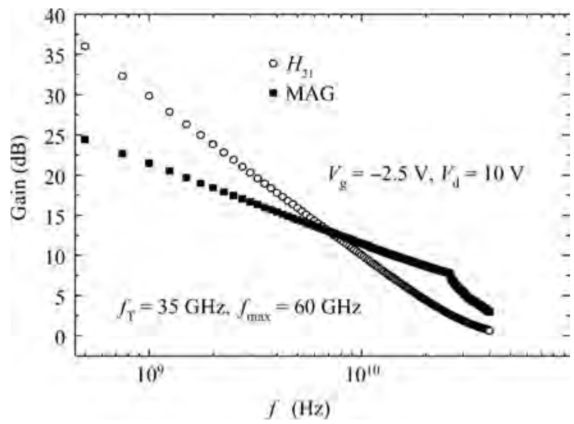

Fig. 7. RF small-signal characteristics for V-gate recess HEMTs.

were performed using a load pull system. The class AB power sweep curves at a drain bias of 20 V are shown in Fig. 8. A power density of 4.44 W/mm with the associated power added efficiency (PAE) as high as 49% was obtained. Large-signal power measurements were only performed below 20 V of the drain bias due to the weak dissipating heat capability of sapphire substrate. If SiC substrates can be used for the devices, the dissipating heat capability and the drain bias would be improved, and therefore better large-signal power results could be obtained.

Table 1 shows the different characteristics of different device structures. The conventional HEMTs have a 0.6 μm gate length and the V-gate recess HEMTs have their 0.2 μm gate length shrunk by a process of isotropic SiN PECVD deposition and anisotropic RIE etching. The same materials were used for conventional HEMTs and V-gate recess HEMTs.

The DC characteristics of the two kinds of device have no obvious differences between them. But the microwave power characteristics of V-gate recess HEMTs improved obviously because of the shrunken gate length. The effective gate length shrank from 0.6 to 0.2 μm, therefore better frequency characteristics can be obtained. Chu[7] has reported the fabrication of a V-gate HEMT with 12.2 W/mm power density at a drain bias of 50 V, because the electric field of the V-shape gate is more uniformly distributed at the gate edge and the peak field was reduced by 40%. However, in our results, the V-gate recess HEMTs have a lower breakdown voltage than conventional HEMTs. The small depletion area size of the 0.2 μm V-gate recess can reduce the breakdown characteristics. More plasma etching in the recessed gate area can generate etching damage, and the surface dislocations caused by etching damage would impact the breakdown voltage of the devices[8]. The results of reverse gate leakage current measurements prove that more plasma etching damage in the recessed gate area could increase the tunneling current of the Schottky gate and then deteriorate breakdown characteristics.

4. Conclusion

We have developed V-gate recess HEMTs on sapphire substrate, which exhibit a power density of 4.44 W/mm with the associated power added efficiency (PAE) as high as 49%. The 0.2 μm V-gate recess AlGaN/GaN HEMTs were fabricated by 0.6 μm gate footprint lithography and a process of isotropic SiN PECVD deposition and anisotropic RIE etching were applied to shrink the 0.6 μm gate footprint to a 0.2 μm V-gate recess. Compared with conventional HEMTs with a 0.6 μm gate footprint, the 0.2 μm V-gate recess HEMTs have better RF small-signal characterization and large-signal power. The device process can be used for X-band microwave power device fabrication.

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