SHA-less architecture with enhanced accuracy for pipelined ADC*

Zhao Lei(赵磊)†, Yang Yintang(杨银堂), Zhu Zhangming(朱樟明), and Liu Lianxi(刘帘羲)

School of Microelectronics, Xidian University, Xi'an 710071, China

Abstract: A new design technique for merging the front-end sample-and-hold amplifier (SHA) into the first multiplying digital-to-analog converter (MDAC) is presented. For reducing the aperture error in the first stage of the pipelined ADC, a symmetrical structure is used in a flash ADC and MDAC. Furthermore, a variable resistor tuning network is placed at the flash input to compensate for different cutoff frequencies of the input impedances of the flash and MDAC. The circuit also has a clear clock phase in the MDAC and separate sampling capacitors in the flash ADC to eliminate the nonlinear charge kickback to the input signal. The proposed circuit, designed using ASMC 0.35-μm BiCMOS technology, occupies an area of 1.4×9 mm^2 and is used as the front-end stage in a 14-bit 125-MS/s pipelined ADC. After the trim circuit is enabled, the measured signal-to-noise ratio is improved from 71.5 to 73.6 dB and the spurious free dynamic range is improved from 80.5 to 83.1 dB with a 30.8 MHz input. The maximum input frequency is up to 150 MHz without steep performance degradations.

Key words: pipelined analog-to-digital converter; sample-and-hold amplifier; SHA-less; aperture error
DOI: 10.1088/1674-4926/33/2/025010 **EEACC:** 2570

1. Introduction

High-speed high-resolution pipelined analog-to-digital converters (ADCs) are widely used in mobile wireless communications systems and instrumentation. Traditionally, the sample-and-hold circuit in pipelined ADCs[1, 2] tends to consist of a sample-and-hold amplifier (SHA). The SHA is used to present a held signal to the first pipeline stage. It, however, consumes a significant amount of power, and contributes substantially to the distortion and noise of the whole ADC. To overcome these disadvantages, a "SHA-less" architecture is employed, as shown in Fig. 1, in which the sample-and-hold (S/H) circuit is integrated in the first multiplying digital-to-analog converter (MDAC), without a dedicated amplifier[3−5].

However, an unbalanced sampling phenomenon when there is no SHA at a typical front-end stage is shown in Fig. 1. During Φ_2, comparators are sampling the threshold voltages, while the MDAC is amplifying the residue voltage of the previous sample. During Φ_1, the analog input signal is connected to both the comparators and the MDAC. A critical sampled signal mismatch occurs at this clock period. The comparators make a bit-decision with V_1 at the falling edge of Φ_{1P} while the MDAC samples the voltage V_2 at phase Φ_1 which causes the voltage difference V_e. This will be increased significantly as a function of input frequency and appears as an offset error at the comparator input which is known as the aperture error[6]. The second issue is that the sample capacitors in the first MDAC and flash receive undesirable remnant charges during the sample mode. These charges vary nonlinearly with the input signal and this nonlinearity degrades the accuracy of the signal conversion process. In this work, a trim circuit, a clear clock phase, and separate sampling capacitors in flash are proposed. Using these methods, the accuracy of the front-end stage is significantly enhanced.

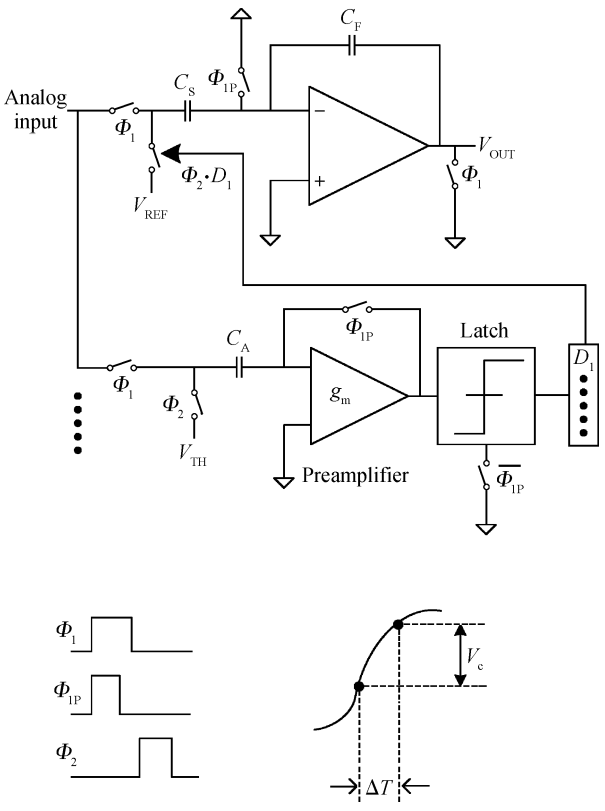

Fig. 1. Conventional SHA-less architecture for the pipeline stage.

* Project supported by the National Natural Science Foundation of China (Nos. 60725415, 60971066, 61006028, 61006028), the National High-Tech R&D Program of China (No. 2009AA01Z258), and the Shaanxi Special Major Technological Innovation Program (No. 2009ZKC02-11).

† Corresponding author. Email: leizhao.ic@gmail.com

Received 21 August 2011, revised manuscript received 20 October 2011

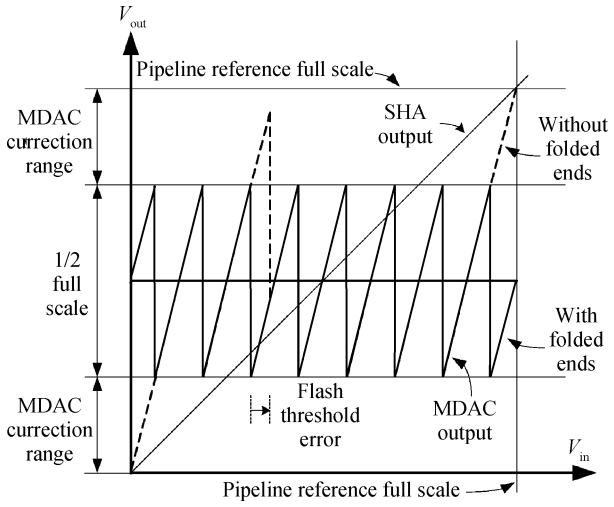

Fig. 2. S/H and 2.5-bit MDAC transfer function comparison.

2. SHA merged with first stage MDAC

Comparing the S/H and the 2.5-bit MDAC transfer function (Fig. 2), it can be seen that the 2.5-bit MDAC has more signal gain with nominally 1/2 the output swing. Therefore, if the front-end S/H is removed and the input signal is sampled directly with the pipeline stage, there is a noise advantage from the higher first stage gain, and a distortion advantage from the reduced swing at the output.

However, this traditional SHA-less architecture has some issues. The first issue is aperture error which is caused by a mismatch of the input networks of the flash and the MDAC of the first stage. Since the flash and the MDAC see the actual input signal, not a held signal, any mismatch between the bandwidth and the sampling instant of these two input networks will result in a mismatch between the sampled values of the MDAC and the flash. The net effect of the mismatches can be approximated as

$$\begin{cases} V_{\text{err\_max}} = \dfrac{1}{2} V_{\text{IN\_FS}} \omega_{\text{IN}} \cdot \Delta T, \\ \Delta T = (t_1 - t_2) + (\tau_1 - \tau_2), \end{cases} \tag{1}$$

where $V_{\text{IN\_FS}}$ is the full range of the input signal; ω_{IN} is the signal frequency of interest; τ_1, τ_2 and t_1, t_2 are the propagation delays and the sampling instants of the flash and MDAC. This mismatch can be corrected by the digital error correction range of the first pipeline stage. In Fig. 2 the 2.5-bit MDAC digital correction range is $\pm\frac{1}{8}V_{\text{REF}}$. If it exceeds that range, errors will go uncorrected causing significant performance degradation.

The second issue is the sample capacitors in the first MDAC and flash, which receive undesirable remnant charges during the sample mode. These charges vary nonlinearly with the input signal and this nonlinearity degrades the accuracy of the signal conversion process. The sampled signal can be mathematically represented as

$$V_{\text{SAMPLED}}(n) = V_{\text{IN}}(nT) + \chi Q(V_{\text{PRE\_SAMPLED}}), \tag{2}$$

where $V_{\text{SAMPLED}}(n)$ is the n-th sample, $V_{\text{PRE\_SAMPLED}}$ is the quantized value of the previous sample which between $-V_{\text{REF}}$ and $+V_{\text{REF}}$, χ is a value between -1 and $+1$ that represents how much of the nonlinear charge kickbacks to the input.

3. The proposed SHA-less architecture and circuit

3.1. SHA-less architecture

To overcome these drawbacks, a novel enhanced accuracy technique for SHA-less is proposed. The SHA-less is realized with the 2.5-bit stage, and the basic circuit is shown in Fig. 3. The circuit includes eight sample capacitors, two feedback capacitors and eight comparators. To minimize the sampling instants, the same sampling clock is used for the MDAC and the flash comparators. After the analog input is sampled during Φ_1, the flash has a time to make a bit-decision in Φ_2, so the time available for settling the first MDAC is decreased which needs the first MDAC amplifier to have a high bandwidth. The amplifier used in SHA-less is shown in Fig. 4. The amplifier is a two-stage Miller-compensated BiCMOS architecture, and the two stages are separated by emitter followers for buffering and level-shifting. The two switch-capacitor common-mode (CMFB) loops are used for the two stages. Bipolar transistors are used as cascodes in the first stage and form the differential pair in the second stage which can improve the bandwidth of the amplifier.

It is noticed that this design uses two additional comparators, which will bring two benefits. First, there is a similar sampling network for the MDAC and flash, which is important in matching bandwidth. Second, the two additional comparators fold the ends of the transfer function so that the pipeline stage output is between $\pm\frac{1}{2}V_{\text{REF}}$ (Fig. 2) at the full scale input swing. Thus, where a S/H amplifier begins to compress, the front-end sampling pipeline stage of the ADC will maintain its linearity across the full dynamic range.

3.2. Sampling network matching

With the pipeline stage sampling a continuous time input signal rather than a held signal from an S/H, there are errors resulting from flash-to-MDAC bandwidth and timing mismatch. To minimize these errors, similar structures are used in the MDAC and flash to measure the input as represented in Fig. 3. Because both the MDAC and flash connect their input signals to capacitors, they both have input impedance that can be modeled as a low pass filter. However, the specific components within the MDAC and flash are different, resulting in different cutoff frequencies for the low pass characteristics of each. Figure 3 shows this difference schematically by showing the MDAC with an input frequency response with a cutoff at frequency F_1. In contrast, the flash has frequency F_2. Commonly, F_1 is lower than F_2. This difference between F_1 and F_2 will bring an aperture error which is shown in Eq. (1). To reduce the significance of this error, a trim circuit is inserted into the flash. The trim circuit equalizes the input impedances between the MDAC and flash as shown in Fig. 5.

As shown in Fig. 3, the same sampling clock is used for the MDAC and flash, so their sampling instants are equal. Aperture error is largely determined by the propagation delays. The trim circuit is inserted between the input switch and the sample capacitors of the flash. The input signal V_{A} has a leg which is applied to the variable resistance network, and V_{A} is coupled to the output V_{B} through resistor R_1. It also includes additional paths that can be connected in parallel with resistor R_1 to

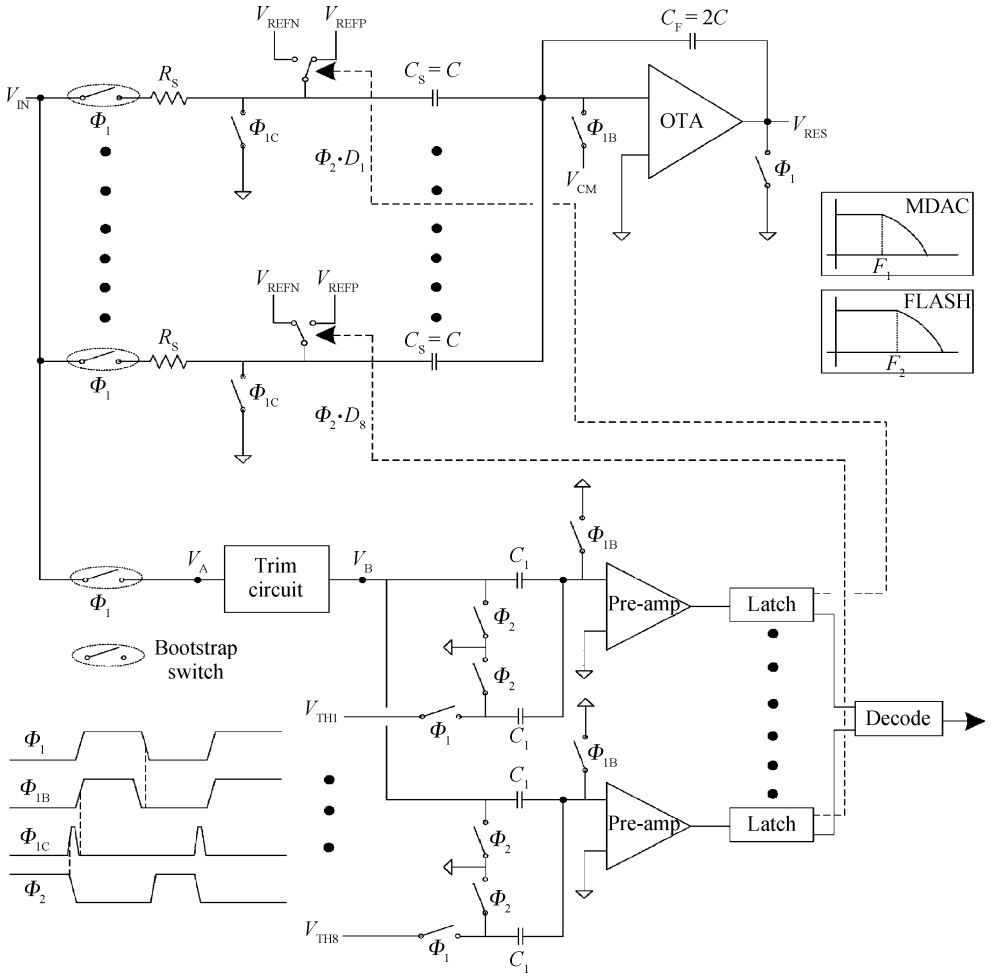

Fig. 3. Proposed SHA-less 2.5-bit stage.

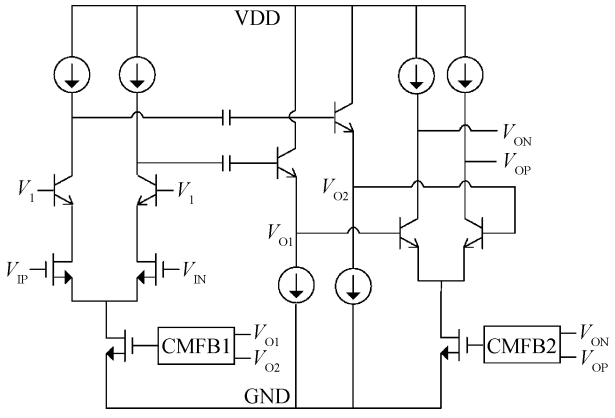

Fig. 4. Schematic of opamp.

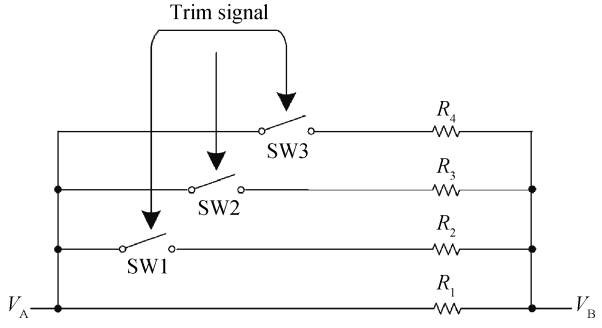

Fig. 5. Trim circuit.

change the resistance. The cutoff frequency F_2 can be changed by changing the resistance in series with those capacitors.

From Fig. 2 and Eq. (1), any bandwidth mismatch between the MDAC and the flash will cause the output V_{RES} of the SHA-less architecture to exceed $\pm\frac{1}{2}V_{REF}$. In order to select the appropriate value for the resistance provided by the trim circuit, a trim procedure is shown in Fig. 6. Through this procedure, the aperture error caused by a resistance-capacitance delay mismatch between the input networks for the first MDAC and the flash will significantly decrease so that the accuracy of the MDAC is enhanced.

3.3. Counteracting remnant charges

In order to eliminate the undesirable remnant charges on the sample capacitors in the first MDAC and flash, an implementation suitable for SHA-less architecture is shown in Fig. 3 along with the timing diagram. The nonlinear charge kickback problem is solved by using a clearing switch driven by a short pulse Φ_{1C} in the MDAC and separate sampling capacitors C_1 in the flash. During Φ_1, C_S samples V_{IN} and during Φ_2, C_S

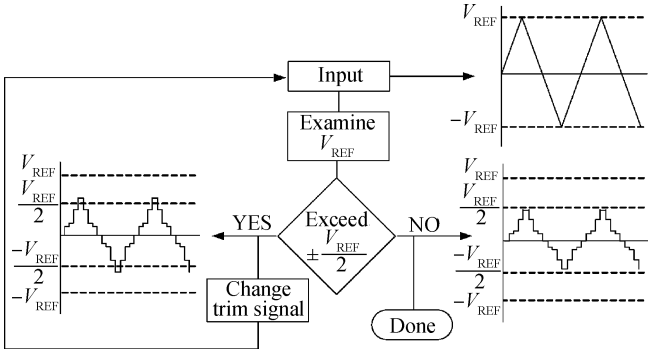

Fig. 6. Trim circuit calibration procedure.

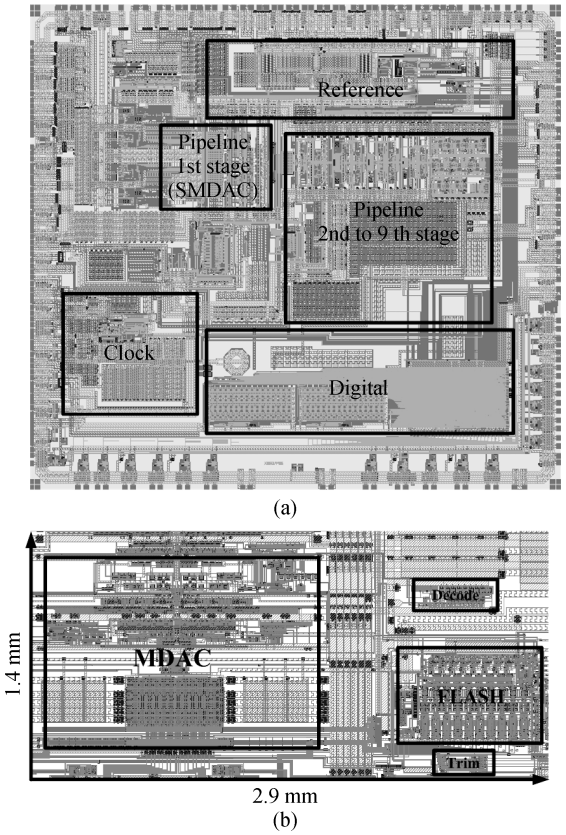

Fig. 7. Layout of the proposed circuit. (a) The 125-MS/s 14-bit pipeline ADC. (b) The first SHA-less stage.

connects to V_{REFP} or V_{REFN} depending on the flash data. Before C_S is connected back to V_{IN}, a short clearing pulse Φ_{1C} discharges the nonlinear charges. Also, during Φ_1, C_1 samples V_{IN} and during Φ_2, C_1 connects to V_{CM}, the nonlinear charges are removed. Therefore, the proposed circuit completely discharges the remnant charges and the accuracy of the SHA-less is substantially enhanced.

4. Experimental results

The proposed circuit is designed in 0.35-μm BiCMOS technology for a 3.3 V supply voltage, and occupies a 1.4 × 2.9 mm^2 area of silicon and consumes 52 mW. Its layout is shown in Fig. 7. This circuit is specially designed to meet the specifications of a front-end stage for a 125-MS/s 14-bit pipeline ADC. The adopted differential full-scale input is 1 $V_{P\text{-}P}$. The common-mode-voltage (V_{CM}) is 1.65 V, V_{REFP} and V_{REFN} are 2.15 V and 1.15 V respectively. C_S is implemented with a PIP capacitor and is set to 750 fF.

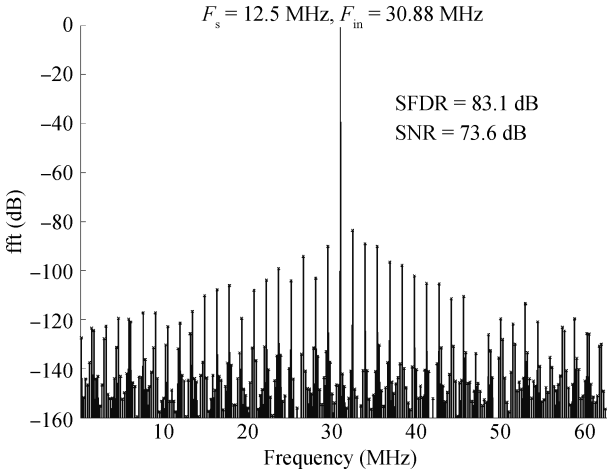

Fig. 8. Spectra of the proposed pipeline ADC.

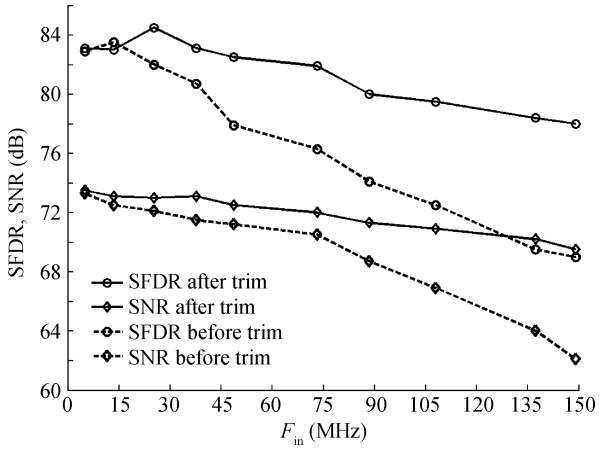

Fig. 9. SNR and SFDR with and without calibration at the sample rate of 125 MS/s.

The dynamic performance of the pipeline ADC is summarized in Figs. 8 and 9. When clocked at 125 MHz, the input signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) with a 30.88 MHz sin-wave input are 73.6 and 83.1 dB. With the trim control code set at its default value, in which all switches are open, the analog impairments such as bandwidth mismatch and clock jitter cause steep dynamic performance degradations over the input frequency. After calibration is turned on, bandwidth mismatch is greatly reduced, the degradations over the input frequency are gradual, a greater than 78 dB SFDR is still measured when the input frequency is up to 150 MHz. The static performance is shown in Fig. 10. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are less than 0.5 and 2.5 LSB.

The performance of the proposed circuit compared with other circuits is summarized in Table 1. The figure of merit (FOM) is defined as $P/2^{ENOB}\cdot f_s$, where P is the power consumption, ENOB is the effective number of bits at low input frequency and f_s is the sampling rate. As shown in Table 1,

Table 1. Performance comparison.

Parameter	This work	Ref. [7]	Ref. [8]	Ref. [9]
Technology (μm)	0.35 BiCMOS	0.35 SiGe-BiCMOS	0.18 CMOS	0.09 CMOS
Architecture	SHA-less	SHA	SHA-less	SHA
Calibration	None	None	Digital background	Digital background
Sampling rate (MHz)	125	65	100	100
Resolution (bit)	14	16	14	14
Supply power (V)	3.3	3.3	3.3	1.2
Power consumption (W)	1.1	1.2	0.23	0.25
Active area (mm^2)	34.5	28	7.28	1
SFDR (dB) (F_{IN} = 30 MHz/150 MHz)	83.1/78.3	78.5/64.3	88.3/82.5	78.1/65.1
SNR (dB) (F_{IN} = 30 MHz/150 MHz)	73.6/69.3	73.9/66.5	72.4/67.5	74.6/62.1
DNL (LSB)	−0.5/+0.4	−0.9/+1.9	−0.8/+0.7	−0.8/+0.9
INL (LSB)	−2.4/+2.5	−4.2/+6.0	−2.1/+2.0	−1.3/+1.2
FOM (pJ/conv.)	2.41	3.15	0.69	0.68
Year (Ref.)	—	2005	2008	2009

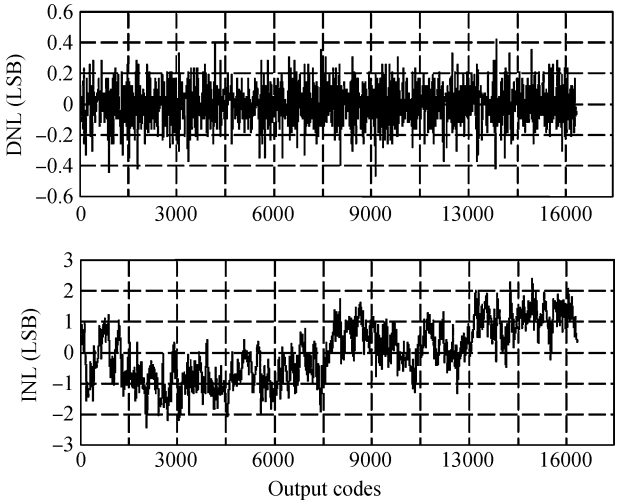

Fig. 10. Static performances.

the proposed pipeline ADC achieves desirable dynamic performance at high input frequency. However, the proposed ADC is designed in 0.35-μm BiCMOS technology, and dos not use digital background calibration. Furthermore, the ADC includes other blocks such as an input buffer, a clock duty cycle stabilizer etc. It sacrifices some area and power to meet the high performance. Overall, the circuit has sufficient performance for high-speed high-resolution applications.

5. Conclusion

This paper describes a novel SHA-less architecture for the front-end stage of a pipelined ADC. A 125-MS/s 14-bit pipeline ADC incorporating this technique has been verified in a 0.35-μm BiCMOS process. By adopting the sampling network matching and counteracting remnant charges to enhance accuracy, experimental results show that SFDR and SNR have been largely improved and the maximum input frequency is up to 150 MHz without steep performance degradations. The proposed SHA-less architecture can be applied widely to high-speed high-resolution analog-to-digital converters.

References

[1] Shirazi N, Mirhaj A, Ashtiani A, et al. A novel low power 1 GS/s S&H architecture with improved analog bandwidth. IEEE Trans Circuits Syst, 2008, 55(10): 971

[2] Wang Y, Yang H G, Ye Z H, et al. An improved high gain and wide bandwidth operational amplifier for the SHA circuit in a pipelined ADC. ICSICT, 2010: 269

[3] Chang D Y. Design techniques for a pipelined ADC without using a front-end sample-and-hold amplifier. IEEE Trans Circuits Syst, 2004, 51(11): 2123

[4] Huang P L, Chiu Y. A gradient-based digital algorithm for sampling clock skew calibration of SHA-less pipeline ADCs. ISCAS, 2007: 1241

[5] Hashemi S, Shoaei O. A 0.9-V 10-bit 100 MS/s switched-RC pipelined ADC without using a front-end S/H in 90 nm CMOS. ISCAS, 2008: 13

[6] Huang P L, Hsien S, Lu V, et al. SHA-less pipelined ADC with in situ background clock-skew calibration. IEEE J Solid-State Circuits, 2011, 46(8): 1

[7] Zanchi A, Tsay F. A 16-bit 65-MS/s 3.3-V pipeline ADC core in SiGe BiCMOS with 78-dB and 180-fs jitter. IEEE J Solid-State Circuits, 2005, 40(6): 1225

[8] Lee B G, Min B M, Manganaro G, et al. A 14-b 100-MS/s pipelined ADC with a merged SHA and first MDAC. IEEE J Solid-State Circuits, 2008, 43(12): 2613

[9] Vel H V, Buter B A J, Ploeg H, et al. A 1.2-V 250-MW 14-b 100-MS/s digitally calibrated pipeline ADC in 90-nm CMOS. IEEE J Solid-State Circuits, 2009, 44(4): 1047