A low-power multi port register file design using a low-swing strategy*

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Abstract: a low-power register file is designed by using a low-swing strategy and modified NAND address decoders. The proposed low-swing strategy is based on the feedback scheme and uses dynamic logic to reduce the active feedback power. This method contains two parts: WRITE and READ strategy. In the WRITE low-swing scheme, the modified memory cell is used to support low-swing WRITE. The modified NAND decoder not only dissipates less power, but also enables a great deal of area reduction. Compared with the conventional single-ended register file, the low-swing strategy saves 34.5% and 51.15% bit-line power in WRITE and READ separately. The post simulation results indicate a 39.4% power improvement when the twelve ports are all busy.

Key words: low-swing; multi port; NAND; register file
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1. Introduction

In order to improve the performance of microprocessors, current microprocessor designs aim at increasing the instruction level parallelism. The instruction level parallelism can not only be achieved through using a pipeline structure in the time domain, but can also be introduced by multiple issuing units in a single cycle. However, the latter leads to the area growth of on-chip hardware and to higher power consumption. The register file is among the main power consumers with growing complexity proportional to the increasing instruction parallelism in a microprocessor[1], and thus how to reduce the power dissipation in a register file becomes a critical problem in low-power microprocessor design and especially in an embedded application.

Recently, several techniques have been introduced for saving the power consumed in SRAM[2−8]. The half-swing pulse technique[2] pre-charges the bit-line to half of the power supply and reduces the swing of the bit-line to $V_{DD}/2$. However, this method needs an additional half V_{DD} power supply. The current-mode write technique[3] saves power by keeping the bit-line swing very small through current-mode operation. This scheme consumes only 30% of the power of an SRAM with current-mode read but voltage-mode write operations. Yang's SRAM[4] uses hierarchical bit-line and local sense amplifiers, and in this SRAM the swing voltages of the bit-lines and the data bus are controlled by the pulse widths only. In this scheme, the voltage swing of the bit-lines for the WRITE operation is reduced to $V_{DD}/10$ at the expense of two additional full swing control signals in the array that runs in parallel to the word line. Segmented virtual ground (SVG) techniques[5] keep the memory cell in the weak inversion region to save static power and lower the SVG to the ground if one of the cells is accessed for READ operation. It saves both dynamic and static power. However, the use of three mid-rail reference voltages makes it less attractive.

The above strategies can provide a great deal of power improvement to SRAM, but most of them are hard to implement in multi-port register file design. First, the silicon area grows in a quadratic manner proportional to the number of register file ports if it is built in the conventional structure[6], and this makes the differential bit-line structure unusable. Therefore, a single-ended bit-line structure is often preferred in high density implementation of multi-port register files. Thus some low-power strategies, such as the current-mode write technique[3] become useless. Second, the additional voltage regulator or reference in Refs. [2, 4, 5, 7] are sometimes hard to implement due to the limits of technology. Most of the processors are fabricated under the general digital CMOS process, which has no analog device to support the voltage regulator or reference. Third, even if the swing of bit-line is reduced by the usage or other voltage source, then how to write the data into the memory cell through a single low-swing bit-line successfully and reliably is still difficult to figure out. Traditional memory cells do not work well yet and with the need for multi-write ports, memory cell design is becoming increasingly difficult.

Taking the above factors into account and to save power, a low-swing strategy is proposed in Ref. [8]. Nevertheless in this low-swing strategy the feedback device consumes a lot of power, especially in the WRITE scheme. In order to the reduce power consumed by the feedback circuits, the low-swing strategy based on dynamic feedback control is introduced in this paper. In addition, the low-swing WRITE strategy in this paper is more robust due to the use of a modified memory core cell. Most importantly, the low-swing strategy in this paper uses dynamic circuitry and eliminates the static current generated by the low-swing voltage, and this enhances the total power improvement in the register file.

This paper also presents a modified NAND decoder. Al-

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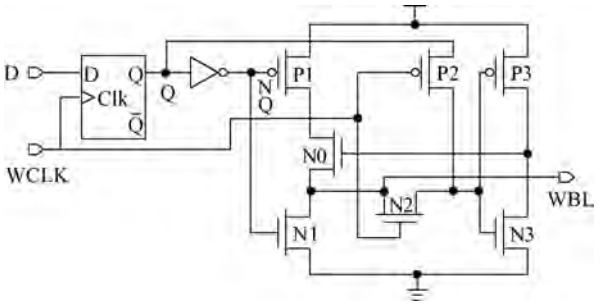

Fig. 1. Low-swing driving circuit.

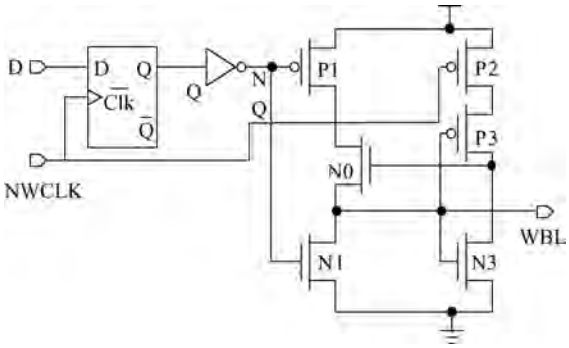

Fig. 2. Low-swing driving circuit with dynamic feedback.

though traditional NAND decoders are good at saving power, the area cost of implementing complementary logic is very large. This is especially important in multi-port register files, because the number of block arrays is proportional to the port number. In order to reduce the area used in a decoder block, a modified NAND decoder has been proposed.

2. Architecture

The architecture of the low-power multi-port register file consists of three parts: the low-swing WRITE, the low-swing READ and the modified low-power NAND decoder. The low-swing WRITE and READ strategy is used to reduce the power consumed in the bit-line and the modified NAND decoder is an optimization of a traditional NAND address decoder.

2.1. The proposed low-swing WRITE strategy

The proposed low-swing WRITE strategy not only reduces power dissipation, but also turns the differential end into a single end without WRITE ability penalty, which cannot be obtained through a traditional memory cell structure, and this is very beneficial for high density design.

The proposed low-swing WRITE strategy consists of two parts: a driving circuit and a memory core cell.

The driving circuit charges or discharges the bit-line quickly, while the bit-line always has a large load capacitance, and thus the driving circuit needs to provide a large current to satisfy the high-speed constraint. An inverter with a large driven capacity serving as the driving circuit is very common in conventional non-low-swing designs. However, the inverter is not able to limit the voltage swing of the bit-line, except for when an additional power supply is used. In order to avoid using an additional power supply or any other on-chip reference voltage, a proposed driving circuit with a voltage clamp function is shown in Fig. 1.

This low-swing driving circuit is based on the feedback mechanism. In this circuit, the P1 and N1 transistors provide a large current to drive the bit-line according to the input data D. Unlike the common inverter, the P1 charges the bit-line through transistor N0, and N0 is controlled by the bit-line state detected by the P3 and N3 transistors. For example, as the data D (D = "1") stands by and the write clock WCLK becomes "1", the N2 transistor is conducted and the voltage of the bit-line is transferred to the gates of P3 and N3 through N2. Once the bit-line is "0", the output of P3 and N3 becomes "1". Then the N0 connects the bit-line to transistor P1, and the bit-line is charged by P1. When the voltage level of the bit-line exceeds the threshold voltage V_{th} of P3 and N3, the output of P3 and N3 turns over and then the voltage level of the bit-line has been clamped to V_{th}. If the data D equals "0", the bit-line will be discharged to the ground. In short, this circuit can limit the swing of the bit-line to $\pm V_{th}$, and by adjusting the ratio of P3 and N3, a reasonable V_{th} can be obtained.

Although the voltage swing of the bit-line is reduced by feedback, the additional power consumption caused by the feedback devices should be considered as well. In this circuit, the feedback circuit is an inverter that consists of transistors P3 and N3. When the voltage of the bit-line is around the V_{th}, the feedback part consumes a large current. If the voltage is still restricted to V_{th}, the feedback circuit will produce a static current and in order to reduce the power caused by this static current, transistor P2 is added to eliminate this state. As the WRITE operation completes, the WCLK signal becomes "0", and then transistor N2 is shut down while transistor P2 is conducted. During this time, the input voltage of the feedback device goes to full swing and this guarantees that the power consumption of the feedback device is minimized.

Figure 2 shows another low-swing driving circuit. In this driving circuit, the feedback device is a dynamic circuit. This dynamic inverter can also eliminate the static current consumption by carefully designing the width of the WRITE clock pulse. Compared with the driving circuit in Fig. 1, this circuit is very simple and uses fewer transistors.

The second part in this proposed low-swing is a memory cell. In traditional register file design, the memory cell may suffer from the weak pulling-up ability of an NMOS access transistor in the WRITE operation. Differential bit-lines are used for their robustness in writing data 1 into the memory cell. As the voltage swing is reduced, it becomes harder to write correct data into memory cells. However, the proposed cell does not have this problem.

Figure 3 depicts a structure that supports the low-swing WRITE scheme with only a single access transistor. Unlike the differential structure, the single-ended structure cannot use a sense amplifier memory cell for a lower complementary bit-line signal or reference voltage. In order to write the data correctly from the bit-line to the memory cell using a low-swing strategy, the low-swing memory core cell uses a level shifter structure. As shown in Fig. 3, the cross-coupled inverters are replaced by a structure similar to part of the level shifter shown in Fig. 4. In this structure, the combination of transistors N1,

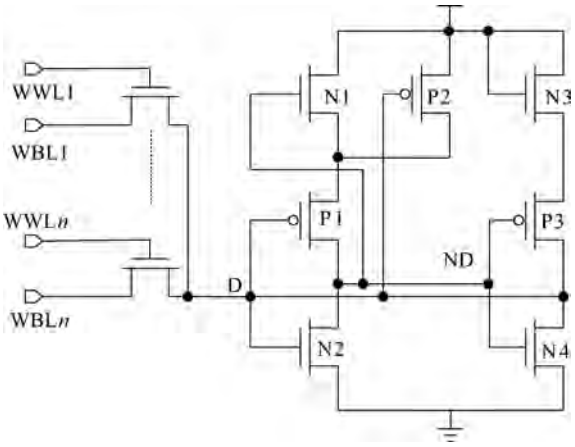

Fig. 3. Low-swing memory core cell with a multi-WRITE port.

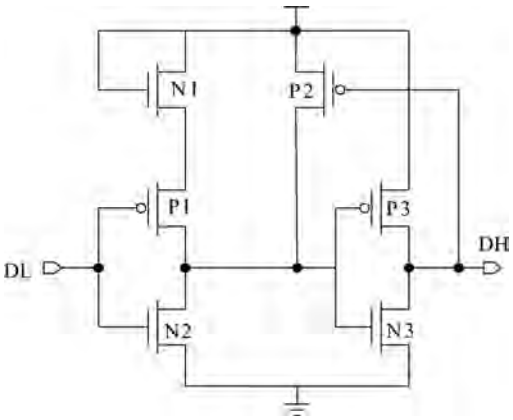

Fig. 4. Single-ended level shifter.

P1 and N2 acts like an inverter, and transistors N3, P3, N4 form another "inverter". These two "inverters" cross couple together to store the information passed from the bit-line. The output voltage swing of this special "inverter" is $\pm(V_{DD} - V_{thn})$ as the use of the surpassing nMOS transistor. Typically, the threshold voltage of this "inverter" is $(V_{DD} - V_{thn})/2$. If the input voltage level is higher than $(V_{DD} - V_{thn})/2$, the "inverter" flips and this lower threshold voltage makes the low-swing WRITE strategy possible. Suppose the data D stored in this memory cell is "0" and the ND is "1". When one of the word lines becomes effective, the bit-line then connects to the memory cell. Once the voltage of the bit-line is driven to V_{th} by the circuit in Fig. 1 and if V_{th} is higher than the $(V_{DD} - V_{thn})/2$, then the output ND of the "inverter" becomes "0". In this memory core cell, only the voltage of node ND is full swing due to the use feedback transistor P2. Thus the word line can use a low-swing signal as well. However, in order to reduce the conductance resistance of the access transistor, a full swing word line signal is preferred.

In this low-swing WRITE scheme, the write margin can be expressed as $V_{th} - (V_{DD} - V_{thn})/2$. Therefore, in order to ensure robustness, the V_{th} can be set to $V_{DD}/2$, and then the write margin is $V_{thn}/2$. The entire design will show great robustness. Sometimes the voltage swing of the bit-line Vth should be set between $(V_{DD} - V_{thn})/2$ and $V_{DD}/2$. When this happens, the write margin decreases. In addition, the threshold voltage of this special "inverter" can be adjusted to support the robustness of the WRITE operation. In this paper, the native transistor N2 is used to lower the threshold voltage and enhance robustness. The worst performance in WRITE operation occurs in the SNFP (slow nMOS fast pMOS) corner. Figure 5 depicts the write margin in this low-swing strategy, and the worst write margin in SNFP is 194 mV. This means that the proposed cell has great robustness in WRITE operation. Based on the above discussion, the swing of the write bit-line in this scheme has been set to a reasonable value through consideration of the write margin.

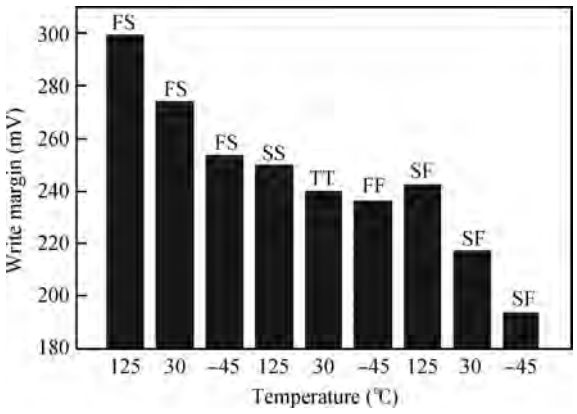

Fig. 5. Write margin in the proposed low-swing scheme.

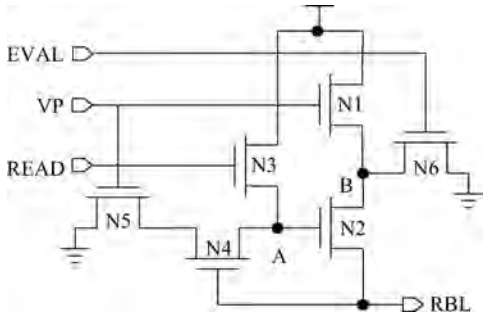

Fig. 6. The pre-charge circuit in the low-swing READ strategy.

2.2. The proposed low-swing READ strategy

The proposed low-swing READ circuit also consists of two parts: a pre-charge circuit and a sense amplifier circuit.

The low-swing pre-charge circuit is shown in Fig. 6. The principle of this pre-charge circuit is feedback logic, which is similar to the driving circuit in the WRITE scheme. However, unlike the driving circuit, this low-swing pre-charge circuit works in a dynamic way and its timing waveform is shown in Fig. 7. Once there is a READ operation, then a pulse called READ is generated to initialize the pre-charge circuit. Node A is pre-charge to $V_{DD} - V_{thn}$. Then the pre-charge pulse VP is generated after the READ pulse. During this time, the bit-line is charged and the voltage begins to rise. When this voltage is above the threshold voltage of transistor N4, node A starts to discharge and then the bit-line's pre-charge process finishes. The EVAL signal is used to reset the node B to avoid charge sharing problems. Ideally, the voltage of the bit-line can be charged to $V_{DD} - 2V_{thn} - \Delta V$. The ΔV is caused by the substrate bias effect in N1 and N2. Compared with the driving cir-

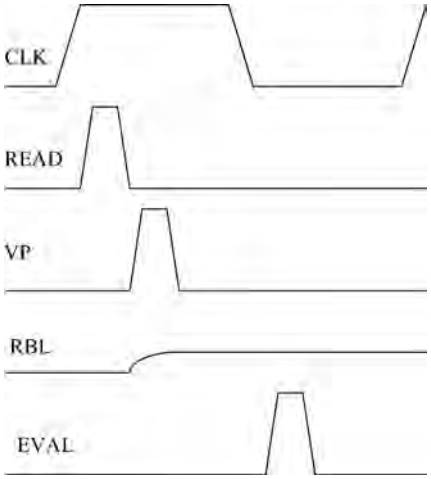

Fig. 7. The timing of the low-swing pre-charge scheme.

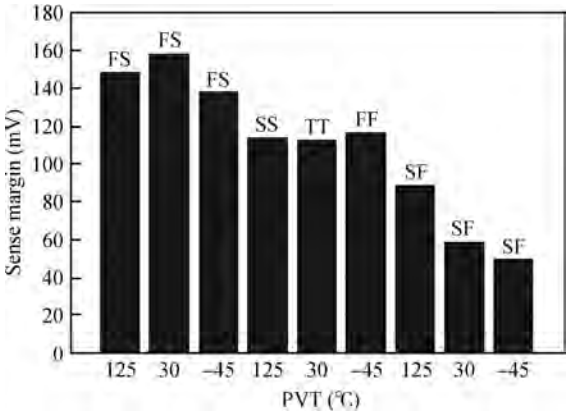

Fig. 8. Sense margin in the proposed low-swing scheme.

cuit in the WRITE scheme, this dynamic pre-charge circuit has no static current caused by the feedback device and has lower swing at the cost of fixed timing control. In this circuit, the voltage of node A is also between $V_{DD} - V_{thn}$ and GND. This proves that the node A is also a low-swing node which further saves power.

Similarly, in the low-swing READ strategy, the voltage swing can not be decreased greatly due to the limits of the sense margin. Typically, the sense amplifier in a single-end bit-line is an inverter, and the transaction point is about half V_{DD} and cannot support low-swing operation. In order to solve this problem, the sense amplifier in the low-swing strategy here is a level shifter. As Figure 4 depicts, the input signal DL connects with the RBL signal and the output of register file can be obtained through a DFF using the EVAL as the sampling clock. Or the signal DL can be sampled by the EVAL signal and then the output of this level shift is the output of the register file. Therefore, the transaction voltage of the common level shift is $(V_{DD} - V_{thn})/2$. Then the sense margin can be expressed as $(V_{DD} - 2V_{thn} - (V_{DD} - V_{thn})/2)$, which equals $(V_{DD} - 3V_{thn})/2$. This is very small compared with the write margin. Hence, in this sense amplifier, the N2 here is a native nMOS transistor. Figure 8 depicts the sense margin in different PVTs. From this picture, the worst case appears at the SF (slow nMOS fast pMOS) corner under −45 ℃, and the sense margin is only about 50 mV.

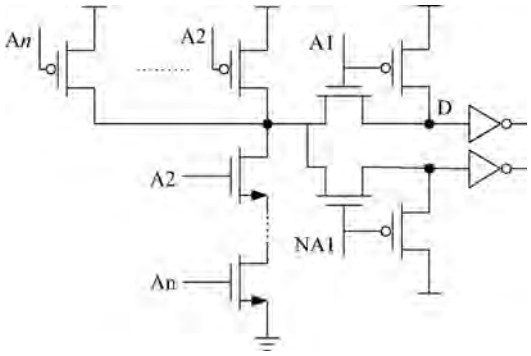

Fig. 9. The modified NAND address decoder.

Considering the sense margin, the bit-line swing during read almost reaches its limitation. If the swing continues to decrease, the sense amplifier does not work correctly.

2.3. The modified NAND address decoder

As a critical block in the memory system, the decoder's performance is very important to the whole register file design. Compared with the NOR decoder, the NAND type decoder performs best as it has the least delay and lowest minimum and maximum energies to a four input address[9]. However, the NAND structure decoder consumes more transistors in realizing complementary logic. The more transistors are used, the more area and larger drive capacity to address lines are needed. In order to solve these problems, a modified NAND decoder is proposed in this paper.

The main idea is to merge two NAND decoders (Fig. 12(d)) into one NAND decoder. The exact implementation is depicted in Fig. 9. The modified NAND decoder merges two static NAND decoders into one by sharing an identical address line. For example, the first NAND decoder input address is A5-A4-A3-A2-A1, and the other one is A5-A4-A3-A2-NA1. Then, the same address bit A5-A4-A3-A2 can be shared by each of them to form a 4-input NAND decoder, and the last address bit A1 and NA1 can receive the output of the shared 4-input NAND structure to generate correct information. The whole structure does not affect the decoding delay.

Suppose the address is N bit, this merged NAND decoder only consumes $2N + 2$ transistors instead of $4N$ transistors in the NAND decoder. This saves a lot of transistors when the address number is more than two. For example, if the address number N equals 5, the merged NAND decoder will save 40% transistors.

3. Performance comparisons

In a conventional single-ended register file, the swing of the bit-line is V_{DD} during WRITE or READ operation. Thus the powers in a conventional bit-line (P_{CVBL}) can be expressed as follows:

$$P_{CVBL\,@\,write} = fC_{WBL}V_{DD}^2, \tag{1}$$

$$P_{CVBL\,@\,read} = fC_{RBL}V_{DD}^2 + P_{SA}, \tag{2}$$

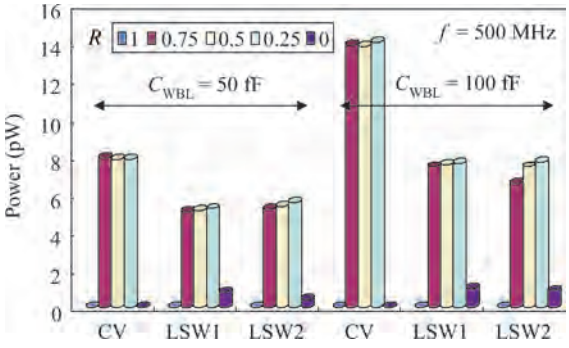

Fig. 10. Power comparison with low-swing WRITE @ 500 MHz.

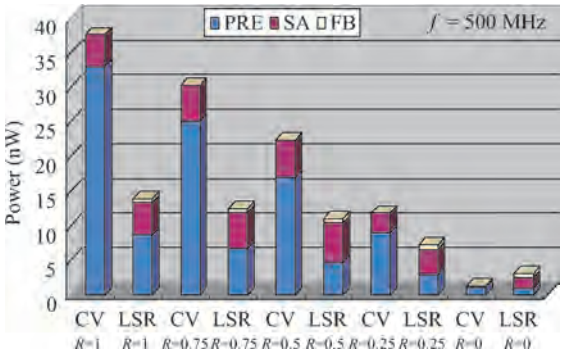

Fig. 11. Power comparison with low-swing READ @ 500 MHz.

where f is the clock frequency and C_{WBL} and C_{RBL} are the load capacitances of a WBL and an RBL. P_{SA} is the power caused by the sense amplifier. For simplicity, the CV is the short form of conventional single-ended register file.

3.1. Power comparison of low-swing WRITE

Suppose the swing of the WBL in a low-swing WRITE scheme is ΔV_{WBL}. Then the power consumed in the WBL can be expressed as follow:

$$P_{\mathrm{LSWBL@write}} = f C_{\mathrm{WBL}} \Delta V_{\mathrm{WBL}}^2 + P_{\mathrm{FBW}}, \qquad (3)$$

where the P_{FBW} is the power cost by the feedback device. In this low-swing scheme, ΔV_{WBL} represents the logic "1" instead of V_{DD} while the logic "0" remains the same. By considering this unchanged logic "0", the feedback device in Figs. 1 and 2 does not dissipate any power as the input data D remains "0". This means that the P_{FBW} is generated by any data switching or by keeping the logic "1" in the WRITE step. This makes P_{FBW} relate to input data D.

Figure 10 shows the power dissipation variation with the R that is the proportion of data "0" in input data D. For example, the number 0.5 indicates that half of the input data D is zero. LSW in Fig. 8 represents LSW. As Figure 8 shows, the LSW strategy is effective in saving power from the WBL. This scheme is very efficient as the majority of the input data is "0". Furthermore, the LSW strategy becomes more effective as the load capacitance of WBL increases. Setting the proportion of data "0" R to equal 0.5, the power improvement through LSW1 is 34.5% when the load capacitance is 50 fF, and as the load capacitance increases to 100 fF, the power improvement rises to 45.4% in the LSW1.

3.2. Power comparison of LSR

Suppose the swing of the RBL in an LSR scheme is ΔV_{RBL}. Then the power consumed in the RBL can be expressed as follows:

$$P_{\mathrm{LSRBL@read}} = f C_{\mathrm{RBL}} \Delta V_{\mathrm{RBL}}^2 + P_{\mathrm{FBR}} + P_{\mathrm{SA}}, \qquad (4)$$

where P_{FBR} is the power caused by the feedback device in the pre-charge step and P_{SA} is the power consumed by the sense amplifier. Unlike the LSW scheme, the feedback circuitry in a LSR scheme is a pure dynamic circuit. Its main power comes from refreshing the node and the transition of the circuit state.

Figure 11 provides a power comparison of the RBL with the LSR scheme. R has the same definition as in the LSW scheme, and the C_{RBL} is set to be fF.

As Figure 11 depicts, the power saved by the LSR scheme is very effective, and when R is equal to 0.5, the power improvement of this strategy is 51.15%. The additional power generated in the feedback control logic is not changed too much. However, the power caused by the sense amplifier becomes the dominant factor in the total power consumption in the LSR strategy, which deteriorates the power improvement and becomes even worse when R is 0.

Although the power dissipated by the sense amplifier in the LSR strategy is larger than in a traditional register file, the sensing speed is reduced by the low swing of the RBL. Because the read-out logic in the memory core cell can discharge the bit-line faster than ever.

From the above comparison of LSW and LSR strategies, the power improvement has a relation with the input data D. Therefore, a simplicity statistic of the data in the register file has been done. According to the FFT1024 and MPEG2, the R in these two programs is 0.771 and 0.628 separately. These results are obtained from the DSP instruction simulator in Ref. [10]. And thus the low-swing strategy can be very effective in the total power improvement.

3.3. Performance comparison of address decoders

This section compares the modified NAND decoder with the other four-type decoders commonly used as address decoders. Those four type decoders are shown in Fig. 12.

In those decoders, the discharge paths are formed by the nMOS transistors, and pMOS transistors are used to charge and initialize the decoder. Therefore the size of pMOS is not very important. In those decoders, the pMOS is the smallest size for reducing the area. Generally, for fast decoding, the width and length ratio of an nMOS is larger than a pMOS's. However, by considering low power applications, the ratio of width and length of the nMOS transistor is set to 200 nm/100 nm in order to reduce the node capacitance.

Suppose that the register file has five bit addresses, and Table 1 gives the hardware resources used in those decoders without using a pre-decoding strategy and taking the pulse generator into account. The Pch in the decoder is the transistor used to pre-charge and the Dch is the number of transistors providing the discharge path. The Inv in the peripheral circuit here repre-

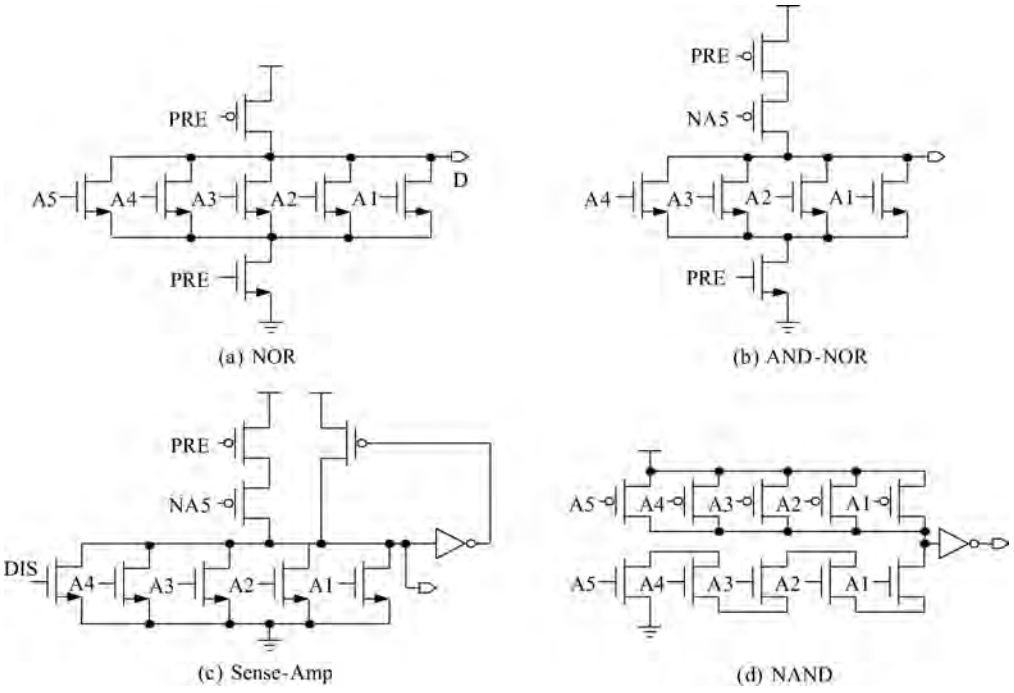

Fig. 12. Four types of address decoders.

Table 1. The hardware resources of those address decoders.

Decoder	Decoder circuit			Peripheral circuit		Total
	Pch	Dch	Sa/Inv	Inv	Control	
NOR	1×32	6×32	—	2×10×4	2×4	312
A-N	2×32	5×32	—	2×10×4	2×4	312
S-A	3×32	5×32	2×32	2×10×4	4×4	416
NAND	5×32	5×32	2×32	2×10×4	—	464
MNAND	6×16	6×16	4×16	2×10×4	—	336

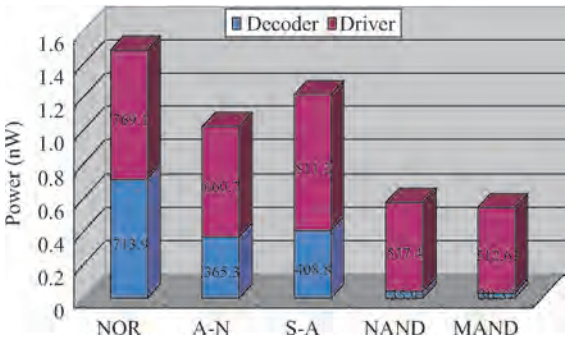

Fig. 13. Power comparisons of those address decoders.

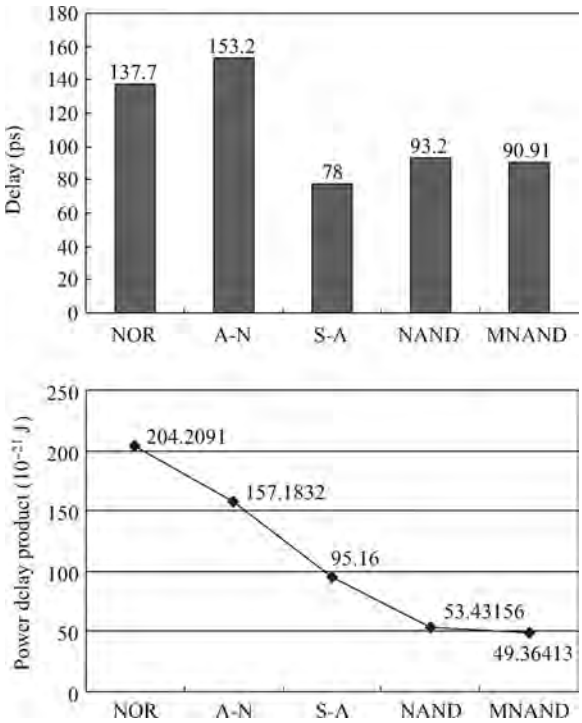

Fig. 14. The delay and PDP of different structure address decoders.

sents the inverter that is used as the driving circuit for address signals and the control circuitry. From Table 1, the MNAND type decoder saves a lot of transistors in implementation compared with the Sense-Amp and NAND decoders. Although a few more transistors are used in the MNAND decoder than in the NOR and AND-NOR type decoders, the MNAND decoder has no additional control signal used in pre-charge.

Figure 13 shows a power comparison diagram of those different decoders in SMIC 90 nm technology with the clock @ 5 GHz @ TT corner. From the diagram, the MAND structure decoder consumes less power in both the driving and the decoding steps. The power delay product is given in Fig. 14, below, and the power delay product is also the best in those address decoders.

4. Implementation

In this paper, an eight read and four write ports register file is designed using the low-swing strategy. The register file

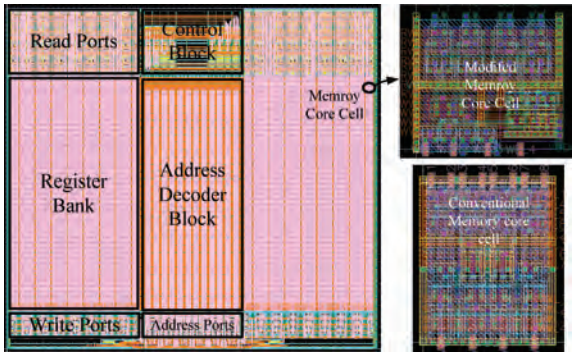

Fig. 15. Layout of the low-power register file and its memory core cell.

Table 2. The feature comparison.

Feature	LS-RF	CVRF
Process	SMIC90G CMOS	SMIC90G CMOS
Organization	32 × 32	32 × 32
Core area (μm^2)	5.51 × 5	4.66 × 5.85
Area (μm^2)	253.6 × 233	226.4 × 241.2
Read access time (ns)	1.36	1.8
Power @ Standby (μW)	659	324.4
Power @ WRITE (μW)	1290	1645
Power @ READ (μW)	1249	1324
Power @ FULL (μW)	8324	13740
Peak current (mA)	40.69	85.84

is organized as 32 × 32 bits. Figure 15 is the layout of this low-power register file.

Table 2 compares the low-power register file with a conventional register file. The data here are obtained by various post-simulations under different PVTs. In the worst case, the read access latency in the proposed register file is 1.36 ns, which is 76% of the conventional one. This proves that the proposed low-swing scheme also brings a timing improvement. According to Table 2, the core size of this modified cell in LSRF is a bit larger than the CVRF even if the previous one uses fewer transistors. That is because the native transistor often needs a huge area to satisfy the design rule. Finally, the area of the LSRF is about 1.08 times that of the CVRF, and by the use of native nMOS transistors, the standby power has been increased as compared with the CVRF. This makes the power improvement by using the low-swing strategy less effective. However, the power has still been reduced by the low-swing strategy. From Table 2, the power in WRITE is reduced by about 21% in one write port, and by removing the influence of leakage and other control devices, the power improvement in WRITE is 55.2%. The power saved in READ is only about 7% in one read port. Without taking other circuit power dissipation in account, the improvement increases to 43.47%. This implies that the power consumed in RBL is less than the WBL in one port. When the twelve ports are all busy, the energy cost in the other circuit, such as the driver, the buffer takes a smaller proportion, and this makes the improvement increase to 39.4%. Furthermore, the low-swing strategy can also decrease the peak current in the register file, which enhances the reliability of the register file. All the power results are based on the post-simulation results @ TT corner under 30 ℃.

Table 3. Comparison of present register file in CMOS.

Parameter	ISSCC'02 [11]	NTIP'07 [12]	ISSCC'04 [13]	ASYNC'09 [14]*	This work*
Size	34 × 64	34 × 64	34 × 64	32 × 32	32 × 32
Ports	16	16	16	4	12
Process (nm)	110	110	110	65	90
Frequency (MHz)	500	500	500	1200	500
Supply (V)	1.2	1.2	1.2	1.0	1.0
Power (mW)	220	106	133	13	8.3
FOM (nW/MHz)	429.69	207.03	179.69	84.64	43.3

* Post-simulation results.

Finally, a comparison of the present register file design in CMOS is given in Table 3. The register file designed in ISSCC'02 has the conventional single-ended structure with a pre-decoder. While in ISSCC'04, the author uses a differential current mode sensing method to reduce the access time and power with the help of a reference cell. In NTIP'07, the register file is based on a multi-bank structure. Each bank is implemented in a two-port differential SRAM structure. The register file in ASYNC'09 is a dual ported SRAM structure. And by observing Table 3, the low-swing register file can save a lot of power compared with other designs. The FOM (figure of merit) in Table 3 is calculated by the below expression.

$$\text{FOM} = \frac{\text{power}}{\text{frequency} \times N_{\text{ports}} \times N_{\text{bits}}}.$$

5. Conclusion

In this paper, a low-power multi-port register file has been designed by using a proposed low-swing strategy and a modified NAND address decoder. The low-swing strategy can save 34.5% and 51.15% power in WRITE and READ step separately when the data proportion of "0" is 0.5. The modified NAND decoder not only has the benefit in saving power, but also saves a lot of transistors in implementation. After the post simulation, the LSRF can save about 39.4% on average with all data ports working, and the peak current has been reduced greatly.

References

[1] Zyuban V, Kogge P. The energy complexity of register files. Proc ISLPED, 1998: 305
[2] K W Mai, T Mori, B S Amrutur, et al. Low-power SRAM design using half-swing pulse-mode techniques. IEEE J Solid-State Circuits,1998, 33(11): 1659
[3] Wang J S, Tseng W, Li H Y. Low-power embedded SRAM with the current-mode write technique. IEEE J Solid-State Circuits, 2000, 35(1): 119
[4] Yang B D, Kim L S. A low-power SRAM using hierarchical bitline and local sense amplifiers. IEEE J Solid-State Circuits, 2005, 40(6): 1366

[5] Sharifkhani M, Sachdev M. Segmented virtual ground architecture for low-power embedded SRAM. IEEE J VLSI, 2007, 15(2): 196

[6] Tremblay M, Joy B, Shin K. A Three dimensional register file for superscalar processors. Proc HICSS, January 1995: 191

[7] Yang H I, Chang M H, Lai S Y, et al. A low-power low-swing single-ended multi-port SRAM. International Symposium on VLSI Design, Automation and Test, April 2007: 25

[8] Yan Hao, Liu Yan, Wang Donghui, et al. A low-swing strategy in multi-port register file design. CSIE, 2011

[9] Turi M A, Delgado-Frias J G. Decreasing energy consumption in address decoders by means of selective precharge schemes. Microelectron J, 2009, 40: 1590

[10] Zhu Hao, Peng Chu, Wang Donghui, et al. high-performance framework for instruction-set simulator. CSIE, 2011

[11] Tzartzanis N, Walker W W, Nguyen H. A 34 word 64 b 10 r 6 w write-through self timed dual-supply-voltage register file. Proc Digest of Technical Papers IEEE International on Solid-State Circuits Conference, 2002, 1: 416

[12] Johguchi K, Aoyama K I, Suegoshi T, et al. Multi-bank register file for increased performance of highly-parallel processors. The Fifth Hiroshima International Workshop on Nanoelectronics for Tera-bit Information Processing, 2007

[13] Tzartzanis N, Walker W W. A differential current-mode sensing method for high-noise-immunity, single-ended register files. Proc Digest of Technical Papers IEEE International on Solid-State Circuits Conference, 2004: 506

[14] Dama J, Lines A. GHz asynchronous SRAM in 65 nm. Proc 15th IEEE Symposium on Asynchronous Circuits and Systems, 2009: 85