Properties of a Ni-FUSI gate formed by the EBV method and one-step RTA*

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Abstract: Nickel fully silicided (Ni-FUSI) gate material has been fabricated on a HfO_2 surface to form a Ni-FUSI gate/HfO_2/Si/Al (MIS) structure by using an ultra-high vacuum e-beam evaporation (EBV) method followed by a one step rapid thermal annealing (RTA) treatment. X-ray diffraction (XRD) and Raman spectroscopy were used to reveal the microstructures and electrical properties of the MIS structure. Results show that a one step post RTA treatment is enough to promote the full reaction of nickel silicide, compared with multiple RTA treatments. Furthermore, the HfO_2 gate dielectric film is sensitive to heat treatment, and multiple RTA treatments can damage the electrical properties of the HfO_2 film rather than improve them. By optimization of the sample fabrication technique, the MIS capacitor produces good high-frequency capacitance–voltage curves with a hysteresis of 30 mV, a work function of about 5.44–5.53 eV and leakage current density of only 1.45×10^{-8} A/cm^2 at –1 V gate bias.

Key words: Ni-FUSI gate; EBV; HfO_2
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1. Introduction

Metal gates for use in advanced complementary metal–oxide–semiconductor (CMOS) technology have attracted enormous research attention[1−3]. A nickel fully silicided (Ni-FUSI) gate has been considered as one of most promising candidates due to its compatibility with conventional CMOS technology, its low resistivity, and low consumption of Si[3−5]. To improve the performance of the sub-45 nm CMOS devices, a Ni-FUSI gate fabricated on a Hf-based high dielectric constant (high k) film is one possible way to replace the conventional poly-Si/SiO_2 gate stack[6].

It has been reported that the Ni-FUSI gate can be fabricated using the following methods[3, 6−8]. A poly-Si layer is first deposited on a high k gate dielectric film by low-pressure chemical vapor deposition (LPCVD) at a temperature of 600 ℃. Then the Ni film is grown by physical vapor deposition (PVD) or the EBV method. Finally, two-step post rapid thermal annealing (RTA) treatments are performed to form nickel silicide phases. Although the RTA technique is used to treat the sample instead of the regular thermal annealing treatment to reduce the thermal budget, HfO_2 gate dielectric films are still repeatedly annealed. Multiple annealing could promote HfO_2 film crystallization, which leads to an increase in leakage current.

In this paper, in order to further reduce the influence of the thermal annealing process on the formation of poly-crystal structures of a HfO_2 gate dielectric film, we propose one method with a one-step RTA treatment of Si and Ni films deposited on a HfO_2 gate dielectric by the EBV method at room temperature. Raman spectroscopy and XRD are employed to study microstructures of Ni-FUSI gate materials. Electrical properties of Ni-FUSI gate/ HfO_2/Si/Al capacitors have been analyzed.

2. Experimental

P-type Si(100) wafers with a resistivity of 7–13 Ω·cm were used as substrates. After a standard cleaning process with tools made by the Radio Corporation of America (RCA), substrates were loaded into a plasma atomic layer deposition (PEALD) chamber, where in situ NH_3 plasma nitridation was performed to passivate the Si surface[9]. Then a 7 nm HfO_2 film was grown on the Si substrate at 150 ℃. After the growth of the HfO_2 film, the samples were put into an EBV chamber and deposition of a 100 nm Si film and an 80 nm Ni film at room temperature took place. Finally, one-step RTA was performed on the samples at 500 ℃ in a N_2 environment for 60 s for nickel silicidation. Because the Ni film was in excess in this experiment, the excessive nickel was expected to survive on the sample surface after the reaction between the silicon and the nickel. To avoid the influence of residual nickel on device performance, we used an SPM (sulfuric-peroxide mixture) solution ($H_2SO_4 : H_2O_2 = 3 : 1$) to etch away the unreacted nickel with enough etching time after the RTA treatment. For comparison, we fabricated two other types of samples. One sample was produced without an RTA treatment after the growth of the Si and Ni films, denoted as the as-deposited sample. Another sample was annealed by a traditional two-step RTA processes (500 ℃ for 60 s + 600 ℃ for 60 s) after growth of the Si and Ni films. Rigaku D/max 2000 X-ray diffraction (XRD) and JY-T64000 Raman spectroscopy were used to investigate the microstructures of nickel silicide films.

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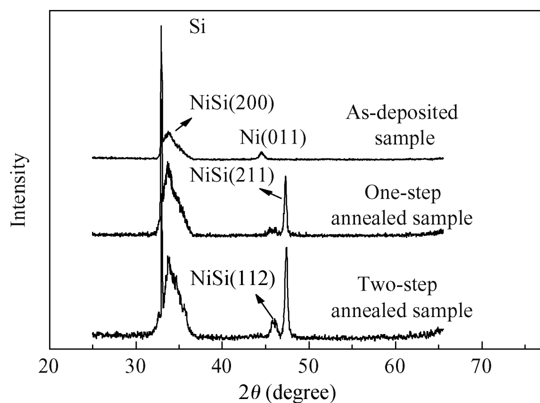

Fig. 1. XRD results.

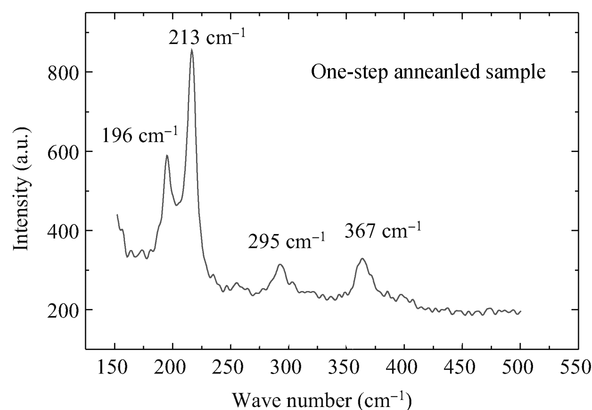

Fig. 2. Raman result of the sample.

To complete the MIS capacitor structure, for a part of the samples, Si and Ni were deposited through a shadow mask to form top electrodes. A back electrode was fabricated with a 100 nm aluminum film. The leakage current density (J–V) and the capacitance (C–V) of MIS capacitors were characterized by an Agilent 1500A semiconductor parameter analyzer and an Agilent 4284A Precision LCR meter at 100 kHz, respectively.

3. Results and discussion

XRD results of ω–2θ scans are shown in Fig. 1. A small peak related to NiSi(200) is observed in the as-deposited sample, indicating the formation of a small quantity of NiSi crystal even without the annealing treatment. A Ni(011) peak of the as-deposited sample can also be found in the figure due to the deposition of a pure Ni film covering the sample. What is more, the Si film grown by EBV in the as-deposited sample is amorphous[10], and no diffraction peaks from the Si film are observed as expected. After the one-step annealing treatment, the NiSi(200) peak increases its intensity due to the full reaction between the Si and Ni. Other NiSi crystal domains with different crystal orientations such as NiSi(112) and NiSi(211) have also been observed after the one-step annealing treatment. To the sample treated by the two-step RTA processes, we find that more crystal domains are formed in the NiSi film with an increasing intensity of NiSi(112) and NiSi(211) diffraction peaks. Thus, we can draw the conclusion that the advantage of the one-step annealing treatment over the traditional two-step annealing treatment is that it prevents the formation of NiSi crystal domains. In the XRD result, no other nickel silicide phases such as $NiSi_2$ are observed, showing that only one NiSi phase exists in the film.

Raman spectrum of a silicide material could be considered as a material fingerprint and used for phase identification[11]. As shown in Fig. 2 for the sample treated with a one-step RTA process, four Raman peaks at 196, 213, 295, and 367 cm^{-1} can be clearly observed. The four peaks are the exact fingerprint of the NiSi material[12]. The three peaks of 213, 295, and 367 cm^{-1} should be assigned A_g symmetry while the peak at 196 cm^{-1} shows B_{3g} symmetry[13]. Due to $NiSi_2$ forms at temperatures higher than 750 ℃[14], no Raman peaks of $NiSi_2$ are observed in the film, which is coincident to the XRD result. In the two-step RTA annealed samples, small changes of domain orientation are observed in the XRD patterns with increasing relative intensity of the NiSi(112) and NiSi(211) diffraction peaks, but no significant changes can be observed in the Raman spectrum (figure not shown) as the non-polarized Raman cannot be used to find the orientation of the crystal. For a perfect NiSi crystal, the intensity of the 213 cm^{-1} peak is higher than that of 196 cm^{-1} peak due to a larger Raman scattering cross section of the 213 cm^{-1} peak than the 196 cm^{-1} peak[15]. The Raman result in Fig. 2 shows that the sample treated by the one-step annealing process has a highly uniform NiSi phase structure.

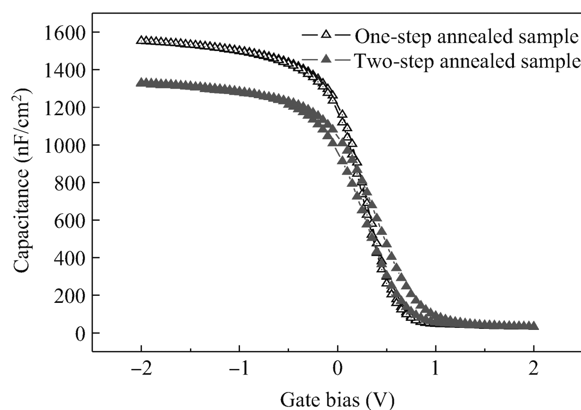

Fig. 3. High-frequency (100 kHz) C–V curves for Ni-FUSI/ HfO_2/Si gate stacks on the p-Si substrate.

The electrical properties of Ni-FUSI gate/HfO_2/Si/Al MIS capacitors are analyzed (Fig. 3) with excellent high-frequency capacitance–voltage (C–V) curves where the accumulation region is flat and the transition from accumulation to inversion is sharp. The maximum accumulation capacitance is calculated to be 1560 nF/cm^2. The flat band voltage (V_{FB}) and equivalent oxide thickness (EOT) estimated from the C–V curves are 0.5 V and 2.21 nm, respectively. The work function of the Ni-FUSI gate can be obtained from the following equation:

$$V_{FB} = \frac{W_M - W_S}{q} - \frac{Q_f}{\varepsilon_{OX}\varepsilon_0}\mathrm{EOT},$$

with the work function of the Si substrate (W_S) as 4.93 eV. Considering the error allowance of the fixed charged density Q_f ranging from 10^{11} to10^{12} cm^{-2}[16–19], the calculated effective

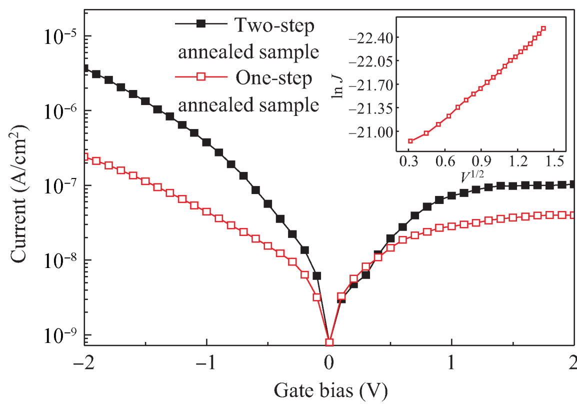

Fig. 4. Leakage current densities of Ni-FUSI/ HfO_2/Si gate stacks MIS capacitors under gate injection conditions. Inset is the plot of $\ln J$–$V^{1/2}$.

work function of the Ni-FUSI gate (W_m) is about 5.44–5.53 eV, larger than the reported data[1, 2, 7, 20], indicating that our one-step annealing treatment can improve device performance.

Notice that when the C–V curve is swept from accumulation to inversion and back to accumulation, it shows a small negative shift of 30 mV. This hysteresis may be caused by the movable Ni ions. For a two-step annealed sample, the maximum accumulation capacitance is reduced markedly and the hysteresis increases. This is because of a thickening of the interfacial layer and degeneration of the interface quality, which is caused by multiple high temperature treatments.

J–V curves of MIS capacitors under gate injection conditions are shown in Fig. 4. For the one-step annealed sample, the leakage current density is 4.43×10^{-8} A/cm^2 at a –1 V gate bias, which is four orders of magnitude smaller than the reported values for Ni-FUSI/ HfO_2/Si gate stacks[2, 6]. For the two-step annealed sample, the leakage current increases significantly due to the additional high-leakage path along the grain boundaries through the polycrystalline dielectric, indicating that the HfO_2 gate dielectric film is very sensitive to heat treatment.

To clarify the conduction mechanism of the leakage current, the logarithmic current density $\ln J$ versus the square root of the gate voltage is plotted and shown in the inset figure in Fig. 4. A fair linear tendency of the plot for $\ln J$ versus $V^{1/2}$ is achieved, indicating that Schottky emission is the dominant current conduction mechanism. The plot for $\ln(J/V)$ versus $V^{1/2}$ is not a straight line (figure not shown), suggesting that Poole–Frenkel emission is not a primary conduction mechanism and the NiSi/HfO_2 interfacial state density is low.

4. Conclusion

In this work, the Ni-FUSI gate has been deposited on a HfO_2 gate dielectric and the electrical properties of Ni-FUSI/HfO_2/Si/Al stacks are investigated. The results of XRD and Raman measurements demonstrate that the one-step RTA treatment of Si and Ni evaporated by EBV at room temperature can improve the electrical properties of the MIS structure. The one-step RTA treatment can decrease thermal damage to the electrical properties, compared with the two-step annealing treatment.

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