Metal gate etch-back planarization technology*

Meng Lingkuan(孟令款)†, Yin Huaxiang(殷华湘)†, Chen Dapeng(陈大鹏), and Ye Tianchun(叶甜春)

Key Laboratory of Microelectronics Devices of Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

Abstract: Planarization used in a gate-last CMOS device was successfully developed by particular technologies of SOG two-step plasma etch-back plus one special etch-back step for SOG/SiO_2 interface trimming. The within-the-wafer ILD thickness non-uniformity can reach 4.19% with a wafer edge exclusion of 5 mm. SEM results indicated that there was little "dish effect" on the 0.4 μm gate-stack structure and finally achieved a good planarization profile on the whole substrate. The technology provided a CMP-less process basis for sub-100 nm high-k/metal gate-last CMOS integration.

Key words: metal gate; plasma etch-back; planarization; spin on glass

DOI: 10.1088/1674-4926/33/3/036001 **EEACC:** 2570

1. Introduction

Recently, a high-k/metal gate for better short-channel-effect control has been successfully implemented into advanced CMOS technologies. Gate-last process flow has also proved an effective method for high-k/metal gate integration. However, new process challenges are emerging continuously; planarization of the interlayer dielectric (ILD) for dummy gate open is one of the critical technologies for high-k/metal gate-last integration, which is not available in traditional gate-first CMOS process flow.

Normally, the deposited dielectric film on poly-silicon gate lines introduces a non-planar surface across the chip surface. Therefore, how to get a planar ILD surface will have a strong influence on subsequent processes of selectively etching dummy gates in an ILD layer. While metal fills a dummy gate in a rough ILD surface, considerable metal residue will produce and induce device reliability issues for thickness variations. For a long time, several planarization methods such as spin on glass (SOG)[1−4], BPSG reflow[4], plasma etch-back[5, 6] and advanced chemical mechanical polish (CMP)[7] technology, etc. have been extensively developed for normal ILD planarization for interconnection in the back-end-of-line. Recently, CMP technology was introduced into ILD planarization for a high-k/metal gate-last CMOS process, and also applied to metal gate planarization. Steigerwald[7], Achard[8], and Diao[9] presented a lot of research work for this technology and achieved superior planarization results for both the ILD and metal gate.

However, since it is very difficult to consistently control the chemical solution proportion in a CMP slurry and the cost of a mechanical polisher in a CMP tool is high[10], the total process cost will be great for common gate-last device fabrication. In addition, as the device dimensions scale to 45 nm and beyond, keeping a reliable and cost effective CMP performance presents a lot of challenges: uniformity issues, topography and low defect control.

Plasma etch-back has been a general advantage in sub-micron CMOS fabrication; it normally requires a lower cost and less process complexity than CMP technology. Through etch-back composite dielectric films like SiO_2 combining with SOG, a similar result to CMP can be achieved. In addition, since etch-back technology has good compatibility with traditional processes, it will have little effect on device performance[11].

To realize a gate-last integration process, the authors successfully developed special technologies of SOG two-step plasma etch-back plus one special etch-back step for SOG/SiO_2 interface trimming, which provided a good basic isolation structure for beneath dummy gate removal and high-k/metal gate integration.

2. Experiment

The substrate is a 100 mm (4 inch) wafer and a dry etch is processed in a LAM Rainbow 4520 tool with the reactive-ion-etch (RIE) model. Its upper electrode has a ground connection and the lower electrode connects to a 13.56 MHz RF power supply. Plasma density and energy are both controlled by the lower electrode RF, which presents a large challenge for superior planarization performance. The etch gas includes CF_4, CHF_3, Ar and O_2. The main parameters that effect the SiO_2 and SOG etch rate are RF power, gas flow and its proportion.

A thickness measurement was performed using AFT film metrology equipment made by American NANOSPEC Company. Etch rate can be calculated by measuring ILD thicknesses of pre and post etch. The cross-sectional view and topography detection of the wafer sample were characterized by a Hitachi S4800 SEM tool.

* Project supported by the Chinese National Science and Technology Major Project (No. 2009ZX02035), the Special Funds for Major State Basic Research Projects, China (No. 2006CB302704), and the Opening Project of Key Laboratory of Microelectronics Devices of Integrated Technology (IMECAS).

† Corresponding author. Email: menglingkuan@ime.ac.cn, yinhuaxiang@ime.ac.cn

Received 26 August 2011, revised manuscript received 12 October 2011

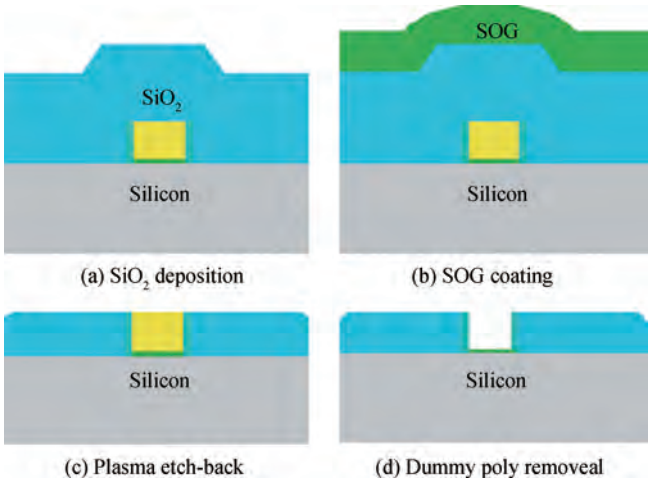

Fig. 1. ILD plasma etch-back process flow.

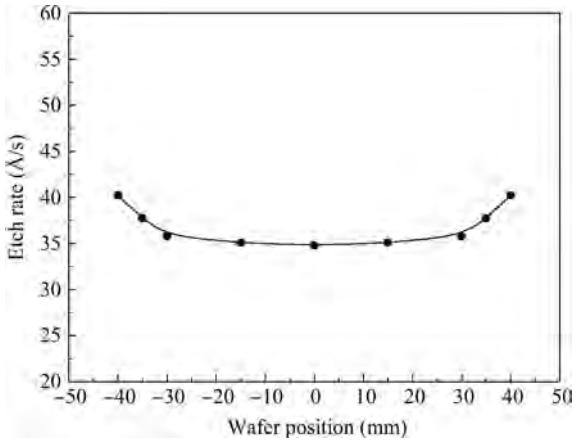

Fig. 2. SOG etch rate profile with a traditional RIE recipe.

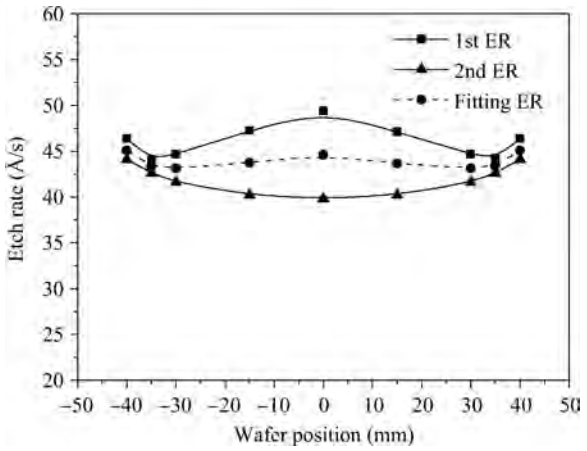

Fig. 3. SOG etch rate profile with a new developed technology.

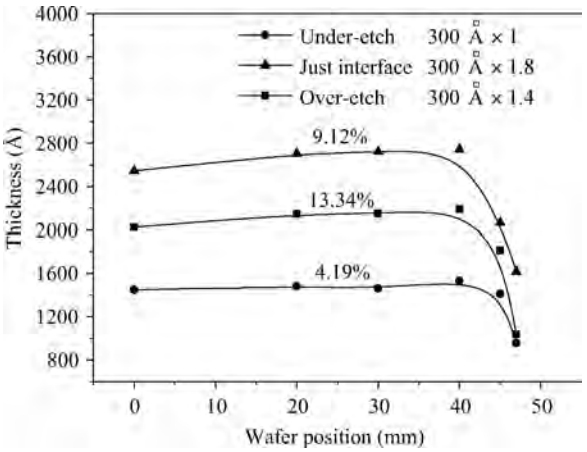

Fig. 4. SOG etch stop location split test results.

The ILD stack structure and plasma etch-back process flow are shown in Fig. 1. Firstly, a 8000 Å thick SiO_2 is deposited on a pre-formed device structure such as poly-Si dummy gate and spacers for contact isolations, and then a 4000 Å thick SOG is coated on the wafer followed by a curing process for a more uniform surface (Fig. 1(a)). Subsequently, a 2-step plasma etch-back is performed until underneath the SOG/SiO_2 interface (Fig. 1(b)); then another etch-back step is performed to obtain the desired surface (Fig. 1(c)). Finally a dry or wet etch process is carried out to remove the poly dummy gate for subsequent metal electrode filling (Fig. 1(d)).

3. SOG/SiO_2 planarization fundamental and process

Traditional SOG etch-back technology cannot provide a superior etch uniformity, which is attributed to greater polymer generation during the SOG etch. Furthermore, due to the pressure difference within the etch chamber, a different amount of polymer generation in a different area determines a varying etch rate. This is shown in Fig. 2, where the x-axis represents the wafer position dimension range from –50 to 50 mm on the 4 inch (100 mm) wafer diameter, and the y-axis indicates the SOG etch rate. In this figure, the central SOG etch rate is slower than that of wafer edge area; therefore, the thickness profile is a concave shape across the whole wafer. In the following SiO_2 etch, the dielectric layer in the wafer edge area will be over etched, however, the central area is under etched, which makes etch uniformity even worse[12, 13].

To solve this issue, we developed a two-step plasma etch-back combined with O_2 *in-situ* plasma treatment technology that can effectively suppress polymer impact on RIE. Namely, one common plasma etch process is split into two steps and every etch step adds an O_2 *in-situ* plasma treatment to remove polymer accumulation. In particular, tuning of the chamber pressure, power and gas and gas proportion can achieve a preferred etch rate profile. In the first step, the etch rate profile in the central area shows a convex shape and in the second step, the corresponding etch rate profile demonstrates a concave shape. The profile of the fitting of these two step etch rates indicates a more uniform distribution, which is shown in dashed line of Fig. 3.

In the area of the local devices, due to dummy poly-Si gate protrusion, the subsequently deposited SiO_2 and coated SOG produced non-planar step coverage, so induced a different etch rate on the whole wafer. In the SOG etch process, SiO_2 to SOG demonstrates a 2.3 : 1 etching selectivity. On the other hand, a special etching process is developed for SiO_2/SOG interface trimming. A method with a 1 : 1 etch selectivity of SiO_2 to SOG

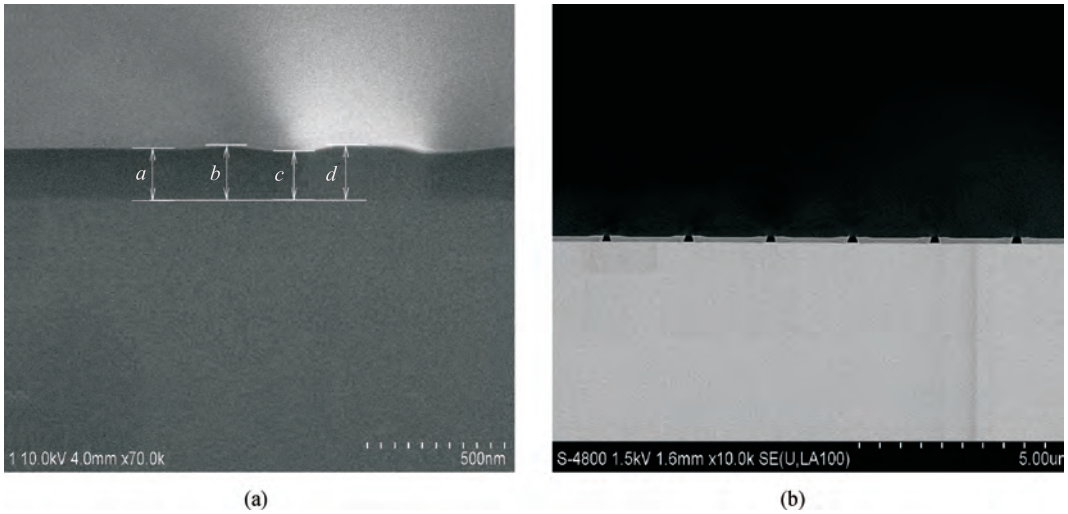

Fig. 5. Cross-sectional view of ILD planarization on (a) sub-micrometer gate line and (b) dense gate-line array with the optimized method. *a*: 153 nm; *b*: 160 nm; *c*: 142 nm; *d*: 160 nm.

is adopted to remove the step height difference of the dummy poly-Si gate. Three split tests are performed to find a proper SOG etch stop location including (1) a SiO_2 under-etch 300 Å plus 1 : 1 interface etch stop, (2) just at the interface and (3) a SiO_2 over-etch 300 Å are performed. Figure 4 shows the test results with different split etch-back methods. In the figure, there are two curves enlarged by 1.4× and 1.8× respectively for better comparison. An under etch 300 Å split demonstrates a maximal effective work region and the optimum uniform performance. Here, the effective work region means a valuable radius scope representing the final ILD thickness drifting 150 Å from the targeted object of 1500 Å (1500 ± 150 Å).

The test results clearly demonstrate that the etch rate uniformity depends on different approaches described previously. The method of under-etch 300 Å plus 1 : 1 interface trimming shows an excellent non-uniformity 4.19% (exclude edge 5 mm). On the other hand, the non-uniformity result is the worst at 13.34% when SOG etching is just stopped at the interface. However, when SiO_2 is over etched, non-uniformity can be improved to 9.12% compared with the split (2) condition. All these data show that the SOG etch stop location has a critical effect on the final ILD thickness uniformity, which is attributed to less polymer accumulation during the SOG under-etch and the SiO_2/SOG 1 : 1 etching.

However, if the SOG etch just stops at the interface and the normal SiO_2 etch step is applied, the etch-back process generates considerable polymer accumulation to affect etch rate distribution among different local device regions. As a result, the etch rate between the upper-SOG and lower-SiO_2 shows some differences from the normal etch recipe, which makes some regions over etched and others perhaps under etched. Therefore, with the SiO_2 etch ongoing, the etch rate of the exposed SiO_2 region is faster than that of the under-exposed region. It causes a considerable thickness variation in random regions and induces serious non-uniform phenomena. In the method of SiO_2 over-etch 300 Å, the interface etch is also affected by the above phenomena and the non-uniformity (9.12%) is a little worse than that of method (1).

With the optimized etch-back approach, the planar ILD distribution on a 0.4 μm dummy poly-Si gate stack is achieved and shows little of the "dish effect" that often happens in the CMP process. Figure 5 shows the cross-sectional SEM results of this experiment on an isolated gate line as well as the dense gate-line array where dummy poly-Si gates have been selectively removed. On the other hand, since the devices fabricated with a thin ILD layer on silicon wafers are usually directly exposed to plasma during the plasma etch process, charge collection may cause IC yield loss on the devices as well as reliability issues. The residual polymer of the etch also needs an additional cleaning step for subsequent process integration.

4. Conclusion

In exploring the nanometer-level CMOS gate last process, a two-step plasma etch-back combined with O_2 in-situ treatment technology as well as a special 1 : 1 SOG/SiO_2 interface trimming process were developed. These could effectively suppress the effect of polymer accumulation during an SOG etch. Finally a 4.19% ILD non-uniformity within-the-wafer (exclude edge 5 mm) was achieved. The technology reduced loading effect by a faster etch rate in the wafer's central area and produced an excellent planarization result for ILD with little of the "dish effect", often seen in CMP. This technology provides a useful planarization alternative for sub-100 nm high-*k*/metal gate-last integration via a CMP-less approach and also decreases greatly the process cost.

References

[1] Chung H W M, Gupta S K, Baldwin T A. Fabrication of CMOS circuits using non-etchback SOG processing for dielectric planarization. VLSI Multilevel Interconnection Conference, Santa Clara, CA, 1989: 373

[2] Kawai M, Matsuda K, Miki K, et al. Interlayered dielectric planarization with TEOS-CVD and SOG. VLSI Multilevel Interconnection Conference, 1988: 419

[3] Whitwer F, Davies T, Lage C. Premetal planarization using spin-on-dielectric. VLSI Multilevel Interconnection Conference, 1989: 96

[4] Bogle-Rohwer E, Nulty J, Chu W, et al. Spin-on-glass/phosphosilicate glass etchback planarization process for 1.0 μm CMOS technology. Advanced Techniques for Integrated Circuit Processing, 1991, 1392: 280

[5] Davari B, Koburger C W, Schulz R, et al. A new planarization technique, using a combination of RIE and chemical mechanical polish (CMP). Electron Devices Meeting, 1989: 61

[6] Andre S, Laetitia P, Maryse P, et al. Plasma etch-back planarization coupled to chemical mechanical polishing for sub 0.18 μm shallow trench isolation technology. J Vac Sci Technol A, 2000, 18(4): 1313

[7] Steigerwald J M. Chemical mechanical polish: the enabling technology. Electron Devices Meeting, 2008: 61

[8] Achard H, Ducroquet F, Coudert F, et al. Full CMP integration of TiN damascene metal gate devices. Proceeding of the 30th European Solid-State Device Research Conference, France, 2000: 408

[9] Diao J, Leung G, Qian J, et al. ILD0 CMP: technology enabler for high k metal gate in high performance logic devices. Advanced Semiconductor Manufacturing Conference (ASMC), San Francisco, CA, 2010: 247

[10] Zhao Xiaohui, Li Hong, Sun Xiangran. The technology of agent planarization in several layers of metal process. MIC Roproces Sors, 2004, (4): 8

[11] Li Hongzheng, Chen Haifeng, Guo Jinglei. SOG local planarization technology study. Electronics & Packaging, 2002, 2(5): 17

[12] Keelung H C. Two step etch back process having a convex and concave etch profile for improved etch uniformity across a substrate. USA Patent, No.5639345, 06/17/1997

[13] Keelung H C. Spin-on-glass etchback planarization process using an oxygen plasma to remove an etchback polymer residue. USA Patent, No. 5679211, 10/21/1997