A low power 2.5–5 GHz low-noise amplifier using 0.5-μm GaAs pHEMT technology*

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Abstract: A two-stage 2.5–5 GHz monolithic low-noise amplifier (LNA) has been fabricated using 0.5-μm enhanced mode AlGaAs/GaAs pHEMT technology. To achieve wide operation bandwidth and low noise figure, the proposed LNA uses a wideband matching network and a negative feedback technique. Measured results from 2.5 to 5 GHz demonstrate a minimum of 2.4-dB noise figure and 17-dB gain. The input and output return loss exceeded –10-dB across the band. The power consumption of this LNA is 33 mW. According to the author's knowledge, this is the lowest power consumption LNA fabricated in 0.5-μm AlGaAs/GaAs pHEMT with the comparable performance.

Key words: LNA; GaAs pHEMT; MMIC; microwave

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1. Introduction

Low noise amplifiers (LNAs) are critical components in any receiver system. The development of modern radar and wireless applications necessitate next generation receivers with wideband frequency range, such as S-band and C-band radars, ultra-wide-band (UWB), and software-defined radios. The power consumption is also critical under many applications. The aim of this work is to produce a low noise, high gain, and low power LNA for wireless applications.

The high yield and reliability make GaAs MMIC a reliable technology and is widely adopted for the realization of circuits and subsystems for microwave and millimeter wave applications. Though some new processes and technology of III–V compounds have been developed to provide better performance, the yield is still a problem and not reliable for commercial use[1, 2]. Although higher gain GaN devices are starting to make a significant impact in wireless applications with better power performance, the cost and power consumption are still problems for wildly use. Silicon substrate technology such as CMOS and BiCMOS processes have achieved cut-off frequencies over 300 GHz. However the critical components of the systems, such as the ultra-low-noise wideband amplifier, high power amplifier and switch, are still need to develop with GaAs technology due to the good performance and high reliability.

There are some previous woks published designing low noise amplifiers around the S-band and C-band in recent publications aiming at low noise or low voltage applications[4−10]. In this paper, a low power, high gain LNA MMIC is implemented in a commercial 0.5 μm AlGaAs/GaAs pHEMT technology and achieves a 2.4–3 dB noise figure in 2.5–5 GHz frequency range. The gain of the LNA is greater than 17 dB through the working frequency. The LNA topology was selected to also achieve flat gain and 50 Ω input and output match over a wide frequency range. The output P_{1dB} is 2.3 dBm. The LNA occupies 1.5 mm^2 and dissipates 33 mW with 1.5 V power supply. This paper will also summarize the design, fabrication, and measured performance of the low power, low noise GaAs pHEMT LNA.

2. Circuit design and layout consideration

The proposed LNA is designed using 0.5 μm low noise AlGaAs/GaAs enhanced mode pHEMT technology. To design a low power low noise amplifier, many trade-offs must be taken into consideration. In this paper, two amplifying stages are utilized to produce enough gain for trade-off.

The schematic of the LNA is shown in Fig. 1. The first stage has been designed to obtain the low noise figure of the circuit. Utilizing source degeneration technical with common source topology, the input return loss and noise match can be

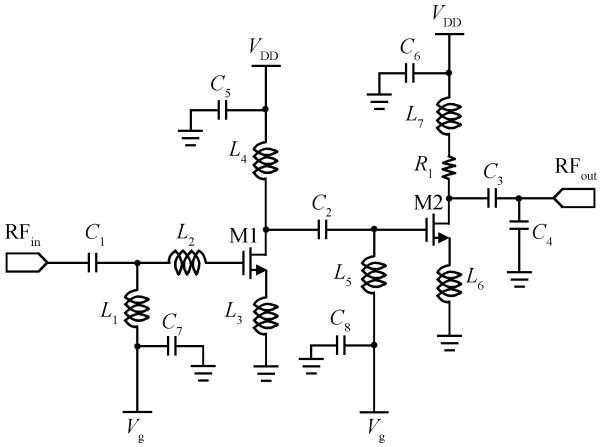

Fig. 1. Schematic of the proposed LNA.

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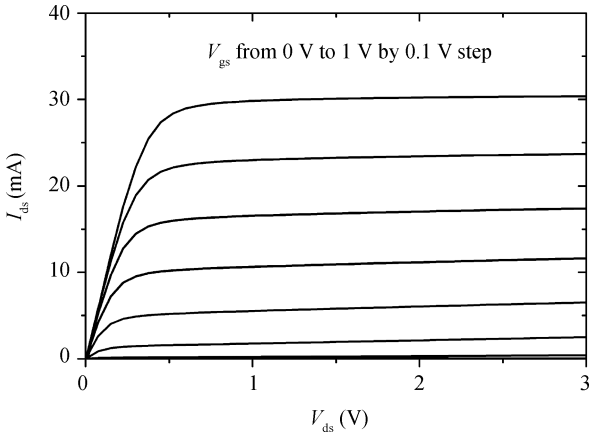

Fig. 2. DC-I–V characteristics of the FET.

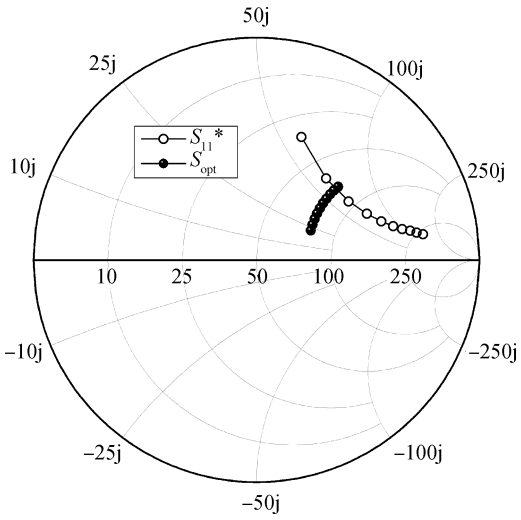

Fig. 3. S_{opt} and conjugate of S_{11} versus source degeneration inductors.

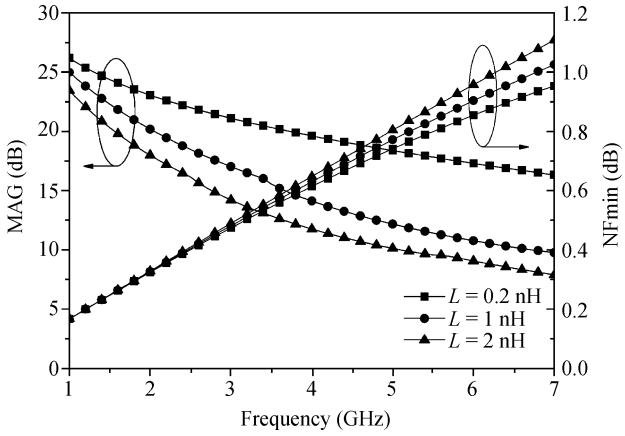

Fig. 4. Simulation of MAG/MSG and NFmin of the first stage with various source degeneration inductor values.

achieved simultaneously. The central frequencies of the two stages have been designed to have little differences to get a wideband frequency response. The input and output are all matched to 50 Ω through the matching network. Lossy matches are placed at the output to make a stable gain as well as not to deteriorate the noise figure. The DC-I–V character of the FET with 200 μm gate width is shown in Fig. 2.

2.1. Design for low noise figure and low power

To design a low power amplifier, devices of smaller size are preferred because of the fewer power consumptions. Although smaller devices also have another advantage of higher maximum available gain, the linearity will be degraded.

In this work, the total gate width of the first stage is 200 μm and it is biased at V_{DD} =1.5 V; $V_G = 0.7$ V, with $I_{DD} = 11$ mA. The transistor is conditionally stable over the desired frequency band. To ensure the stability, source degeneration inductor is utilized. There is a trade-off between the stable condition, noise figure and the available gain.

To make the common source stage more stable and easily achieve noise match and input match simultaneously, the source degeneration inductor must be selected carefully. Figure 3 presents the S_{opt} and the conjugate of S_{11} at the operation frequency of 4 GHz with various L_s. As it shows, with proper selected of L_s, the matching of S_{opt} and S_{11} can be got simultaneously. Besides, the stability factor, maximum available gain and minimum noise figure are also need to be taken into consideration when selecting the inductor value. Figure 4 shows the simulation results of MAG/MSG and NF_{min} of the first stage with various source degeneration inductor values. When L_s = 2 nH, the amplifier cell is stable above 1 GHz and the minimum noise figure is also reduced, but the MAG/MSG is decreased by 10 dB comparing with simple common source cell. In this design, the source degeneration inductor is selected to be 1 nH. The amplifier cell is conditionally stable in the working frequency, matching networking are selected to keep the amplifier away from the unstable region.

To keep the overall LNA noise figure, the noise contribution of the second stage is minimized by matching the FET input near optimum noise match Γ_{opt}. A source degeneration inductor is also placed at the source to move the conjugate of the input reflection coefficient towards Γ_{opt}. The total gate width of the second stage is 200 μm and it is biased at $V_{DD} = 1.5$ V, $V_G = 0.7$ V, with $I_{DD} = 11$ mA.

2.2. Design for wideband

As shown in Fig. 5, to obtain a wideband performance, the central frequencies of the two stages have been designed to have a little difference. With this consideration, the gain of the two stages LNA will be more flat through the working band.

The matching network of the LNA is also carefully selected. The topologies are chosen individually for the input, output and inter stage matching to make a wideband input/output return loss. As shown in Fig. 6, the input and output impedance are matching to 50 Ω in the desire frequency range. The curves of S_{11} and S_{22} in Smith chart show that the wideband matching target is satisfied.

The negative feedback of source degeneration inductor makes the FET more stable. To further ensure the stability of the amplifier, lossy matches are utilized at the output of the third stage. The output is matched to 50 Ω for the on chip measurement.

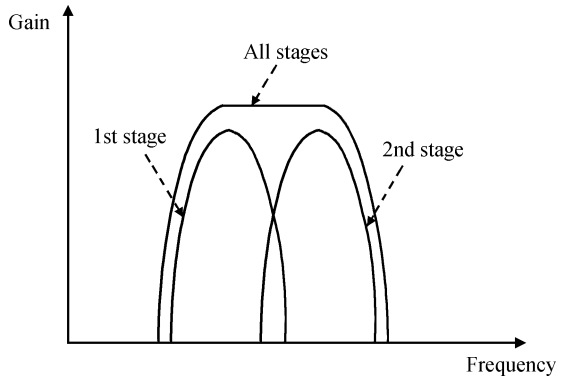

Fig. 5. Gain profiles of the two-stage LNA.

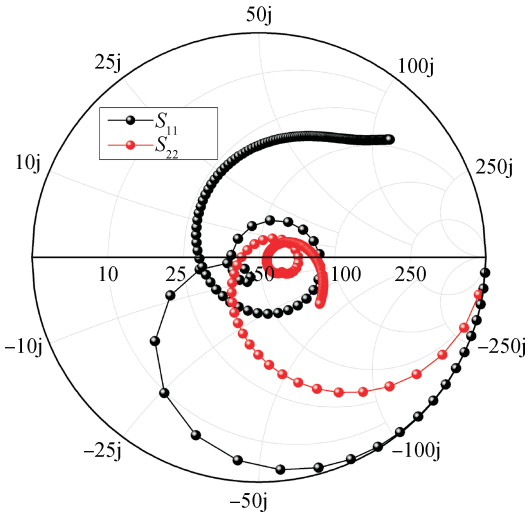

Fig. 6. Simulation of input/output S-parameters of the LNA.

2.3. Layout consideration

The dc biases are feed through RF chock inductors. In this design, the RF chock inductor values are properly selected as to share with the matching networks. The bypass capacitors are carefully designed. To realize the parasitic and coupling effects of the circuits, a commercial electromagnetic (EM) simulator is utilized to analysis the circuit. And the characters of the inductors in this design have been checked with measurement data to design the LNA accurately. Yield analysis was also utilized to keep the circuit not sensitive to process variation.

The gate and drain of each FET are connected to DC pads individually, allowing the bias condition of every stage can be adjusted separately. Ground–signal–ground (GSG) pads are used for on-wafer measurement. The dimension of the LNA chip is 1.5×1 mm^2. The chip photograph of the LNA is shown in Fig. 7.

3. Measured results

Performance of the wideband LNA was measured via on-wafer using Anritsu 37397D VNA and Agilent 8975A noise measurement equipment. Wafer-level calibration was performed to take cable and probe losses into account. The DC biases are fed using bond wires connected to a PCB test board.

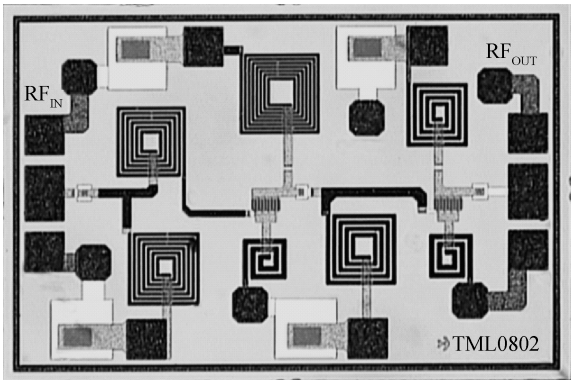

Fig. 7. Chip photograph of the LNA.

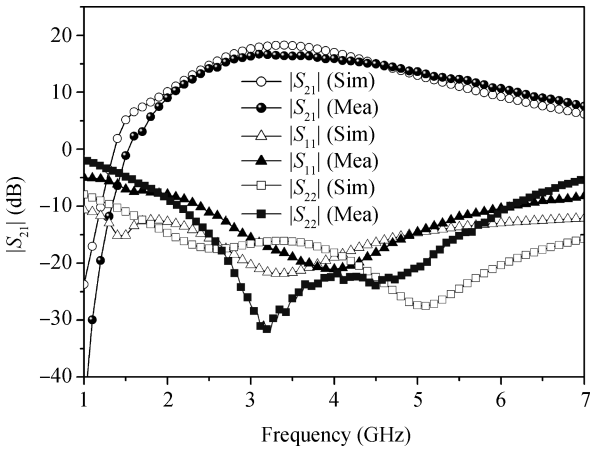

Fig. 8. Simulated and measured small signal gain and return losses of the LNA.

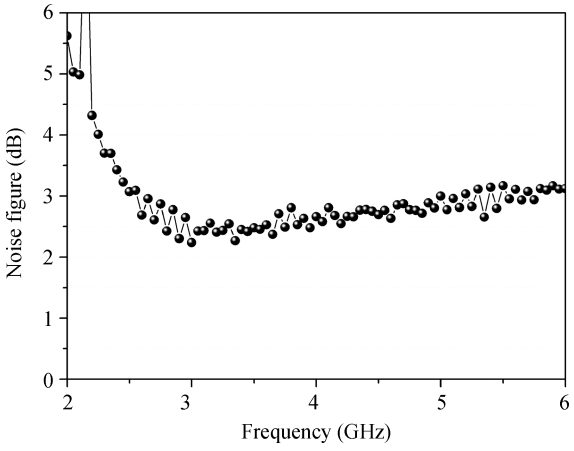

Fig. 9. Measured noise figure of the LNA.

The measured small signal gain and return losses of the LNA are shown in Fig. 8. The measured data fitted the simulated one very well. The average gain is 17 dB with flatness of 1.6 dB from 2.5 to 5 GHz. Input and output return losses over this band are less than 10 dB. The DC bias of this condition is $V_{DD} = 1.5$ V, $V_G = 0.7$ V, with $I_{DD} = 22$ mA.

Figure 9 illustrates the measured noise figure. The LNA has a noise figure of 2.4 to 3 dB from 2.5 to 5 GHz when the bias current is 33 mA. The power performances of the LNA

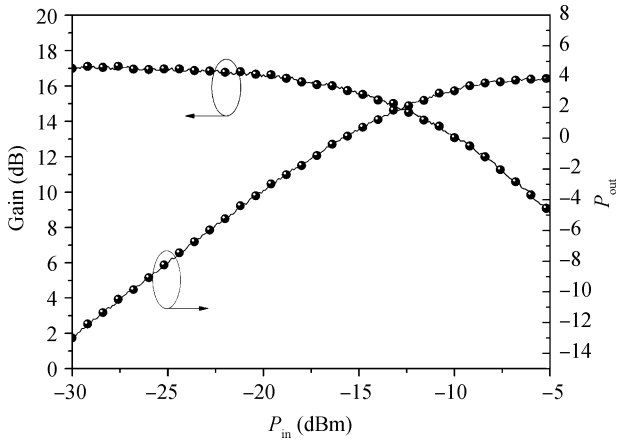

Fig. 10. Power performance of the LNA at 4 GHz.

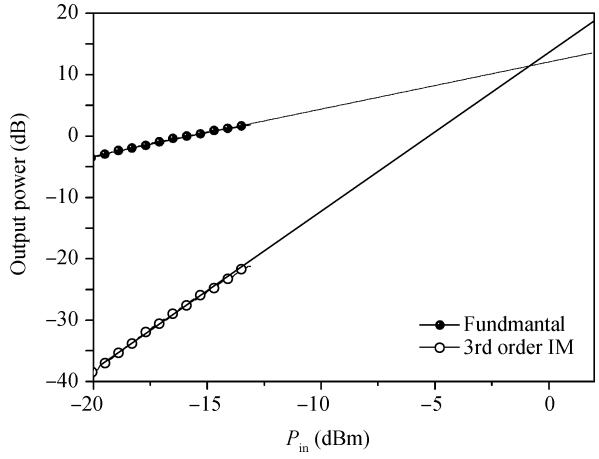

Fig. 11. Third-order intercept point of the LNA at 4 GHz.

are shown in Figs. 10 and 11. As Figure 10 shows, the LNA has an output P_{1dB} of 2.3 dBm with total power consumption of 33 mW. And as shown in Fig. 11, the IIP3 is –2 dBm.

4. Conclusion

A 2.5–5 GHz LNA has been fabricated using 0.5-μm enhanced mode AlGaAs/GaAs pHEMT technology. The LNA achieves good performance with 17 dB gain and 2.4 to 3 dB noise figure from 2.5 to 5 GHz. The LNA topology was selected to also achieve flat gain and 50-Ω input and output match over a wide frequency range. The LNA chip occupies 1.5 mm^2 and dissipates 33 mW with a 1.5 V power supply.

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