A fully integrated frequency synthesizer for a dual-mode GPS and Compass receiver

Chu Xiaojie(楚晓杰)[1,†], Lin Min(林敏)[1], Shi Yin(石寅)[1], and Dai F F(代伐)[2]

[1]Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China
[2]Department of Electrical & Computer Engineering, Auburn University, Alabama, 36849-5201, USA

Abstract: This paper presents a fully integrated frequency synthesizer for a dual-mode GPS and Compass receiver fabricated in a 0.13 μm CMOS technology. The frequency synthesizer is implemented with an on-chip symmetric inductor and an on-chip loop filter. A capacitance multiplying approach is proposed in the on-chip loop filter design for area-saving consideration. Pulse-swallow topology with a multistage noise shaping $\Delta\Sigma$ modulator is adopted in the frequency divider design. The synthesizer generates local oscillating signals at 1571.328 MHz and 1568.259 MHz with a 16.368 MHz reference clock by working in integer and fractional modes. Measurement results show that the phase noise of the synthesizer achieves –91.3 dBc/Hz and –117 dBc/Hz out of band at 100 kHz and 1 MHz frequency offset, separately. The proposed frequency synthesizer consumes 8.6 mA from a 1.2 V power supply and occupies an area of 0.92 mm^2.

Key words: fully integrated; frequency synthesizer; GPS; Compass
DOI: 10.1088/1674-4926/33/3/035004   **EEACC:** 2220

1. Introduction

Recently, there has been an increasing interest in global navigation satellite system (GNSS) research and applications. The integration of positioning capabilities into electronic and handheld devices is experiencing fast growth, and this demands a continuous reduction in power consumption and area cost. Further more, GNSSs include global positioning system (GPS), European navigation system Galileo, Russian Glonass and Chinese Compass. Therefore, there is a strong trend for future development to combine these GNSSs in a hybrid receiver. In this work, a dual-mode receiver for both GPS and Compass is presented. A block diagram of the receiver is illustrated in Fig. 1.

The RF signals of GPS (L1 band) and Compass centre on 1575.42 MHz and 1561.098 MHz separately. As shown in Fig. 1, low-IF architecture is preferred to zero-IF architecture for the following reasons. In spite of its simplicity and no image rejection issues, a zero-IF receiver has a few problems such as DC offset, I/Q mismatch, flicker noise, even-order distortion and local oscillator (LO) leakage, which are rather challenging to resolve. Nevertheless, low-IF architecture has image rejection issues. The adoption of complex active-RC filters offers a good solution to image suppression. As illustrated in Fig. 1, GPS and Compass systems share the same RF front-end, and then the down-converted IQ quadrature signals are sent to two different analog baseband chains for GPS and Compass separately. Occupying similar configurations, these two baseband chains are composed of 3rd Butterworth complex band-pass filters (BPFs) with programmable bandwidth, programmable gain amplifiers (PGAs) and analog-to-digital converters (ADCs).

A frequency synthesizer is a key building block in an RF receiver. Phase noise performance of the synthesizer has an important effect on the sensitivity and dynamic range of the receiver. As far as this dual-mode receiver is concerned, the target phase noise performance is –80 dBc/Hz in band and –110 dBc/Hz out of band. A fully integrated frequency synthesizer which can work in both integer and fractional mode is introduced for this hybrid receiver application. This paper will focus on the design of this frequency synthesizer. Figure 2 shows the block diagram of the proposed frequency synthesizer.

As illustrated in Fig. 2, the proposed synthesizer adopts the charge pump (CP) based phase-locked loop (PLL) structure. The PLL is composed of a crystal oscillator, a phase-frequency detector (PFD), two charge pumps with a capacitance multiplying approach, an on-chip loop filter, a voltage-controlled oscillator (VCO), a VCO buffer, an LO quadrature generator, and a fractional-N frequency divider. The crystal oscillator is responsible for providing an accurate and clean input reference signal to the frequency synthesizer. Then, the PFD detects the phase and frequency differences between the reference signal and the output signal of the frequency divider. The following CP injects an output current proportional to the differences detected by the PFD into the loop filter to adjust the control voltage on VCO. The 3rd-order loop filter implementing with a capacitance multiplying approach filters out the high frequency components and extracts an average VCO voltage to improve the noise performance of the VCO. The VCO is adjusted by the feedback loop so the PLL can be locked at the desired frequency. LO quadrature signals are generated by a divide-by-2 block and then sent to the mixer by LO buffers. A programmable frequency divider is included in the feedback path for channel selection. This frequency divider is based on the pulse-swallow topology incorporating a 3rd multistage noise shaping (MASH) $\Delta\Sigma$ modulator with noise-shaped dithering techniques, which is used for phase noise and spur reduction considerations. The feedback signal output by the fractional-N frequency divider is re-synchronized by the output of the LO buffer in order to reduce the noise produced by the fractional-
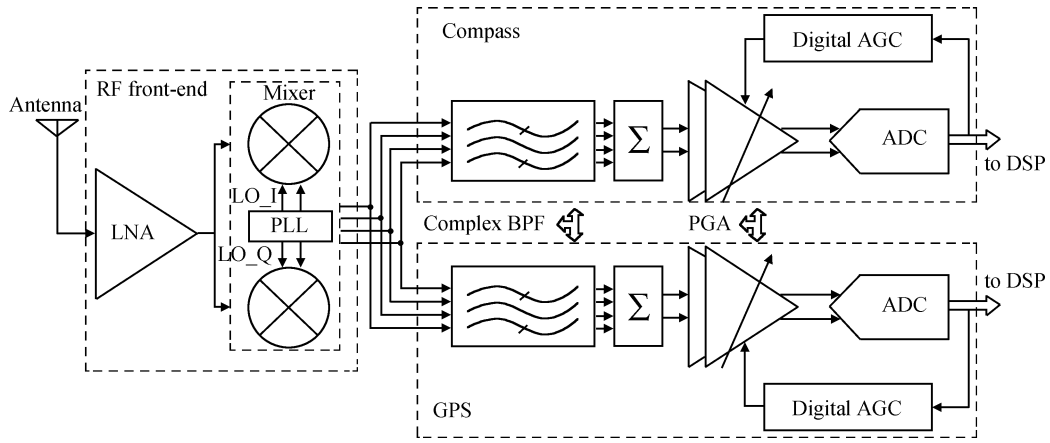

Fig. 1. Block diagram of the proposed dual-mode receiver for GPS and Compass.
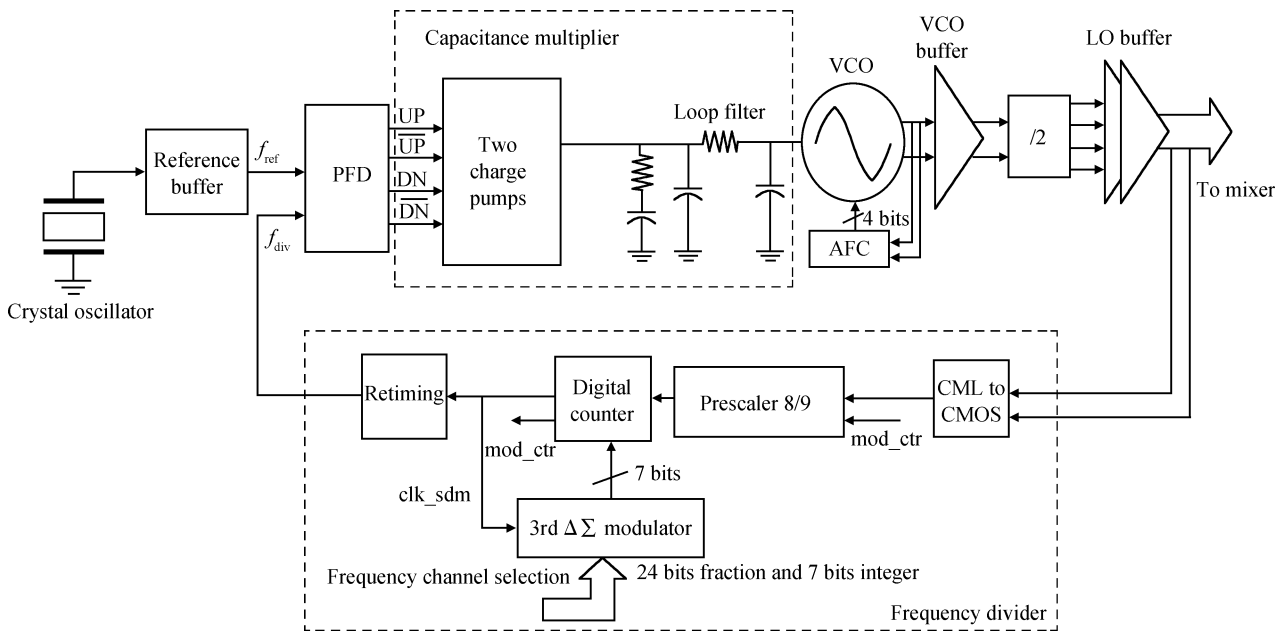

Fig. 2. Block diagram of the proposed frequency synthesizer.

N frequency divider.

2. Circuit design and analysis

2.1. Frequency planning

As given in Table 1, the RF signals of GPS and Compass centre on 1575.42 MHz and 1561.098 MHz respectively. There are two options of LO centre frequency for the synthesizer, 1571.328 MHz and 1568.259 MHz. Thus, the down-converted IF can be 7.161 MHz for both Compass and GPS, or 10.023 MHz for Compass and 4.092 MHz for GPS, separately. The choice of IF is a good trade-off between a gain-bandwidth product of amplifiers in an analog baseband and the flicker noise of the mixers. The former demands the lowest possible IF, especially in a broadband receiver, while the latter demands an IF high enough to easily eliminate the DC offset and $1/f$ noise effect. In addition, the reference clock is chosen to be 16.368 MHz to keep its high-order harmonics away from the GPS and compass bands[1].

Table 1. Frequency planning of this work ($f_0 = 1.023$ MHz).

Parameter	Compass	GPS
Radio frequency	$f_{RF} = 1526 f_0$	$f_{RF} = 1540 f_0$
LO frequency	$f_{LO1} = 1533 f_0$	$f_{LO1} = 1533 f_0$
	$f_{LO2} = 1536 f_0$	$f_{LO2} = 1536 f_0$
IF centre	$f_{IF1} = 7 f_0$	$f_{IF1} = 7 f_0$
	$f_{IF2} = 10 f_0$	$f_{IF2} = 4 f_0$
IF bandwidth	$4 f_0$	$2 f_0$
Reference clock	$16 f_0$	$16 f_0$
VCO frequency	$f_{VCO} = 3052 f_0$	$f_{VCO} = 3080 f_0$
Dividing ratio	Div.R_LO1 = 191.625	Div.R_LO1 = 191.625
	Div.R_LO2 = 192	Div.R_LO2 = 192

2.2. Capacitance multiplying approach

In a PLL, the loop filter plays a key role in system-level loop dynamics. In the proposed synthesizer, a 3rd passive loop filter implemented with resistance and capacitance arrays is
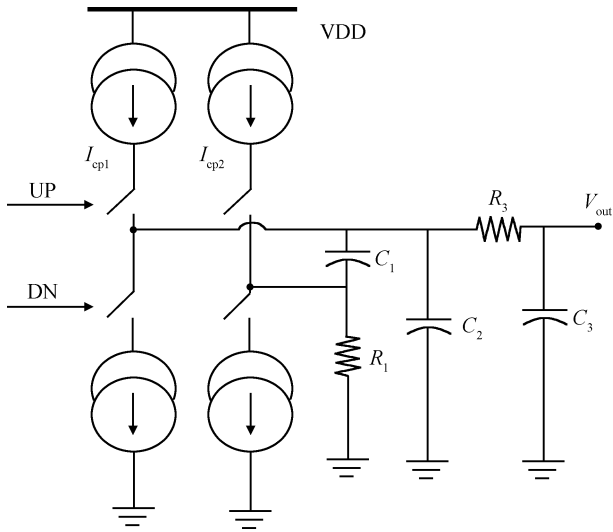
Fig. 3. Simplified architecture of the proposed capacitance multiplying approach.

Fig. 4. Schematic structure of prescaler8/9.

used to keep the loop stable and suppress the out-of-band phase noise and spurs. The optimum resistance and capacitance values are selected based on the reference clock for optimum phase margin and loop bandwidth. However, a large capacitor, which is the integration bottleneck, is usually needed in the loop filter to reduce the ripples of the control voltage on the VCO. To solve the problem of integrating a large capacitor on-chip without large area consumption, the approach of capacitance multiplying is proposed in this paper. Figure 3 illustrates the simplified architecture of this capacitance multiplier.

In order to get more insight into this technique, detailed analysis is given in the following part. The switching operation of the charge pump makes the PLL a discrete-time system. However, the loop bandwidth is much less than the input frequency, so the state of the PLL changes by a small amount during each cycle of the input. Thus a continuous-time approximation can be used to study the loop. As shown in Fig. 3, this capacitance multiplier involves two charge pumps with different operating currents I_{cp1} and I_{cp2}. We can assume that

$$I_{cp2} = N I_{cp1}. \tag{1}$$

The 3rd passive filter consists of two resistors R_1, R_3 and three capacitors C_1, C_2, and C_3. The output voltage V_{out} is the control voltage on the VCO varactor array for fine frequency tuning. Hence, the transfer function of I_{cp1} to V_{out} can be written as

$$H_{cp1}(s) = \frac{V_{out}}{I_{cp1}} = \frac{sR_1C_1 + 1}{s(C_1 + C_2) + s^2 R_1 C_1 C_2} \frac{1}{sR_3C_3 + 1}. \tag{2}$$

Similarly, the transfer function of I_{cp2} to V_{out} is given by

$$H_{cp2}(s) = \frac{V_{out}}{I_{cp2}} = \frac{R_1C_1}{C_1 + C_2 + sR_1C_1C_2} \frac{1}{sR_3C_3 + 1}. \tag{3}$$

In addition, the output voltage of the loop filter V_{out} is

$$V_{out} = I_{cp1} H_{cp1}(s) + I_{cp2} H_{cp2}(s). \tag{4}$$

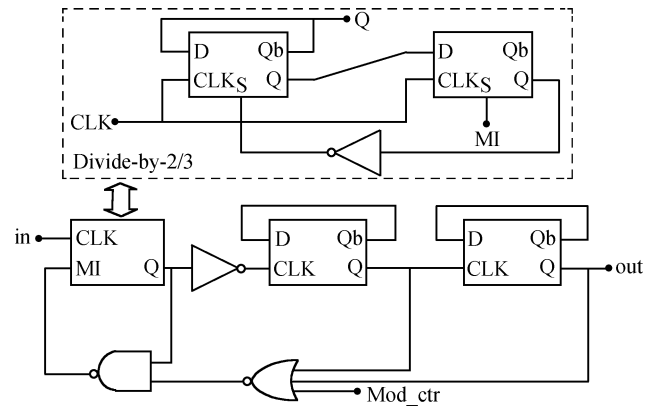According to Eqs. (1)–(3), Equation (4) can be drawn as

$$V_{out} = I_{cp1} H_{cp1}(s) + N I_{cp1} H_{cp2}(s)$$

$$= \frac{(N + 1)sR_1C_1 + 1}{s(C_1 + C_2) + s^2 R_1 C_1 C_2} \frac{1}{sR_3C_3 + 1}. \tag{5}$$

Comparing Eq. (5) and Eq. (2), we find that the effective capacitance of C_1 has been increased by $N + 1$ times by using I_{cp2}.

In this work, C_1 is designed to be 300 pF and I_{cp2} is four times larger than I_{cp1}, thus an effective capacitance as large as 1.5 nF can be obtained with an area of 300 pF with the help of this capacitance multiplying approach. Comparing the proposed capacitance multiplier with other approaches for loop filter integration such as a dual-path loop filter, a sample-reset loop filter and a resistor scaling loop filter[2], the control voltage V_{out} has fewer ripples and less sensitivity. However, additional active noise is introduced by the adoption of the other CP. Besides, the effect of clock feedthrough and charge sharing caused by current mismatch and parasitic capacitance needs to be carefully dealt with. Hence, special attention should be paid to the design of two CPs to minimize the in-band noise of the phase-locked loop.

2.3. Frequency divider

A programmable fractional-N frequency divider is employed in the synthesizer to realize channel selection. As depicted in Fig. 2, the frequency divider is based on pulse-swallow topology. It consists of a current-mode logic (CML)-to CMOS converter, a prescaler8/9, a digital counter and a 3rd MASH 1-1-1 $\Delta\Sigma$ modulator. The feedback signal output by the fractional-N frequency divider is re-synchronized by the output of the LO buffer to reduce the noise produced by the frequency divider for a further step.

True single-phase clocking (TSPC) is preferred to CML in prescaler8/9 design, because TSPC consumes much less power than CML at high frequency, such as 1.57 GHz in this work. A CML-to-CMOS converter is placed before the prescaler8/9 to realize the conversion from differential to single signal. Figure 4 demonstrates the architecture of the prescaler8/9. As shown in Fig. 4, the prescaler8/9 is composed of a divide-by-2/3 unit which has two D-flip flops and an inventor, two TSPC D-flip flops, and three logic gates. Design of the divide-by-2/3 unit
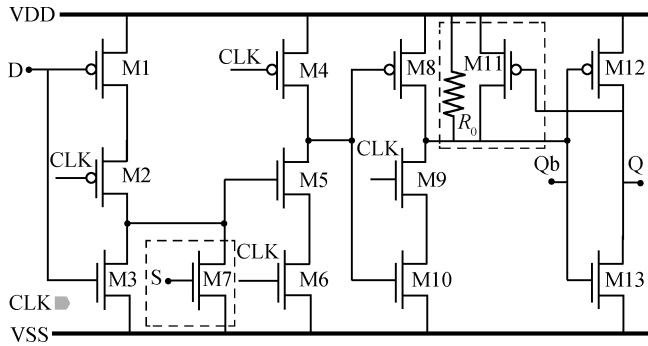
Fig. 5. Schematic of the TSPC D-flip flop used in the divide-by-2/3 unit.

is crucial because it operates at the highest frequency of all blocks. Schematic of the D-flip flop used in the divide-by-2/3 unit is shown in Fig. 5. The resistor R_0 is designed to be 100 kΩ, which is only used in the first D-flip flop. The reason for employing R_0 is that the node Qb can be pulled high when the circuit is cut-off to avoid the static leakage current.

In fractional-N synthesis, the instantaneous divisor value achieved by using different integers is always around the desired fractional value. The time-averaged divisor value is equal to the desired fraction when the loop is locked. However, switching between different divisors results in undesirable phase jitter or spurs near the desired carrier frequency. Thus, randomization techniques are needed to break the correlation and repeated patterns and to spread the spur energy over the frequency band. This is usually accomplished by using a $\Delta\Sigma$ modulator. A noise shaping $\Delta\Sigma$ modulator, which has a high-pass noise characteristic in the frequency domain, is used to control the integer divisor of the pulse-swallow divider such that the fractional spurs can be randomized and shifted to a higher frequency band where they can be easily eliminated by the loop filter. The MASH 1-1-1 structure is one of the most widely used topologies due to its stability, high-order in-band noise-shaping characteristic and easy implementation. In this work, a 3rd order 24-bit MASH 1-1-1 $\Delta\Sigma$ modulator is adopted. Mash 1-1-1 is a cascaded $\Delta\Sigma$ structure with three first-order loops. Each of the three loops is identical to the previous single-loop architecture. The quantization error generated in the first and second loops are totally cancelled and the total quantization noise is equal to that of a single loop, although three loops are used[3]. Therefore, the multi-loop $\Delta\Sigma$ architecture provides high-order noise shaping without additional quantization noise. The $\Delta\Sigma$ accumulator outputs are dithered around the desired value in the $I(z) - 3$ to $I(z) + 4$ range, where $I(z)$ is the integer divisor. $I(z)$ is expressed with a 7-bit word while the fractional divisor adopts a 24-bit word. Thus fine frequency resolution ($\ll$ 1 Hz) is achieved by using the 24-bit fraction.

In the programmable fractional frequency divider, the dual-modulus precaler8/9 and the CML-to-CMOS converter are completed by analog design, while counters of the pulse swallow divider and the 3rd MASH 1-1-1 modulator are implemented digitally with the help of a verilog-HDL and synthesis tools. The overall fractional divider consumes 0.96 mA from the power supply.

2.4. Other contributing blocks

The voltage controlled oscillator is the most determinant building block of the frequency synthesizer. Phase noise and frequency tuning range are the most important characteristics. Designing an optimized VCO with good performance is challenging because compromises must be made among many different variables which all interact with others.

As demonstrated in Fig. 6(a), the VCO proposed in this work is based on a current steered LC tank structure. To obtain sustained oscillation, cross-coupled PMOS transistors M1 and M2 are adopted to provide negative resistances by forming a positive feedback loop to cancel the LC tank loss. PMOS is preferred to NMOS due to its lower frequency flicker noise. The frequency range is tuned coarsely by a 4-bit switched capacitor array, thus there are sixteen sub frequency bands in total. An automatic frequency control (AFC) scheme is introduced for fast switching among different sub-bands. Fine frequency tuning is accomplished with two PMOS varactors which are tuned by the control voltage from the loop filter. C_3 and C_4 are designed as 6 pF to suppress instantaneous voltage variation of the varactors. Fixed capacitors C_5 and C_6 are used to reduce the frequency changes over temperature, voltage and process variations. L_0 is a differential symmetric inductor with a high Q value for low phase noise considerations. A small inductor L_1 is used for filtering substrate noise. Experimental results show that the achieved frequency tuning range is from 2.9 to 3.3 GHz and the average K_{VCO} is 105 MHz/V. Good noise performance is attained when the tail current is set at 1.6 mA.

The VCO buffer is designed to isolate the VCO from on chip noise, captive loading, and frequency pulling. A schematic of the VCO buffer is shown in Fig. 6(b). The output signal of the VCO is ac coupled by two small capacitors and sent into two differential common source NMOS transistors M1 and M2. The gates of M1 and M2 are biased at 900 mV through two resistors R_1 and R_2. Cascode topology is adopted for its high output impedance and good reverse isolation. M3 and M4 are cascode transistors whose gates are connected to the power supply. The resistor loads R_3 and R_4 need to be carefully designed for acquiring a high output voltage. The driving capability can be adjusted by programming the tail current which varies from 1 to 2.5 mA.

A schematic of the divide-by-2 is shown in Fig. 7(a). It is used as the quadrature LO generator, which consists of two CML D-latches. Since the divider runs at the maximum frequency, it is very important to improve the operating speed of D-latches. As illustrated in Fig. 7(b), a novel D-latch is adopted in this work. Two transistors M7 and M8 working in the linearity region are used as the load rather than the traditional resistor load[4]. The equal resistance R_{on} of M7 and M8 is given in the following equation.

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{V_{DS}}{\mu_p C_{ox} \dfrac{W}{L} \left[(V_{GS} - V_{TH})V_{DS} - \dfrac{1}{2}V_{DS}^2 \right]}$$

$$= \frac{1}{\mu_p C_{ox} \dfrac{W}{L} \left(V_{GS} - V_{TH} - \dfrac{1}{2}V_{DS} \right)}. \tag{6}$$

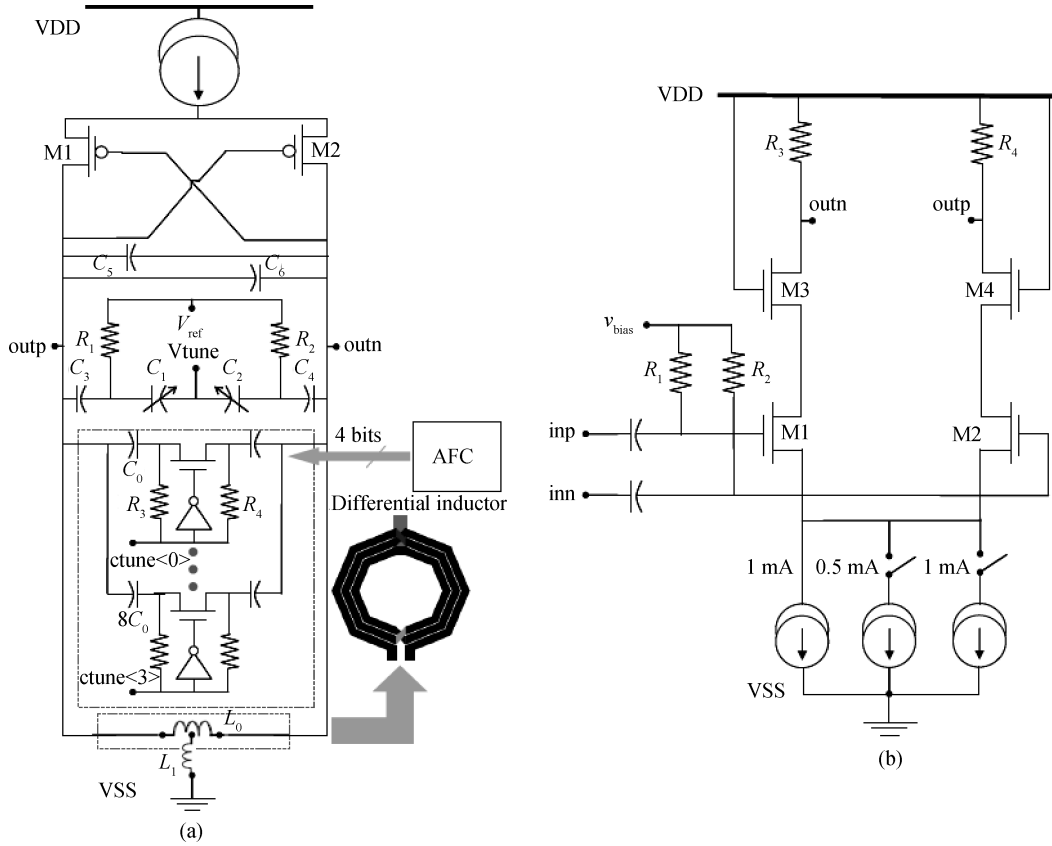When V_{DS} decreases, R_{on} becomes smaller which is desir-

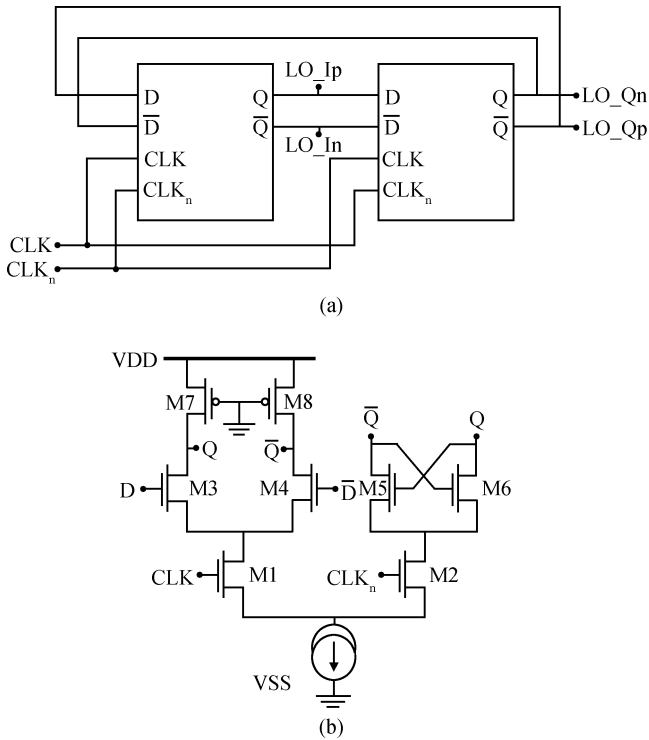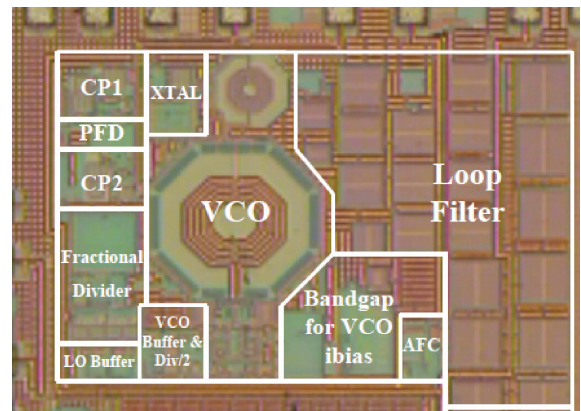Fig. 6. (a) Schematic of a VCO. (b) Schematic of a VCO buffer.

Fig. 8. Die photo of the proposed frequency synthesizer.

The divide-by-2 circuit can operate at 3.4 GHz and dissipates 0.8 mA from a 1.2 V power supply.

3. Experimental results

The proposed synthesizer is fabricated in a 0.13 μm CMOS process, and occupies an area of 0.92 mm^2. Figure 8 shows a die photograph of this synthesizer.

The proposed PLL has demonstrated good noise and spur performance in tests. Measurement results of 1571.328 MHz are shown in Fig. 9. As illustrated in Fig. 9(a), the reference spur is −53 dBc when the PLL works in integer mode. Phase noise achieves −92.9 dBc/Hz and −121 dBc/Hz at 100 kHz and
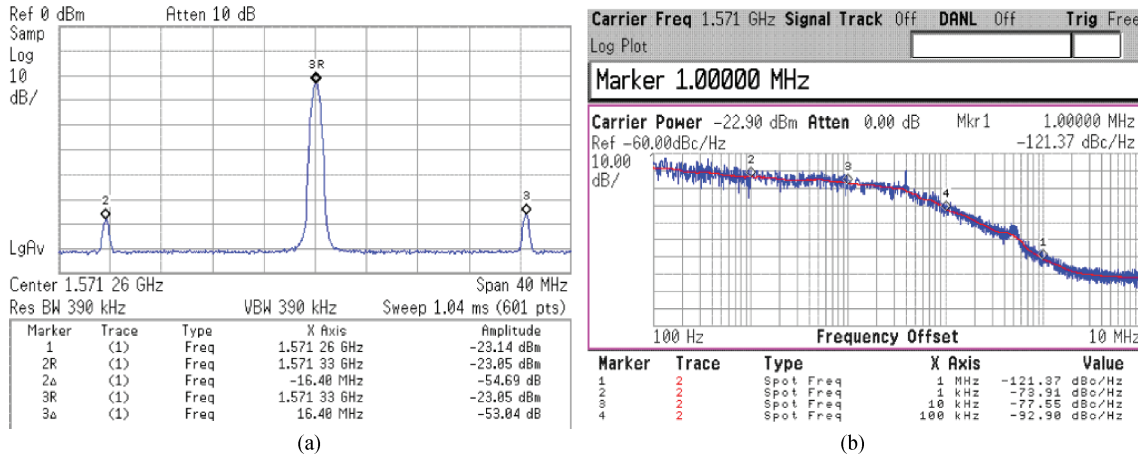

Fig. 7. (a) Schematic architecture of a divide-by-2 LO generator. (b) Schematic of the CML D-flip flop.

able for Q or $\overline{Q}$ to turn to high logic. Hence, both high speed and low power consumption are acquired with the D-latch.

(a)   (b)

Fig. 9. (a) Frequency spectrum of 1571.328 MHz. (b) Phase noise performance of 1571.328 MHz.

(a)   (b)
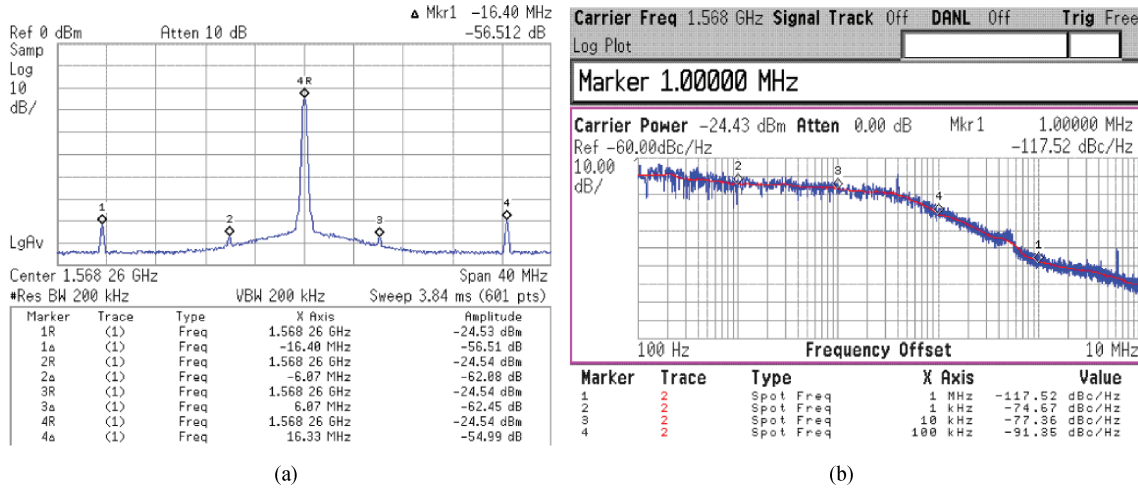
Fig. 10. (a) Frequency spectrum of 1568.259 MHz. (b) Phase noise performance of 1568.259 MHz.

Table 2. Performance comparison with other related works.

Parameter	Ref. [5]	Ref. [6]	Ref. [7]	This work
Supply voltage (V)	1	1.8	1.8	1.2
Technology	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.13 μm CMOS
Application	GPS L1	GPS L1/L2	GNSS	GPS L1, Compass
Loop filter	off-chip	off-chip	off-chip	on-chip
Phase noise (dBc/Hz)	N/A	−90 @ 100 kHz	−95 @ 200 kHz	−91.3 @ 100 kHz
	−110 @ 1 MHz	−112 @ 1 MHz	−118 @ 1 MHz	−117 @ 1 MHz
Power dissipation (mW)	1.2	5.6	11.2	10.32
Area (mm^2)	N/A	N/A	0.53	0.92

1 MHz offset separately as given in Fig. 9(b). When the proposed synthesizer works in fractional mode, the LO signal is locked at 1568.259 MHz. The frequency spectrum and spur performance of 1568.259 MHz is shown in Fig. 10. Fractional spurs are less than −62 dBc and the reference spur located at 16.368 MHz is −55 dBc as shown in Fig. 10(a). Phase noise achieves −91.3 dBc/Hz and −117.5 dBc/Hz at 100 kHz and 1 MHz offset separately as given in Fig. 10(b).

4. Conclusion

In this paper, a $\Delta\Sigma$ fractional-N frequency synthesizer fabricated in a 0.13 μm CMOS technology is proposed for the application of a dual-mode GPS and Compass receiver. The proposed synthesizer consumes 8.6 mA current from a 1.2 V supply and occupies an area of 0.92 mm^2 excluding PADs. Table 2 gives a performance summary of this work and a comparison with other related works[5−7].

References

[1] Gramegna G, Mattos P G, Losi M, et al. A 56-mW 23-mm^2 single-chip 180-nm CMOS GPS receiver with 27.2-mW 4.1-mm^2 radio. IEEE J Solid-State Circuits, 2006, 41(3): 540

[2] Shu K, Sanchez-Sinencio E. CMOS PLL synthesizers: analysis and design. Springer, 2005: 127

[3] Rogers J, Plett C, Dai F. Integrated circuit design for high-speed frequency synthesis. Artech House, 2006: 315

[4] Hung C M, Floyd B A, Park N, et al. Fully integrated 5.35-GHz CMOS VCOs and prescalers. IEEE Trans Microw Theory Tech, 2001, 49(1): 17

[5] Cheng K W, Natarajan K, Allstot D. A 7.2 mW quadrature GPS receiver in 0.13 μm CMOS. IEEE International Solid-State Cir-

cuits Conference, 2009: 422

[6] Jia Hailong, Ren Tong, Lin Min, et al. A low power dissipation wide-band CMOS frequency synthesizer for a dual-band GPS receiver. Journal of Semiconductors, 2008, 29(10): 1968

[7] Yu Yunfeng, Yue Jianlian, Xiao Shimao, et al. A low-power CMOS frequency synthesizer for GPS receivers. Journal of Semiconductors, 2010, 31(6): 065012