Total dose ionizing irradiation effects on a static random access memory field programmable gate array

Gao Bo(高博)[1,2,3], Yu Xuefeng(余学峰)[1,2,†], Ren Diyuan(任迪远)[1,2], Li Yudong(李豫东)[1,2], Sun Jing(孙静)[1,2], Cui Jiangwei(崔江维)[1,2,3], Wang Yiyuan(王义元)[1,2,3], and Li Ming(李明)[1,2]

[1]Xinjiang Technical Institute of Physics & Chemistry, Chinese Academy of Sciences, Urumqi 830011, China
[2] Xinjiang Province Key Laboratory of Electronics Information Material and Device, Urumqi 830011, China
[3]Graduate University of the Chinese Academy of Sciences, Beijing 100049, China

Abstract: SRAM-based FPGA devices are irradiated by ^{60}Co γ rays at various dose rates to investigate total dose effects and the evaluation method. The dependences of typical electrical parameters such as static power current, peak–peak value, and delay time on total dose are discussed. The experiment results show that the static power current of the devices reduces rapidly at room temperature (25 ℃) and high temperature (80 ℃) annealing after irradiation. When the device is irradiated at a low dose rate, the delay time and peak–peak value change unobviously with an increase in the accumulated dose. In contrast, the function parameters completely fail at 2.1 kGy(Si) when the dose rate increases to 0.71 Gy(Si)/s.

Key words: SRAM-based FPGA; γ-^{60}Co; ionizing irradiation effects; evaluation methods
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1. Introduction

FPGA is the densest and most advanced programmable logic device. It enables a designer to shorten the cycle of design, decrease the cost of design, reduce the risk of design and implement large digital designs in a device at any time in any location. In general, it has the advantages of high integrated level, high performance, low power, small size and fast speed. These advantages give the FPGA device promising application prospects for meeting the ”better, faster, cheaper” trend in aerospace. With the rapid development of technology, the FPGA device has a higher integrated level, stronger function and smaller dimensions. So the performance parameters are easier to influence in the ionization radiation environment of space. Once an FPGA device’s function fails, it will greatly impact the electronic systems of satellites and thereby affect the reliability and shorten the lifetime of satellites.

In the 1990s, research on ionizing irradiation effects of a FPGA device had been started[1−5], but the attention mainly concentrated on engineering applications and single event effects. In recent years, we have also made some progress in studying the ionizing irradiation effects of FPGA devices. We are mostly interested in single event effects and ionizing irradiation effects of anti-fuse technology FPGA devices[6−8]. As for the SRAM-based FPGA device, especially the Altera SRAM-based FPGA device, there are just a few reports on the ionizing irradiation damage mechanism. What’s more, an SRAM-based FPGA device has the ability for reconstruction online, so there are extensive application prospects in the field of aerospace.

Although radiation hardened FPGA devices are available, they are much more expensive than COTS devices, and thus when cost is a major issue they are not affordable. In order to cope with dependability issues, we carried out total dose experiments for COTS devices[9]. The total dose experiments of the FPGA device help us to understand their ionizing irradiation effects and mechanism. Meanwhile, they provide technical support for the establishment of ionizing irradiation evaluation methods. But the diversity of FPGA technologies and architectures make the evaluation of radiation effects complex at the levels of both device and system.

In this paper, we have studied total dose ionizing irradiation effects and the evaluation method of SRAM-based FPGA devices under different dose rates. The dependence of static power current upon accumulation dose and annealing time at different annealing temperatures are discussed. We also analyze the reason why the static power current of the devices decreases rapidly during room temperature (25 ℃) and high temperature (80 ℃) annealing after irradiation. Perhaps evaluation technology in FPGA anti-radiation levels is confidential, so we do not have the relevant report about the phenomenon that static power current does not recover at the beginning of an 80 ℃ annealing process but continues to increase and then decrease. Meanwhile, the peak–peak value and delay time of the output waveform are measured remotely under different dose rates. The dependences of peak–peak value and delay time on accumulation dose are discussed. Our experiment results are meaningful and important for further improvements in design and processing.

2. Experimental details

2.1. Devices under test

We have studied the total dose ionizing irradiation effects on field programmable gate arrays. A series of EP1C6Q240C8 from Altera were irradiated with a γ-^{60}Co radiation source. These devices were chosen to represent the current device family of the manufacturer. Meanwhile, the simple structure of

† Corresponding author. Email: yuxf@ms.xjb.ac.cn
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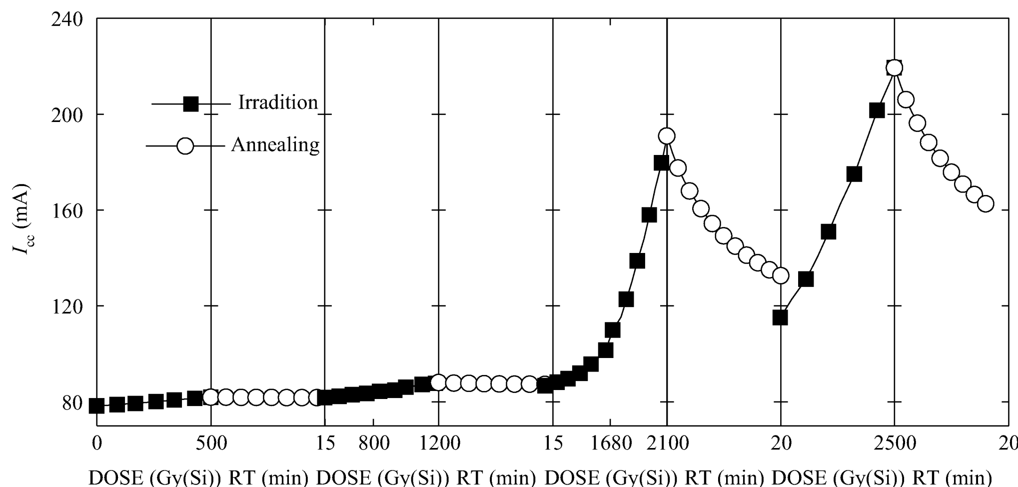

Fig. 1. Static power current versus accumulated dose at a 0.71 Gy(Si)/s dose rate and 25 ℃ annealing.

these devices could also reduce the testing complexity[10−12]. The EP1C6Q240C8 is based on a low voltage (1.5 V) design in a 0.13-μm all-layer copper SRAM process, with densities up to 5980 logic elements (LEs) and up to 92162 bits of RAM. The speed grade of the chips to be tested was 8. Every device is packaged in a cavity up 240-pin plastic quad flat pack[10−12]. The Cyclone is a reduced feature-set version of the Altera Stratix FPGA. The Cyclone and Stratix devices are manufactured in the same process, which allows the results for the Cyclone to be extrapolated to the Stratix[12].

2.2. Experimental methods

The total dose experiment was carried out on seventy-thousand curies of a ^{60}Co γ radiation source. The dose rate was calibrated using a Fricke (ferrous sulfate) dosimeter. The devices were irradiated by ^{60}Co γ-rays to a level of 2.5 $\times$ 10^3 Gy(Si), and the dose rate was 0.71 Gy(Si)/s, 7.73 $\times$ 10^{-2} Gy(Si)/s and 7.8 $\times$ 10^{-3} Gy(Si)/s respectively. In this experiment, the exposure board contained an FPGA device, a power module, a configuration chip, etc. Before irradiation, we built a lead chamber, to protect the power module and the configuration chip, which was beneficial in analyzing accurately the relationship between the performance of the FPGA device and the accumulation dose.

During irradiation and annealing, there was a static bias condition for the testing samples. The bias condition was $V_{\rm CCIO}$ = 3.3 V, $V_{\rm CCINT}$ = 1.5 V, $V_{\rm SS}$ = 0 V, and the floating signal ports. The irradiated FPGA devices were connected to a personal computer kept outside the radiation area. The monitoring of static power current about the FPGA devices was performed by this PC. We had real-time monitoring of the static power current of the FPGA devices as a function of total dose and annealing time respectively. When the dose rate was 0.71 Gy(Si)/s and 7.73 $\times$ 10^{-2} Gy(Si)/s, we observed the static power current as a function of time at 25 ℃ annealing after irradiation. When the dose rate was 0.71 Gy(Si)/s, we put the irradiated FPGA device into a high temperature furnace after irradiation and found how the static power current changed with time during 80 ℃ annealing after irradiation. We also studied the device's delay time and peak–peak value as a function of accumulation dose under different dose rates.

3. Experimental results and discussion

3.1. Experimental results

Figure 1 shows the static power current as a function of accumulation dose and annealing time when the device is irradiated at the 0.71 Gy(Si)/s dose rate and then annealed at 25 ℃ after irradiation. The static power current increases as the accumulated dose increases, and then quickly decreases during annealing at 25 ℃ after irradiation. In the third irradiation and annealing process, it is found that the static power current increases from 86.72 to 190.86 mA during irradiation under a 0.71 Gy(Si)/s dose rate while it quickly decreases from 190.86 to 132.56 mA during annealing after irradiation at room temperature for 20 min. Then we shift tested the device's function parameter. It is found that when the next irradiation process begins, the static power current has already decreased to 115.18 mA.

Figure 2 shows the static power current as a function of accumulated dose and annealing time when the device is irradiated at the 0.71 Gy(Si)/s dose rate and then annealed at 80 ℃ after irradiation. The static power current increases as accumulated dose increases, as shown in Fig. 2. When we put the irradiated FPGA devices into a high temperature furnace, the device's static power current does not recover immediately at the beginning of the 80 ℃ annealing but shifts to a worse position and then decreases rapidly with annealing time. (The static power current slowly decreases in the initial stage of 80 ℃ annealing, as shown in Fig. 2. This is because the FPGA device was in a room temperature environment and not placed into a high temperature furnace at this stage.)

Figure 3 shows the static power current versus accumulated dose and annealing time when the device is irradiated at a 7.73 $\times$ 10^{-2} Gy(Si)/s dose rate and then annealed at 25 ℃ after irradiation. From the figure we see that the static power current increases with the increase in accumulated dose, and then quickly decreases at 25 ℃ annealing after irradiation.

Figure 4 shows the device's delay time and peak–peak value as a function of accumulated dose under different dose

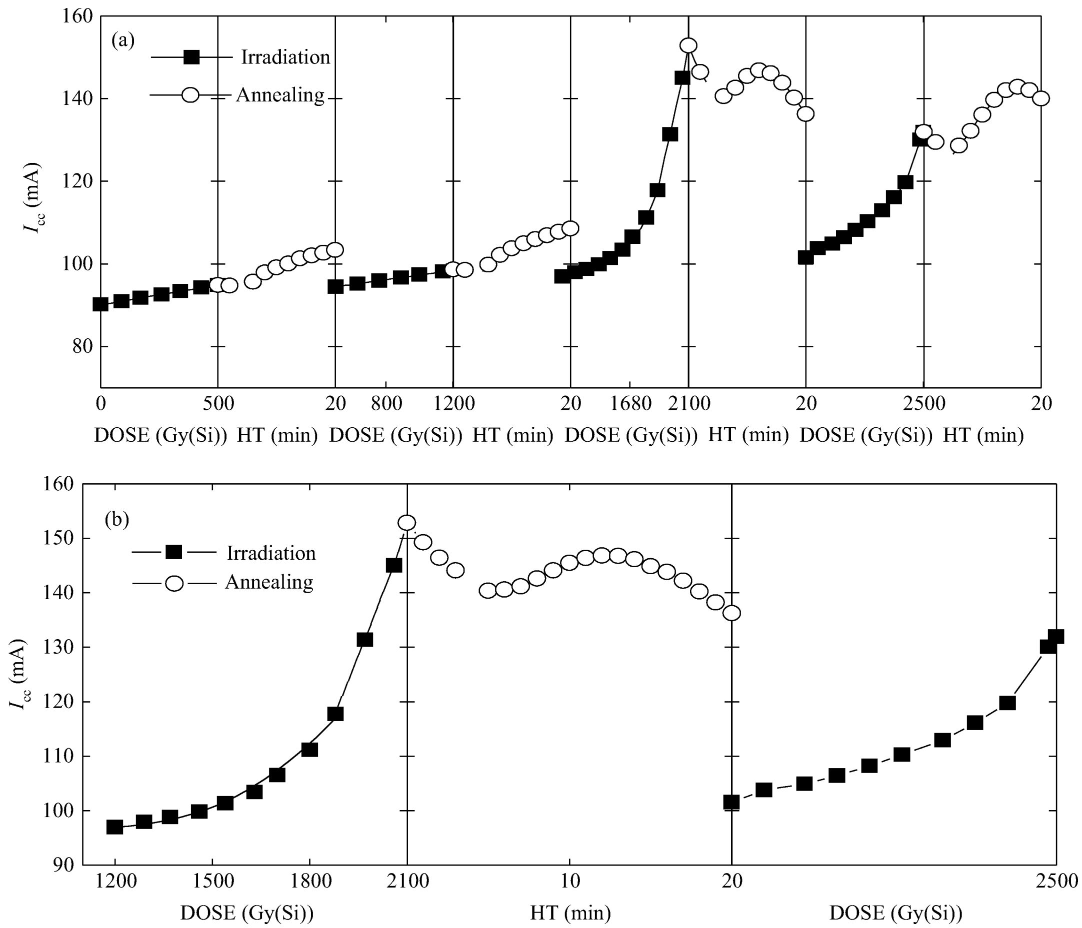

Fig. 2. Static power current versus accumulated dose at a 0.71 Gy(Si)/s dose rate and 80 ℃ annealing time.

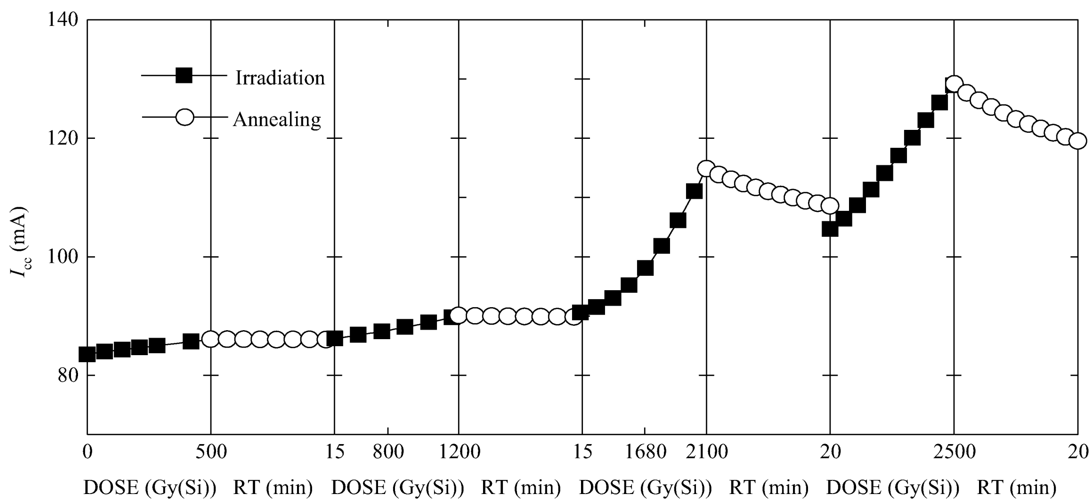

Fig. 3. Static power current versus accumulated dose at a 7.73×10^{-2} Gy(Si)/s dose rate and 25 ℃ annealing time.

rates. When the device is irradiated at a 7.73×10^{-2} Gy(Si)/s dose rate and a 7.8×10^{-3} Gy(Si)/s dose rate, the delay time and peak–peak value change unobviously with increasing accumulated dose, as shown in Fig. 2. When the accumulated dose reaches 2.5 kGy(Si), the device's function parameters remain at normal levels. Nevertheless, the function parameters completely fail at 2.1 kGy(Si) when the dose rate increases to 0.71 Gy(Si)/s.

3.2. Results and discussion

Ionization irradiation effects are mainly caused by the interaction of high-energy photons or charged particles (protons, electrons, or energetic heavy ions, i.e.) with the atoms of the gate dielectric of the material. When a photon or charged particle travels through a material, it interacts with electrons in the material and causes some of the atoms to become ionized,

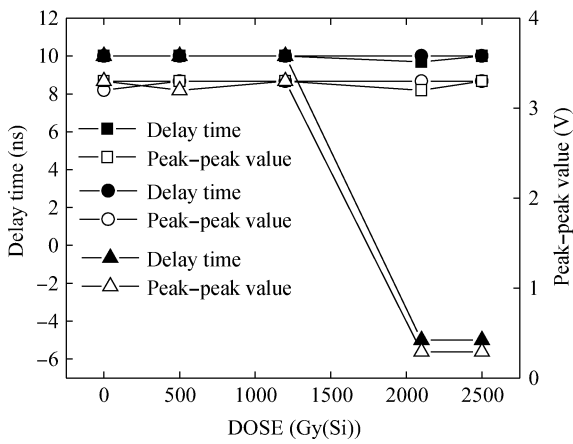

Fig. 4. Peak–peak value and delay time versus accumulated dose at different dose rates. ■ 7.8×10^{-3} Gy(Si)/s, ● 7.73×10^{-2} Gy(Si)/s, ▲ 0.71 Gy(Si)/s.

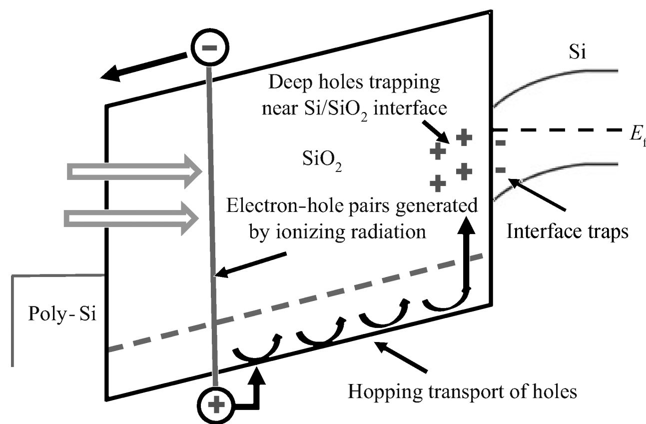

Fig. 5. Schematic energy band diagram for a MOS structure, indicating major physical processes underlying radiation response[14].

creating electron–hole pairs along the track of the incident particle. With the processes of generation, compound, drift, diffusion, accumulation and recombination of these electron–hole pairs, they produce oxide trapped charges in the SiO_2 insulating layer and interface state charges in the Si–SiO_2 interface. These trapped charges lead to obvious changes in device performance parameters, and even malfunction[13, 14]. Figure 5 shows a schematic energy band diagram of a MOS structure, where positive bias is applied to the gate, so that electrons flow toward the gate and holes move to the Si substrate. Four major physical processes, which contribute to the radiation response of a MOS device, are also indicated[14]. In sub-micron devices, the hole trapping near the Si/SiO_2 interface is the primary effect[15].

Figures 1 and 3 show that the static power current decreases rapidly as annealing time increases. We know that because the process improves and the gate oxide layer level becomes thin, the gate oxide layer of the CMOS technology FPGA device is not sensitive to total irradiation dose damage. Instead, the irradiation damage mainly relates to field oxide layer isolation. The trapped charges of the field oxide layer, particularly the shallow energy level trapped charges, $E_{\delta'}$ center defect, play an important role in the oxide-trapped holes. $E_{\delta'}$ defects are known to be high capture cross section hole traps in SiO_2. In several studies, the $E_{\delta'}$ has been associated with the dimer O vacancy defect that is illustrated in Fig. 6[16]. Most $E_{\delta'}$ center energy levels locate at the SiO_2 band gap about 0.5–1.0 eV above the valence band. So the electrons can easily tunnel into the SiO_2 layer and composite with the trapped holes[16]. As a result, trapped holes can be annealed by electrons tunneling directly from the valence band of either the polysilicon gate or the Si substrate, regardless of the polarity of the applied gate bias, which leads to the static power current return drift. The reduction of static power current is due to the annealing of trapped holes. When the device is irradiated at different dose rates, we observe the same phenomenon that the static power current decreases fast as annealing time increases.

During 80 ℃ annealing, the static power current does not recover at the beginning of 80 ℃ annealing but continues to increase and then decrease, as shown in Fig. 2. This is mainly because at the initial period of 80 ℃ annealing, some defects gain activity and turn into an activated state, resulting in the static power current's continual drifting. Bias annealing is not a thorough defect-annihilation process and just removes the activation energy of some traps, when at high temperature some oxide-trapped charges return to an active state[17]. Therefore, the static power current first shows a continual increase, and then drifts back quickly during 80 ℃ annealing after irradiation.

Figure 4 shows the delay time and peak–peak value of the FPGA device change with the variation of accumulated dose under different dose rates. When the accumulated dose reaches 2.1 kGy(Si), the function parameters of the FPGA device fail during high dose rate irradiation, as shown in Fig. 4. We believe that it accumulates massive oxide-trapped charges in a short time during high dose rate irradiation. Simultaneously, it doesn't have enough time to generate interface state trapped charges, as shown in Fig. 7.

As is known, numerous electron–hole pairs would be generated in SiO_2, most of which can survive by recombination and transport in response to the electric field building in and out of the SiO_2. At room temperature, the intrinsic mobility of holes is about one-million time less than that of electrons. Thus, the holes are left behind after the electrons are driven out of the oxide, which could create trapped holes[18]. For the case of a very high dose rate, the mobile holes reach the interface long before the protons. When the number of trapped holes becomes sufficiently large, they can create an electrostatic barrier near the interface that will prevent other mobile particles from reaching the interface[19]. For a very low dose rate, the rate of interface-trap buildup is very slow. This means that there is enough time for protons to get released, reach the interface, and react with the SiH bond to form interface traps. In this case, the protons will participate in both charge buildup and in interface-trap formation[19].

The cumulative oxide-trapped charges make the threshold voltage of the N channel transistor drift negatively, causing function failure of the FPGA device. At the same time, the generation rate of the oxide-trapped charges is slow during low dose rate exposure. Therefore, the function parameters of the FPGA device still remain normal at the accumulated dose of 2.5 kGy(Si).

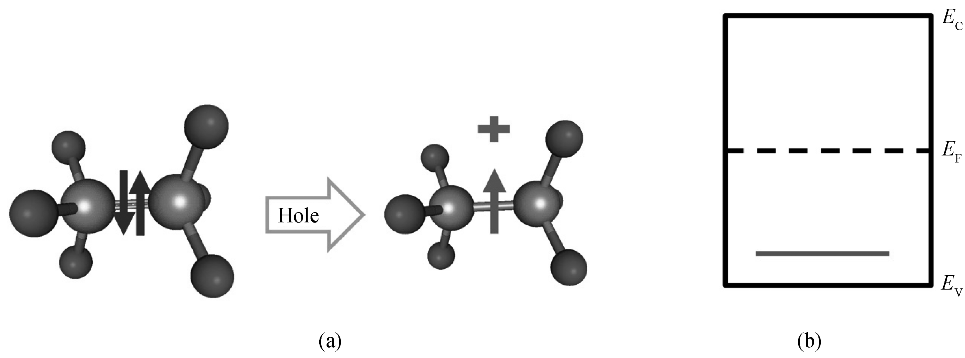

Fig. 6. (a) Schematic illustration of $E_{\delta'}$ defect[16] and (b) trapped hole energy distribution.

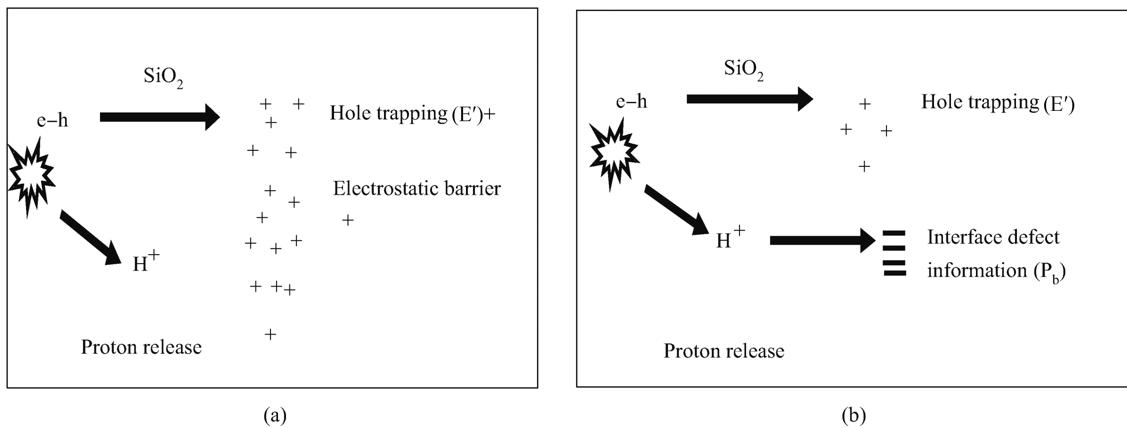

Fig. 7. (a) High dose rate irradiation and (b) low dose rate irradiation.

4. Conclusions

In this paper, we have studied the ionizing irradiation effects and evaluation methods of an SRAM-based FPGA device. The results of our experiments are meaningful and important.

(1) The trapped hole defects are mostly $E_{\delta'}$ center, which locate 0.5–1.0 eV above the valence band. These defects are easily neutralized by substrate electron tunneling during annealing after irradiation, which causes the static power current to reduce significantly.

(2) In the initial period of 80 ℃ annealing, some defects gain activity and turn into an activated state, so that the device's power current does not recover at the beginning of 80 ℃ annealing but continues to increase and then decreases rapidly with annealing time.

(3) During low dose rate exposure, the generation of oxide-trapped charges follows the annealing of oxide-trapped charges, so that the function failure value of the device is much larger than the value of the high dose rate.

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